Freescale Semiconductor, Inc.

Motorola's ColdFire® MCF5407 Integrated Microprocessor

The MCF5407 integrated microprocessor builds on the success of the award winning⁽¹⁾ MCF5307 device by combining its peripheral set with the high performance Version 4 (V4) ColdFire core, achieving a 233 Dhrystone 2.1 MIPS performance level at 162MHz. The fine-tuned capabilities of the single pipeline in the V4 Harvard microarchitecture deliver an amazingly efficient 1.44 MIPS/MHz without the additional cost of a second pipeline. With this outstanding performance level, code compatibility, and well received integration, the MCF5407 processor maximises value for a broad range of embedded applications while decreasing overall time to market.

High System Performance

RISC architectures have traditionally favoured performance at the expense of code density. To improve code density, many architectures offer a front-end add-on to support compressed instruction formats, but performance suffers. The V4 ColdFire core hits the "sweet spot" in this tradeoff. With the excellent code density of the ColdFire architecture,

processor bus bandwidth requirements are greatly reduced, while still achieving outstanding levels of system performance. The MCF5407 device's significant performance increase represents more than three times the performance and twice the system efficiency of any previous ColdFire standard product, providing a compelling migration path for existing ColdFire designs. In addition, the MCF5407 product offers an exciting roadmap for users of the MC68EC040 and MC68EC060, offering more than twice the performance of the 68EC060 and a broad array of integration that is not available on either device, all at a fraction of the price.

Integrated Peripherals

To accelerate system design and reduce system cost, the MCF5407 processor offers a rich array of memory and peripheral integration in an awardwinning(1) combination. Features common to many embedded applications, such as DMAs, Timers, an SDRAM interface, UART and USART and on-chip memories are integrated cost-effectively using aggressive process technologies.







For More Information On This Product, Go to: www.freescale.com



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Contact Information:

Motorola offers user's manuals, product briefs and application notes for all of its ColdFire microprocessors. In addition, local support is also provided for these products. This information can be found at http://www.motorola.com/ColdFire

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at: 800-521-6274 or http://www.motorola.com/semiconductors

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Fast Time to Market

The MCF5407 product extends the successful 68K family by providing a compatible environment for 68K and ColdFire microprocessor customers allowing leverage of world-class third-party development tools, software and programmer familiarity. In fact, customers moving from 68K to ColdFire microprocessors can use code translation and emulation tools free of charge, and subject to a licensing agreement, to facilitate modifying and reusing 68K assembly. The package, pinout and integration mix of the MCF5407 processor create an extremely simple pin-to-pin compatible upgrade with three times the performance for current MCF5307 device designs. By delivering on the development roadmap for the 100% synthesizable ColdFire family, Motorola provides room to grow and powerful new capabilities to designers eager to create new classes of electronic products, while leveraging their previous investments.

Features

- V4 ColdFire processor core with Harvard memory architecture and branch cache acceleration logic
 - Limited superscalar design
 - Fully code compatible with Version
 2 & 3 ColdFire processor core
 - Enhanced instruction set
- 16K Instruction-cache, 8K data-cache.
- 4KByte SRAM.
- Multiply Accumulate (MAC) with integer and fractional capabilities.
- Industry leading debug module offering both background and real
- For More Information On This Product, a new product under development. Specifications and information herein are subject to change without notice.
 - Hardware integer divide unit.

- Integrated Processor
 - DRAM Controller: (glueless interface to SDRAM, FPM and EDO)
 - 1 UART, 1 synchronous UART
 - Four fully programmable DMA Channels
 - Eight Chip Selects
 - 16-bit General Purpose I/O
 - Two 16-bit Timers
 - I² C module
 - System Integration (PLL, SW Watchdog)
- Doze Mode & Variable frequency operation.

Product Specifications

- 233 Dhrystone 2.1 MIPS at 162 MHz.
- + 0°-70°C operating temperature.
- Implemented in 0.22µm, QLM.
- Requires 1.8V and 3.3V power supply.
- 208-pin plastic QFP package.
- Pin compatible with MCF5307 (note voltage and timing changes).

16 K Instruction Cache	V4 I Addr Gen I Fetch 1	8 K Data Cache
2K SRAM	I Fetch 2 IEDecode	System Bus Controller
2K SRAM	Instr Buf Dec&Sel Op	DRAM Cntr & Chip
UART/ USART	Addr Gen Op Fetch 1	Selects Interrupt Ctr
2 Timers	Op Fetch 2 Execute	General Purpose I/O
4 DMAs	MAC H/W Divide	l²C
JTAG	Debug Module	PLL



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(1) The MCF5307 won the Editor's Choice Award for "1998 Microprocessor of the Year" from Microprocessor report.