REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R020-99. - LTG	99-01-28	Monica L. Poelking
B	Changes in accordance with NOR 5962-R009-00. - TVN	00-01-12	Monica L. Poelking
C	Correct test conditions V_{IN} and V_{OUT} for I_{IL} and I_{OFL}, respectively, in table I. Delete I_{OH} and I_{OL} in footnote 3/ in table I. Add test circuit and output waveform for data floating test (t_{DF}). Update boilerplate. Editorial changes throughout. - TVN	00-07-14	Monica L. Poelking
D	Update boilerplate to MIL-PRF-38535 requirements. - CFS	05-09-07	Thomas M. Hess
E	Update boilerplate to MIL-PRF-38535 requirements. - PHN	19-07-26	Thomas M. Hess

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	E	E	E	E	E	E	E	E	E										
SHEET	15	16	17	18	19	20	21	22	23										

REV STATUS OF SHEETS															
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
87-08-26

REVISION LEVEL
E

SIZE
A

CAGE CODE
67268

5962-87548

SHEET 1 OF 23

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, PROGRAMMABLE COMMUNICATION INTERFACE, MONOLITHIC SILICON

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87548	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8251A	Programmable communication interface
02	8251A	Programmable communication interface

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to +7 V dc
Input voltage range ..... -0.5 V dc to +7 V dc
V_{CC} with respect to V_{SS} ..... -0.5 V dc to +7 V dc
All signal voltages with respect to V_{SS} ..... -0.5 V dc to +7 V dc
Maximum power dissipation (P_D) ..... 1.0 W
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 5 seconds) ..... +270°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}):
Device type 01 ..... +4.5 V dc to +5.5 V dc
Device type 02 ..... +4.75 V dc to +5.25 V dc
Minimum low level input voltage (V_{IL}) ..... -0.5 V dc
Minimum high level input voltage (V_{IH}) ..... +2.2 V dc
Maximum low level input voltage (V_{IL}) ..... +0.8 V dc
Maximum high level input voltage (V_{IH}) ..... V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 True table. The true table shall be as speciified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5 V ±10% for device type 01 V_{CC} = 5 V ±5% for device type 02 unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		All	1, 2, 3		0.8	V
Input high voltage	V_{IH}		All	1, 2, 3	2.2		V
Low level output voltage	V_{OL}	I_{OL} = 2.2 mA	All	1, 2, 3		0.45	V
High level output voltage	V_{OH}	I_{OH} = -400 µA	All	1, 2, 3	2.4		V
Input leakage current	I_{IL}	V_{IN} = V_{CC} max and 0.45 V	All	1, 2, 3		±10 1/	µA
Output float leakage current	I_{OFL}	V_{OUT} = V_{CC} max and 0.45 V	All	1, 2, 3		±10 1/	µA
Power supply current	I_{CC}	Outputs unloaded static 2/	All	1, 2, 3		120	mA
Input capacitance	C_{IN}	f_C = 1 MHz See 4.3.1d	All	4		10	pF
I/O capacitance	$C_{I/O}$	Unmeasured pins returned to GND See 4.3.1d		4		20	
Functional test		See 4.3.1c	All	7, 8			
READ CYCLE							
Address stable before $\overline{RD}$	t_{AR}	See figure 4 3/ 4/ 5/	All	9, 10, 11	0		ns
Address hold time to $\overline{RD}$	t_{RA}	See figure 4 3/ 4/ 5/	All	9, 10, 11	0		ns
$\overline{RD}$ pulse width	t_{RR}	See figure 4 3/ 4/	All	9, 10, 11	250		ns
Data delay from $\overline{RD}$	t_{RD}	See figure 4 3/ 4/ 6/ 7/	All	9, 10, 11		200	ns
$\overline{RD}$ to data floating	t_{DF}	See figure 4 3/ 4/	All	9, 10, 11	10 1/	250	ns
WRITE CYCLE							
Address stable before $\overline{WR}$	t_{AW}	See figure 4 3/ 4/	All	9, 10, 11	0		ns
Address hold time to $\overline{WR}$	t_{WA}	See figure 4 3/ 4/	All	9, 10, 11	20		ns
$\overline{WR}$ pulse width	t_{WW}	See figure 4 3/ 4/	All	9, 10, 11	250		ns
Data setup for $\overline{WR}$	t_{DW}	See figure 4 3/ 4/	All	9, 10, 11	150		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5 V ±10% for device type 01 V_{CC} = 5 V ±5% for device type 02 unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
WRITE CYCLE - Continued								
Data hold for $\overline{WR}$	t_{WD}	See figure 4 3/ 4/		All	9, 10, 11	20		ns
Recover time between $\overline{WR}$	t_{RV}	See figure 4 3/ 4/ 8/		All	9, 10, 11	6 1/		t_{CY}
OTHER TIMINGS								
Clock period 9/	t_{CY}	See figure 4 3/ 4/ 10/ 11/		All	9, 10, 11	320	1350	ns
Clock high pulse width	t_{HO}	See figure 4 3/ 4/		All	9, 10, 11	140	t_{CY} – 90 12/	ns
Clock low pulse width	t_{LO}	See figure 4 3/ 4/		All	9, 10, 11	90		ns
TxD delay from falling edge of TxC	t_{DTX}	See figure 4 3/ 4/		All	9, 10, 11		1	µs
Transmitter input clock frequency	f_{TX}	1 x Baud rate	3/ 4/	All	9, 10, 11	1/ dc	64	kHz
		16 x Baud rate				1/ dc	310	
		64 x Baud rate				1/ dc	615	
Transmitter input clock pulse width	t_{TPW}	1 x Baud rate	See figure 4 3/ 4/	All	9, 10, 11	12		t_{CY}
		16 x Baud rate				1		
		64 x Baud rate				1		
Transmitter input clock pulse delay	t_{TPD}	1 x Baud rate	See figure 4 3/ 4/	All	9, 10, 11	15		t_{CY}
		16 x Baud rate				3		
		64 x Baud rate				3		
Receiver input clock frequency	f_{RX}	1 x Baud rate	3/ 4/	All	9, 10, 11	1/ dc	64	kHz
		16 x Baud rate				1/ dc	310	
		64 x Baud rate				1/ dc	615	
Receiver input clock pulse width	t_{RPW}	1 x Baud rate	See figure 4 3/ 4/	All	9, 10, 11	12		t_{CY}
		16 x Baud rate				1		
		64 x Baud rate				1		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5 V ±10% for device type 01 V_{CC} = 5 V ±5% for device type 02 unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
OTHER TIMINGS - Continued							
Receiver input clock pulse delay	t_{RPD}	1 x Baud rate; See figure 4 3/ 4/	All	9, 10, 11	15		t_{CY}
		16 x Baud rate			3		
		64 x Baud rate			3		
TxRDY delay from center of last bit	t_{TxRDY}	See figure 4 3/ 4/ 13/	01	9, 10, 11		12	t_{CY}
			02			14	
TxRDY fall from leading edge of $\overline{WR}$	$t_{TxRDY\ CLEAR}$	3/ 4/ 13/	All	9, 10, 11		400	ns
RxRDY delay from center of last bit	t_{RxRDY}	See figure 4 3/ 4/ 13/	All	9, 10, 11		26	t_{CY}
RxRDY fall from leading edge of $\overline{WR}$	$t_{RxRDY\ CLEAR}$	3/ 4/ 13/	All	9, 10, 11		400	ns
Internal SYNDET delay from rising edge of RxC	t_{IS}	See figure 4 3/ 4/ 13/	All	9, 10, 11		26	t_{CY}
External SYNDET setup after rising edge of RxC	t_{ES}	See figure 4 3/ 4/ 13/	All	9, 10, 11	16		t_{CY}
TxEMPTY delay from center of last bit	$t_{TXEMPTY}$	See figure 4 3/ 4/ 13/	All	9, 10, 11		20	t_{CY}
Control delay from rising edge of $\overline{WR}$	t_{WC}	See figure 4 3/ 4/ 13/	All	9, 10, 11		8	t_{CY}
Control to $\overline{RD}$ setup time	t_{CR}	3/ 4/ 13/	All	9, 10, 11	20		t_{CY}

1/ Guaranteed if not tested.
2/ I_{CC} is measured in a static condition with outputs in the worst condition with all outputs unloaded.
3/ Test conditions: V_{CC} = 5 V ±10% for device type 01. V_{CC} = 5 V ±5% for device type 02.
(See figure 4) V_{IL} = 0.45 V V_{IH} = 2.4 V
V_{OL} = 0.8 V V_{OH} = 2.0 V
4/ Clock rise and fall times are controlled by the test equipment. Measurement of typical generated signal are $t_R = t_F$ = 5 ns.
5/ Chip Select ($\overline{CS}$) and Command/Data (C/$\overline{D}$) are considered as addresses.
6/ Test condition: C_L = 100 pF (see figure 4).
7/ Assumes that address is valid before $\overline{RD}\downarrow$.
8/ This recovery time is for after a mode instruction only. Write data is allowed only when TxRDY = 1. Recovery time between writes for asynchronous mode is 8 t_{CY} and for synchronous mode is 16 t_{CY}.
9/ Due to test equipment limitations, actual tested values may differ from those specified but specified values are guaranteed.
10/ The TxC and RxC frequencies have the following limitations with respect to CLK: For 1 x Baud rate, f_{TX} or $f_{RX} \le 1/(30\ t_{CY})$. For 16 x and 64 x Baud rate, f_{TX} or $f_{RX} \le 1/(4.5\ t_{CY})$.
11/ Reset pulse width = 6 t_{CY} minimum; system clock must be running during reset.
12/ Limit may be guaranteed by indirect testing if not tested directly.
13/ Status update can have a maximum delay of 28 clock periods from the event affecting the status.

Device type	All		
Case outlines	X and 3		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D_2	15	TxRDY
2	D_3	16	SYNDET/BD
3	RxD	17	$\overline{CTS}$
4	GND	18	TxEMPTY
5	D_4	19	TxD
6	D_5	20	CLK
7	D_6	21	RESET
8	D_7	22	$\overline{DSR}$
9	$\overline{TxC}$	23	$\overline{RTS}$
10	$\overline{WR}$	24	$\overline{DTR}$
11	$\overline{CS}$	25	$\overline{RxC}$
12	$C/\overline{D}$	26	V_{CC}
13	$\overline{RD}$	27	D_0
14	RxRDY	28	D_1

FIGURE 1. Terminal connections.

READ/WRITE LOGIC FUNCTION

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	DEVICE DATA → DATA BUS
0	1	0	0	DATA BUS → DEVICE DATA
1	0	1	0	STATUS → DATA BUS
1	1	0	0	DATA BUS → CONTROL
X	1	1	0	DATA BUS → THREE-STATE
X	X	X	1	DATA BUS → THREE-STATE

FIGURE 2. Truth table.

Block diagram showing data bus buffer
and read/write logic functions

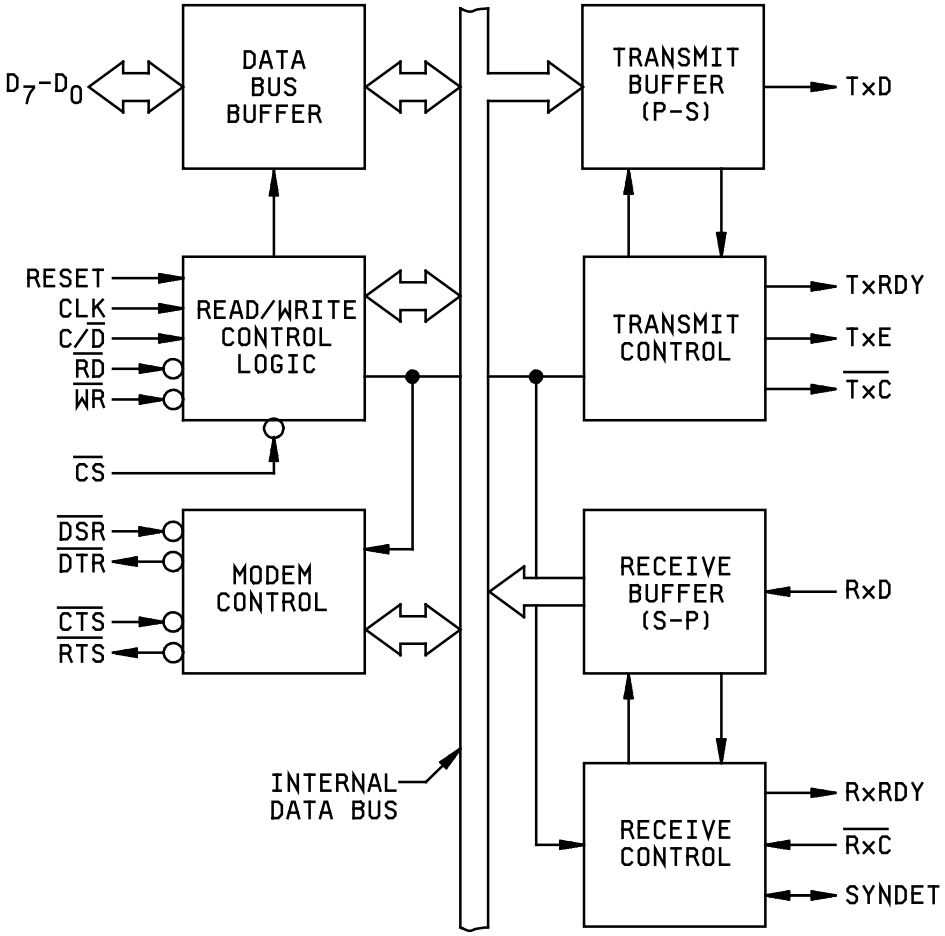


FIGURE 3. Block diagram.

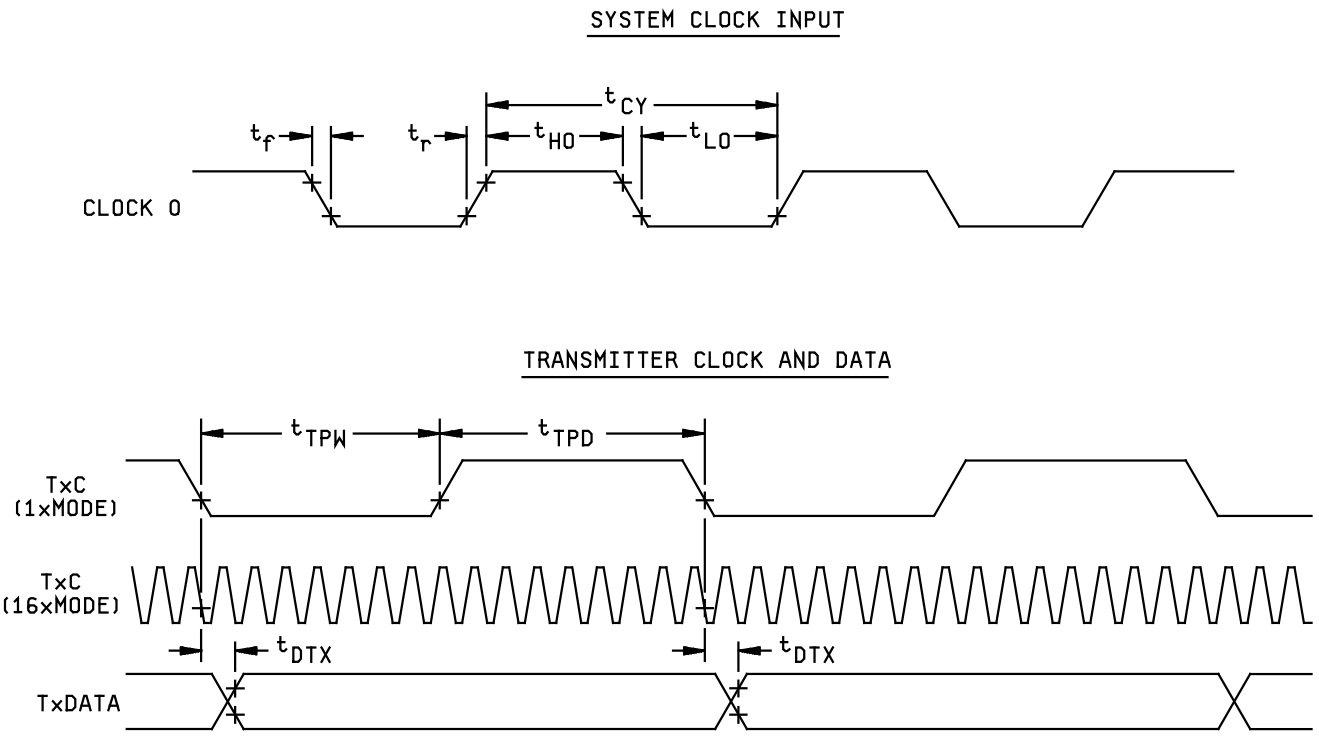


FIGURE 4. Switching waveforms and test circuit.

RECEIVER CLOCK AND DATA

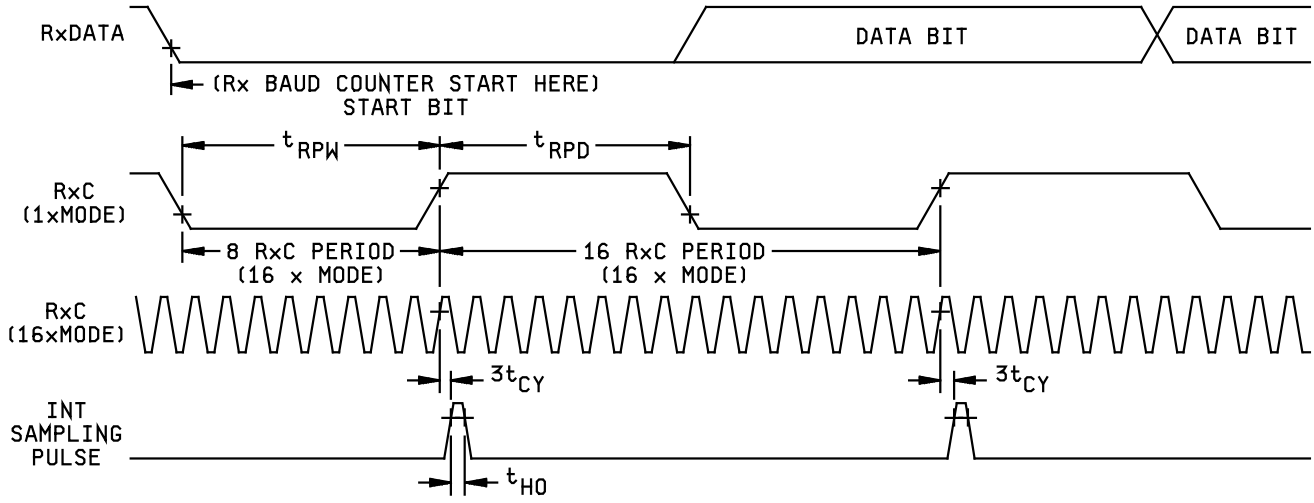


FIGURE 4. Switching waveforms and test circuit - Continued.

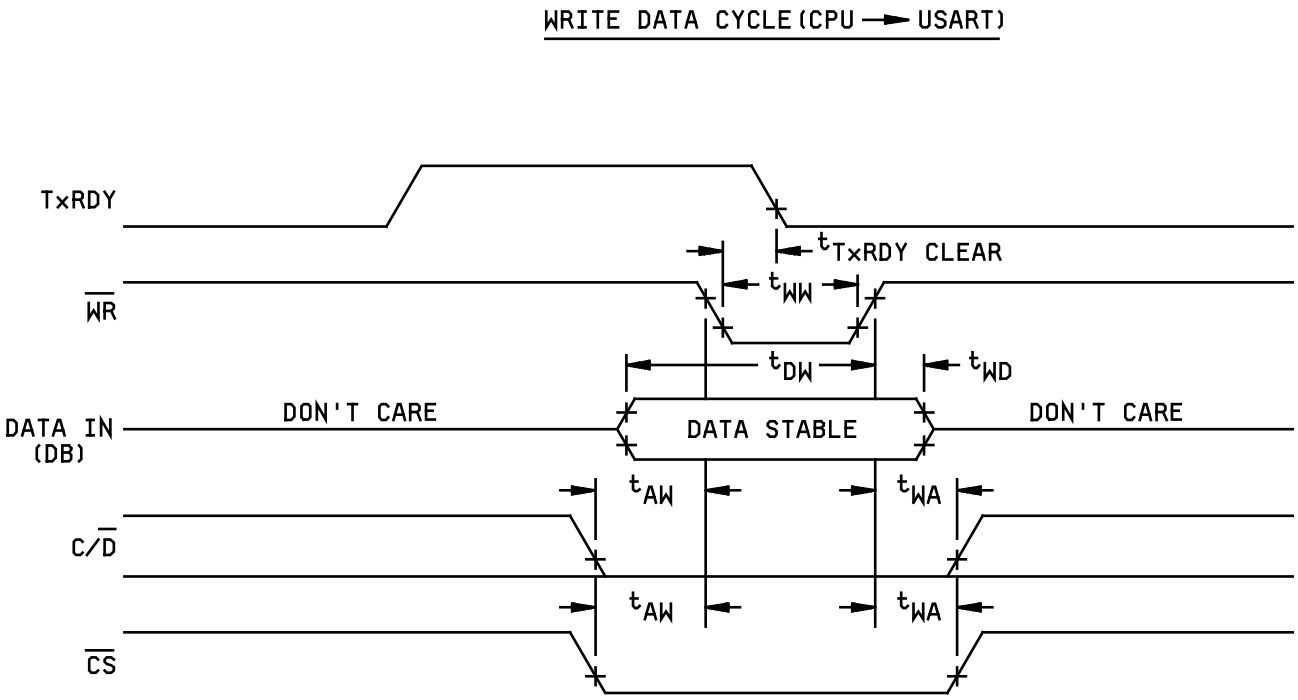


FIGURE 4. Switching waveforms and test circuit - Continued.

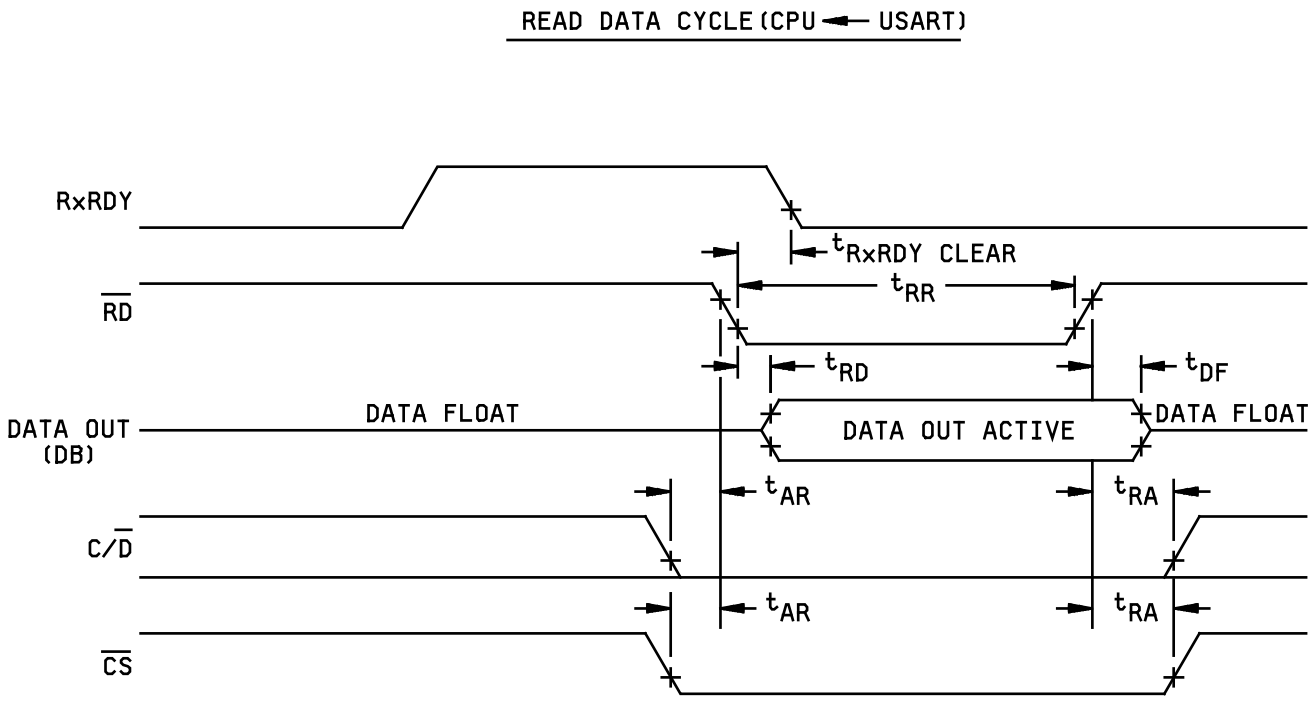


FIGURE 4. Switching waveforms and test circuit - Continued.

WRITE CONTROL OR OUTPUT PORT CYCLE (CPU → USART)

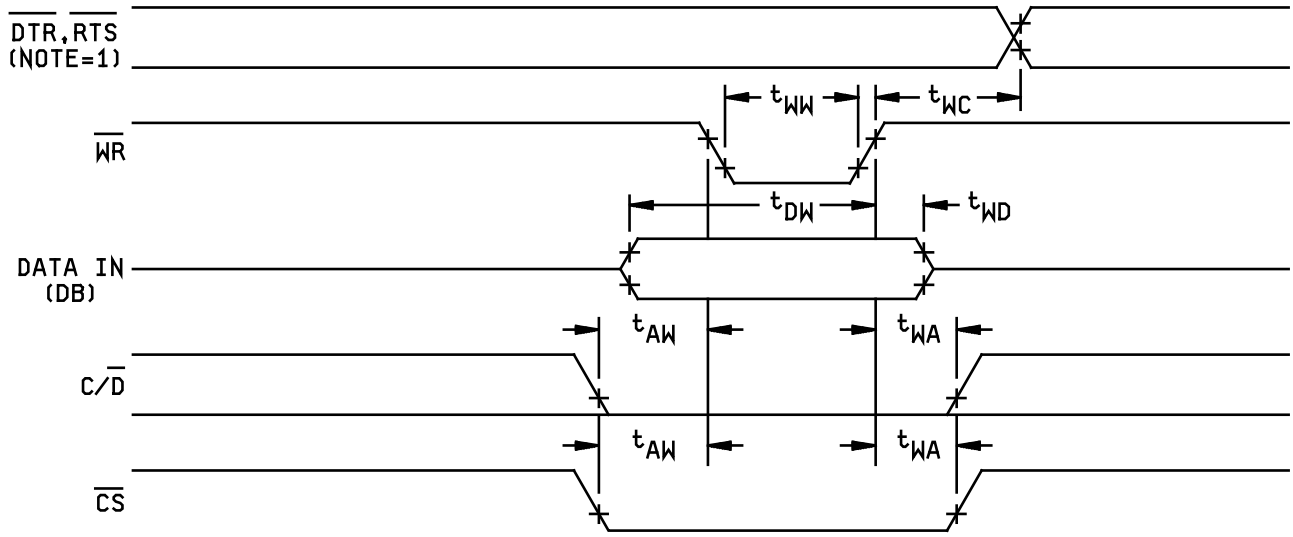
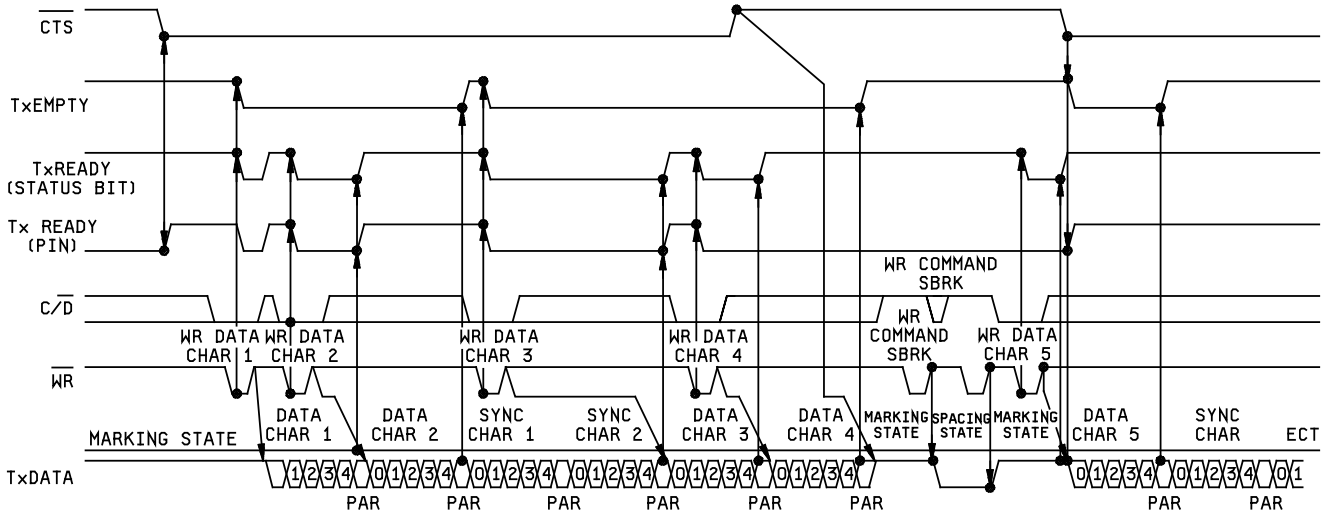


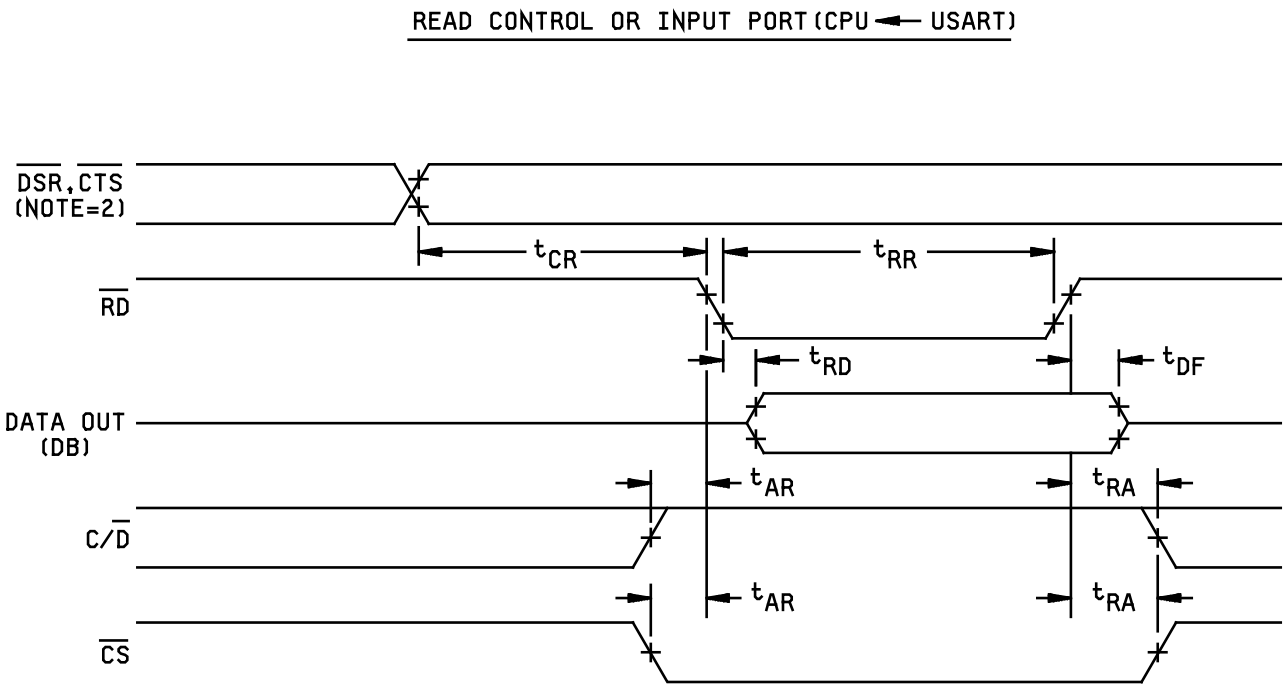
FIGURE 4. Switching waveforms and test circuit - Continued.

TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



EXAMPLE FORMAT - 5 BIT CHARACTER WITH PARITY 2 SYNC CHARACTER.

FIGURE 4. Switching waveforms and test circuit - Continued.



NOTES:
1. t_{WC} includes the response timing of a control byte.
2. t_{CR} includes the effect of CTS on the TxENBL circuitry.

FIGURE 4. Switching waveforms and test circuit - Continued.

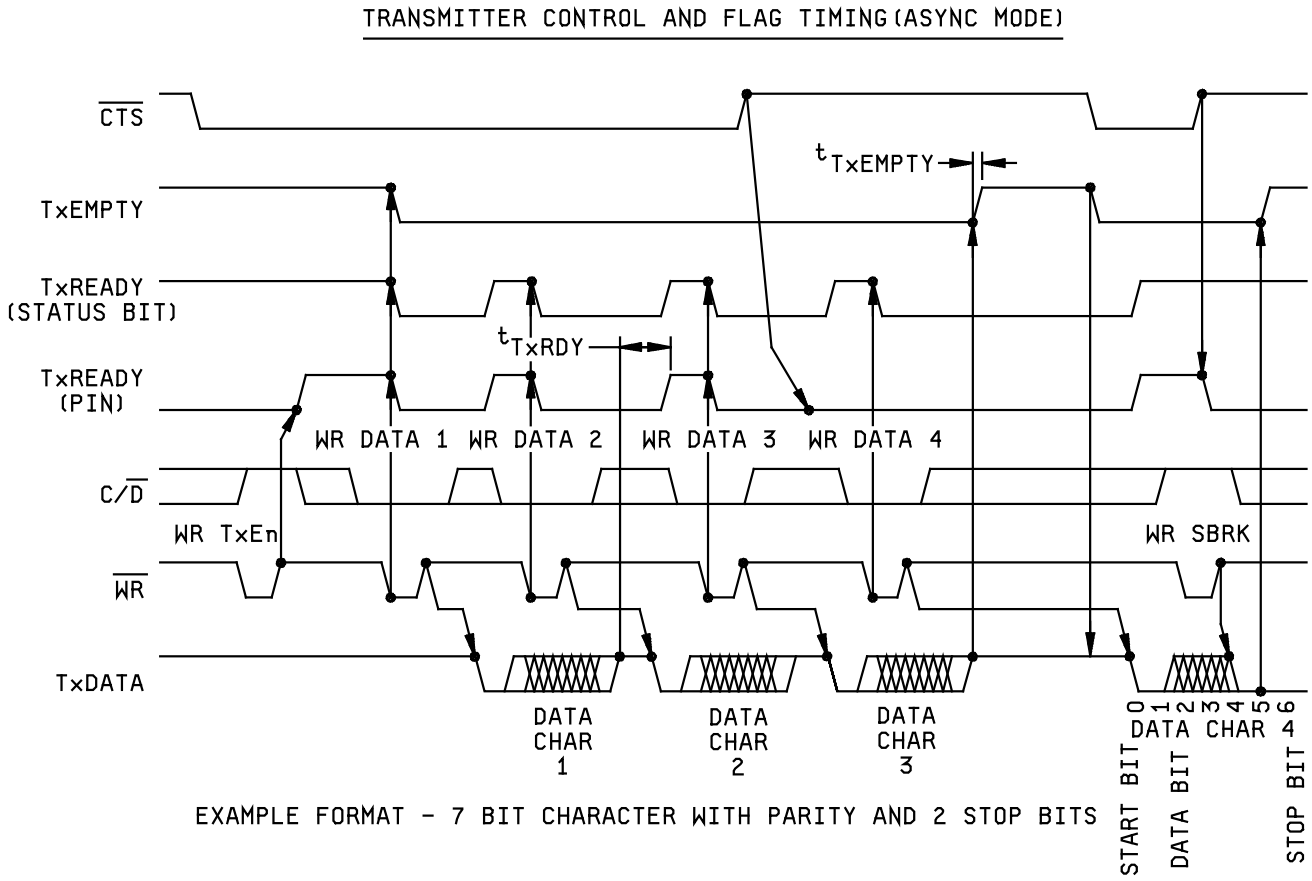


FIGURE 4. Switching waveforms and test circuit - Continued.

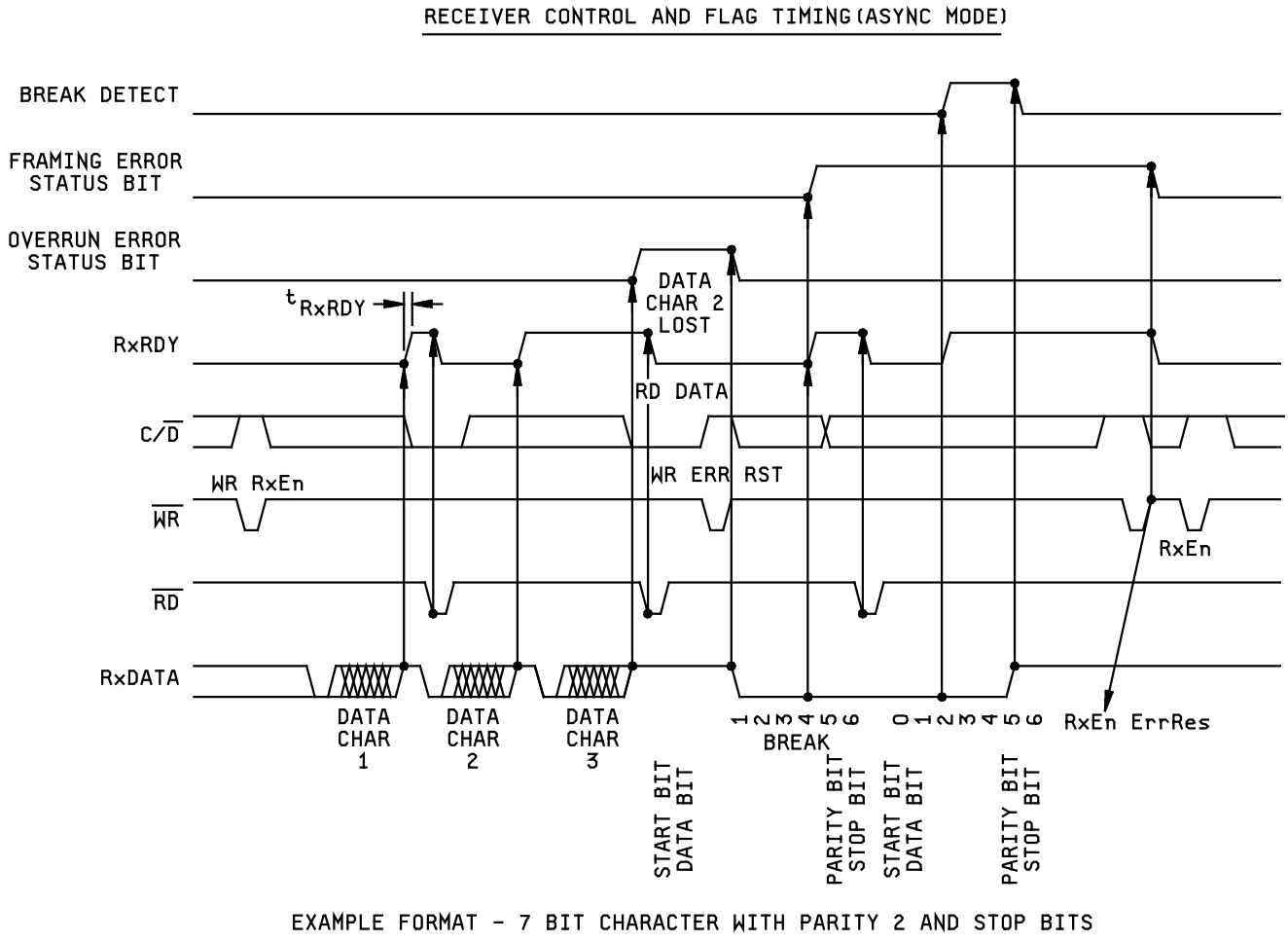
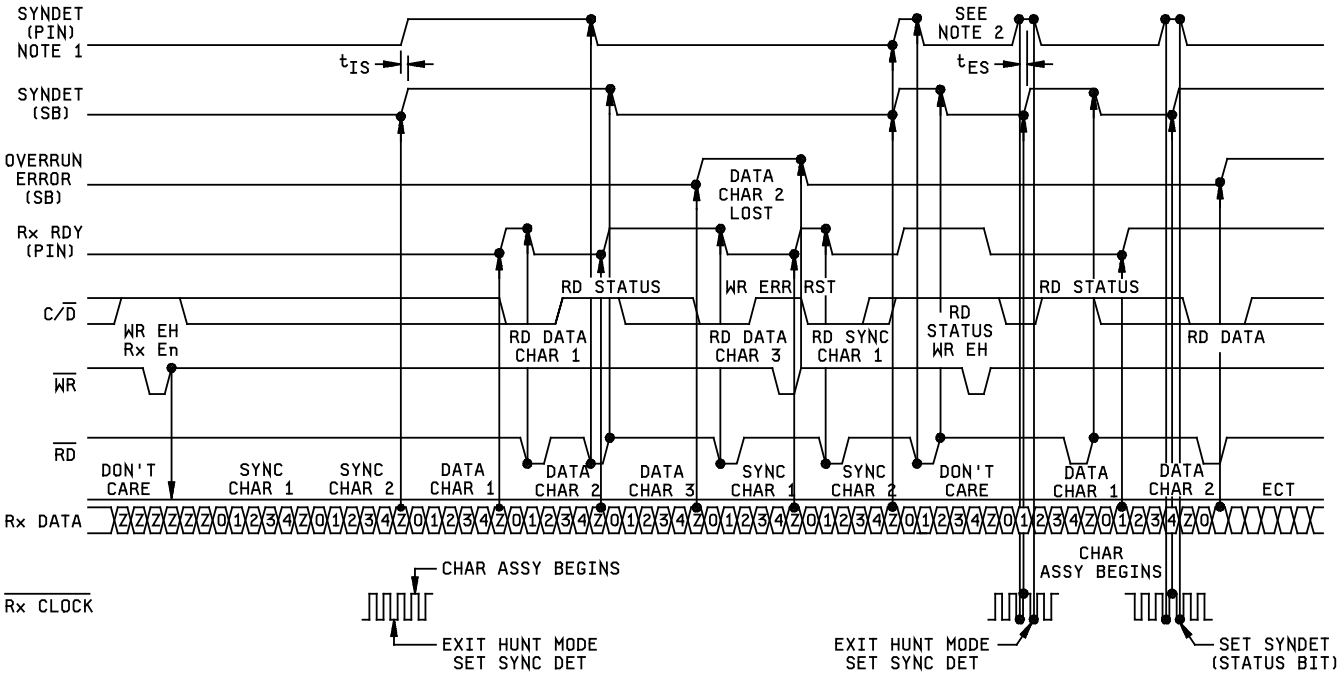


FIGURE 4. Switching waveforms and test circuit - Continued.

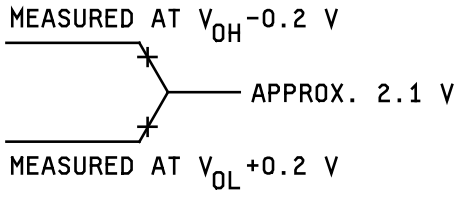
RECEIVER CONTROL AND FLAG TIMING(SYNC MODE)

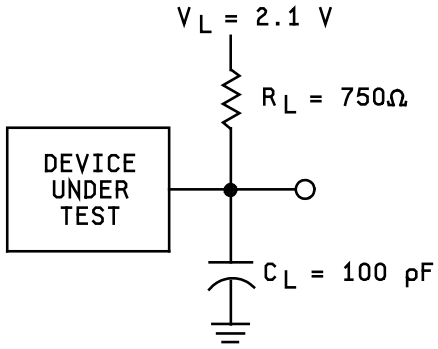


NOTES:
1. Internal sync, 2 sync characters, 5 bits with parity.
2. External sync, 5 bits with parity.

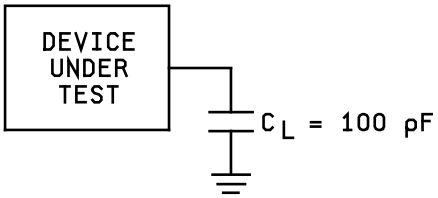
FIGURE 4. Switching waveforms and test circuit - Continued.

OUTPUT WAVEFORM AND TEST CIRCUIT FOR DATA FLOATING (t_{DF})

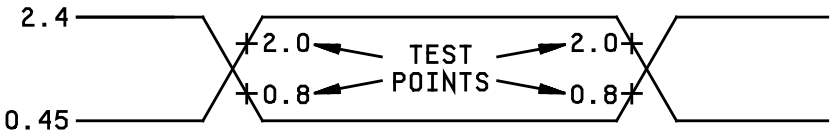




INPUT/OUTPUT WAVEFORM AND TEST CIRCUIT (EXCEPT DATA FLOATING (t_{DF})



INPUT/OUTPUT WAVEFORM



NOTES:
1. AC testing inputs are driven at 2.4 V for a logic “1” and 0.45 V for a logic “0”.
2. Timing measurements are made at 2.0 V for a logic “1” and 0.8 V for a logic “0”.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3 or 2, 8 (hot), 10
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

d. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured initially and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero failures shall be required.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-07-26

Approved sources of supply for SMD 5962-87548 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: https://landandmaritimeapps.dla.mil/programs/smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8754801XA	3/	8251A
5962-8754802XA	3V146	MD8251A/BXA
5962-87548023A	3V146	MR8251A/B3A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics 16 Malcolm Hoyt Drive Newburyport, MA 01950