MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PNP	NPN
MJ4030	MJ4033
MJ4031	MJ4034
MJ4032	MJ4035

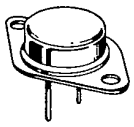
MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 3500 (Typ) @ I_C = 10 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor

16 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60–100 VOLTS
150 WATTS



MAXIMUM RATINGS

Rating	Symbol	MJ4030 MJ4033	MJ4031 MJ4034	MJ4032 MJ4035	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current	I_C	16			Adc
Base Current	I_B	0 5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

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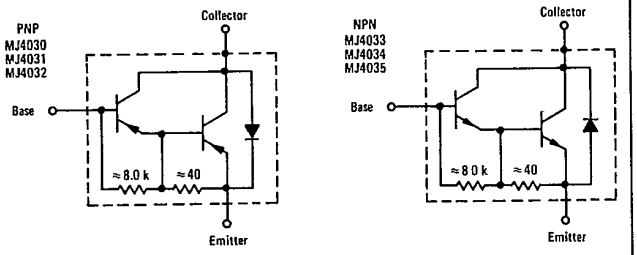
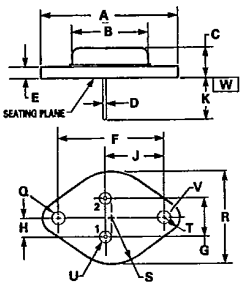
FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS
2. POSITIONAL TOLERANCE FOR HOLE Q: ⌖ | ϕ 0.25 (0.010) Ⓜ | W | V | Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⌖ | ϕ 0.30 (0.012) Ⓜ | W | V | Ⓜ | Q | Ⓜ

CASE 1-04
TO-204AA

T-33-33

PNP MJ4030, MJ4031, MJ4032
NPN MJ4033, MJ4034, MJ4035

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ4030, MJ4033	$V_{(BR)CEO}$	60	–	Vdc
	MJ4031, MJ4034		80	–	
	MJ4032, MJ4035		100	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ4030, MJ4033		–	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ4031, MJ4034		–	1.0	
(V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm)	MJ4032, MJ4035		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4030, MJ4033		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4031, MJ4034		–	5.0	
(V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4032, MJ4035		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
Collector-Emitter Leakage Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	MJ4030, MJ4033		–	3.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ4031, MJ4034		–	3.0	
(V_{CE} = 50 Vdc, I_B = 0)	MJ4032, MJ4035		–	3.0	
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 40 mAdc)			–	2.5	
(I_C = 16 Adc, I_B = 80 mAdc)			–	4.0	
Base-Emitter Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	3.0	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – DC CURRENT GAIN

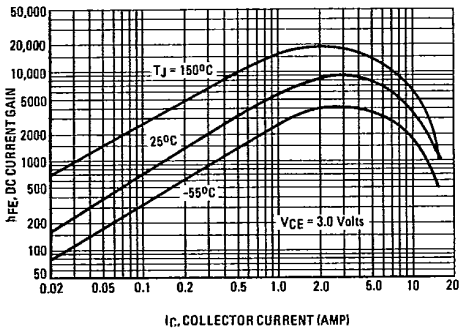


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

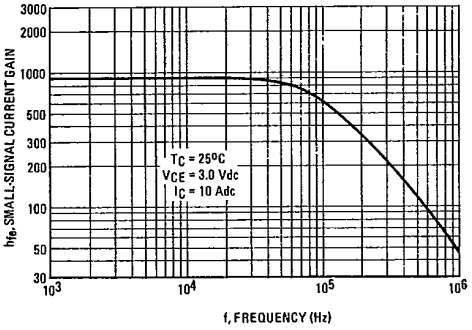


FIGURE 4 – "ON" VOLTAGES

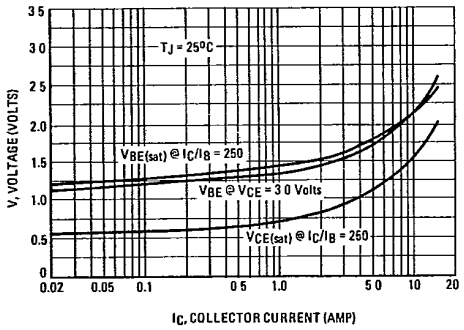
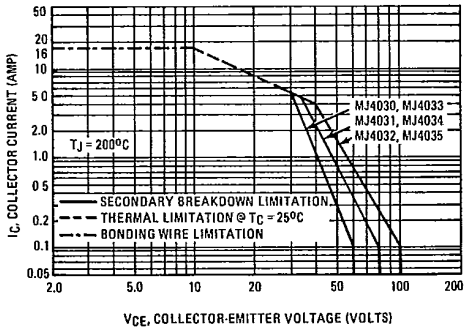


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.