FAIRCHILD
SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C908
Dual CMOS 30-Volt Relay Driver

General Description

The MM74C908 is a general purpose dual high voltage driver capable of sourcing a minimum of 250 mA at $V_{OUT} = V_{CC} - 3V$, and $T_J = 65°C$.

The MM74C908 consists of two CMOS NAND gates driving an emitter follower Darlington output to achieve high current drive and high voltage capabilities. In the "OFF" state the outputs can withstand a maximum of –30V across the device. These CMOS drivers are useful in interfacing normal CMOS voltage levels to driving relays, regulators, lamps, etc.

Features

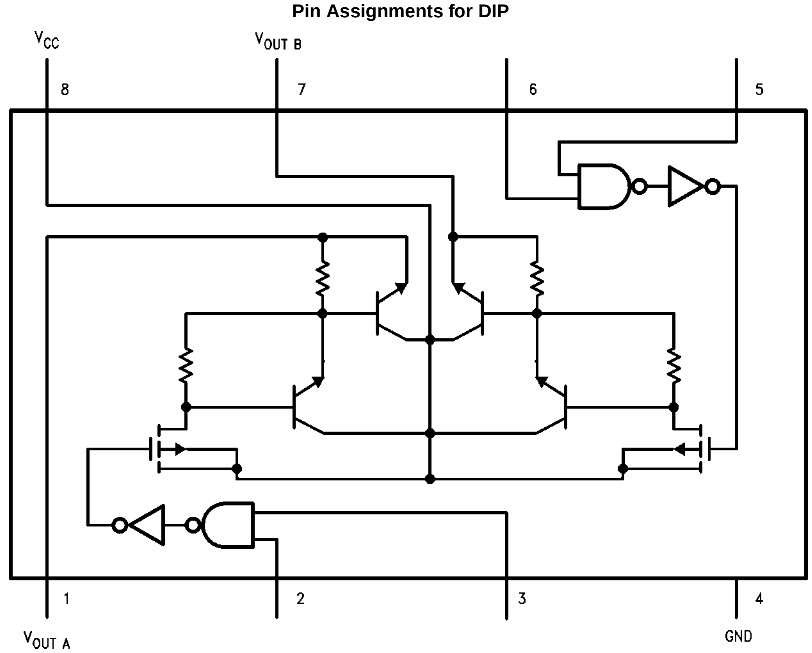
- Wide supply voltage range: 3V to 18V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low output "ON" resistance: 8Ω (typ.)
- High voltage: –30V
- High current: 250 mA

Ordering Code:

Order Number	Package Number	Package Description
MM74C908N	N08E	8-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

Pin Assignments for DIP



Top View

Absolute Maximum Ratings (Note 1)

Voltage at any Input Pin	–0.3V to V_{CC} +0.3V
Voltage at any Output Pin	32V
Operating Temperature Range	–40°C to +85°C
Operating V_{CC} Range	4V to 18V
Absolute Maximum V_{CC}	19V
I_{SOURCE}	500 mA
Storage Temperature	+150°C
Range (T_S)	–65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
Power Dissipation (P_D)	Refer to Maximum Power Dissipation vs Ambient Temperature Graph

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	–1.0	–0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V, Outputs Open Circuit		0.05	15	µA
	Output "OFF" Voltage	V_{IN} = V_{CC}, I_{OUT} = –200 µA		–30		V
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} – 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage	I_{OUT} = –300 mA, V_{CC} ≥ 5V, T_J = 25°C	V_{CC}–2.7	V_{CC}–1.8		V
		I_{OUT} = –250 mA, V_{CC} ≥ 5V, T_J = 65°C	V_{CC}–3.0	V_{CC}–1.9		V
		I_{OUT} = –175 mA, V_{CC} ≥ 5V, T_J = 150°C	V_{CC}–3.15	V_{CC}–2.0		V
R_{ON}	Output Resistance	I_{OUT} = –300 mA, V_{CC} ≥ 5V, T_J = 25°C		6.0	9.0	Ω
		I_{OUT} = –250 mA, V_{CC} ≥ 5V, T_J = 65°C		7.5	12	Ω
		I_{OUT} = –175 mA, V_{CC} ≥ 5V, T_J = 150°C		10	18	Ω
	Output Resistance Coefficient			0.55	0.80	%/°C
θ_{JA}	Thermal Resistance	(Note 2)		100	110	°C/W
	MM74C908	(Note 2)		45	55	°C/W

Note 2: θ_{JA} measured in free air with device soldered into printed circuit board.

AC Electrical Characteristics (Note 3)

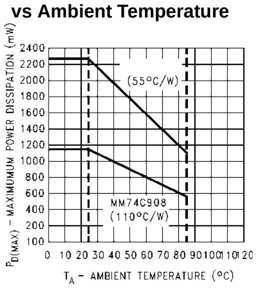
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logical "1"	V_{CC} = 5V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		150	300	ns
		V_{CC} = 10V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		65	120	ns
t_{pd0}	Propagation Delay to a Logic "0"	V_{CC} = 5V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		2.0	10	µs
		V_{CC} = 10V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		4.0	20	µs
C_{IN}	Input Capacitance	(Note 4)		5.0		pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

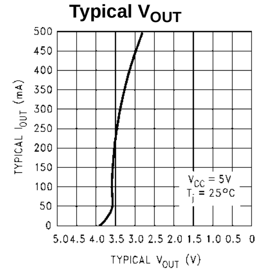
Note 4: Capacitance is guaranteed by periodic testing.

Typical Performance Characteristics

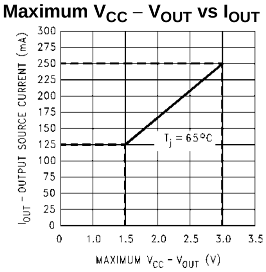
Maximum Power Dissipation vs Ambient Temperature



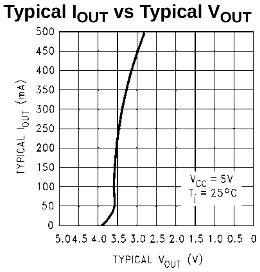
Typical I_{OUT} vs Typical V_{OUT}



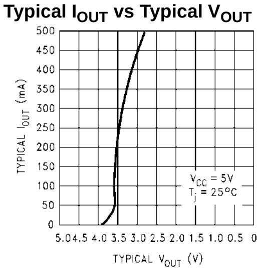
Maximum $V_{CC} - V_{OUT}$ vs I_{OUT}



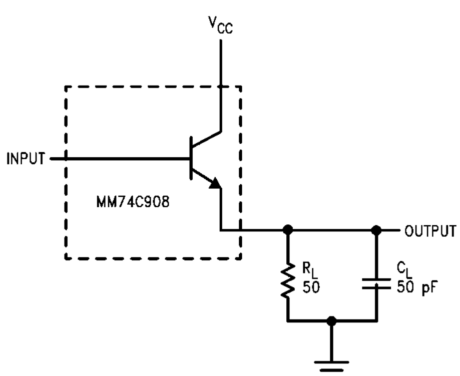
Typical I_{OUT} vs Typical V_{OUT}



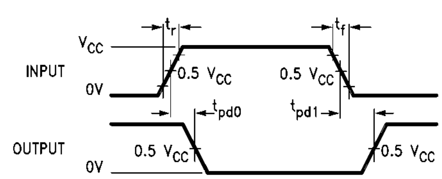
Typical I_{OUT} vs Typical V_{OUT}



AC Test Circuit



Switching Time Waveforms



$t_r = t_f = 20$ ns

Power Considerations

Calculating Output "ON" Resistance ($R_L > 18\Omega$)

The output "ON" resistance, R_{ON}, is a function of the junction temperature, T_J, and is given by:

$R_{ON} = 9\ (T_J - 25)\ (0.008) + 9$: (1)

and T_J is given by:

$T_J = T_A + P_{DAV}\ \theta_{JA}$,: (2)

where T_A = ambient temperature, θ_{JA} = thermal resistance, and P_{DAV} is the average power dissipated within the device. P_{DAV} consists of normal CMOS power terms (due to leakage currents, internal capacitance, switching, etc.) which are insignificant when compared to the power dissipated in the outputs. Thus, the output power term defines the allowable limits of operation and includes both outputs, A and B. P_D is given by:

$P_D = I_{OA}^2 R_{ON} + I_{OB}^2\ R_{ON}$, (3)

where I_O is the output current, given by:

$$I_O = \frac{V_{CC} - V_L}{R_{ON} + R_L}$$

(4)

V_L is the load voltage.

The average power dissipation, P_{DAV}, is a function of the duty cycle:

$P_{DAV} = I_{OA}^2 R_{ON}\ (\text{Duty Cycle}_A) +$ (5)

$I_{OB}^2\ R_{ON}(\text{Duty Cycle}_B)$

where the duty cycle is the % time in the current source state. Substituting equations (1) and (5) into (2) yields:

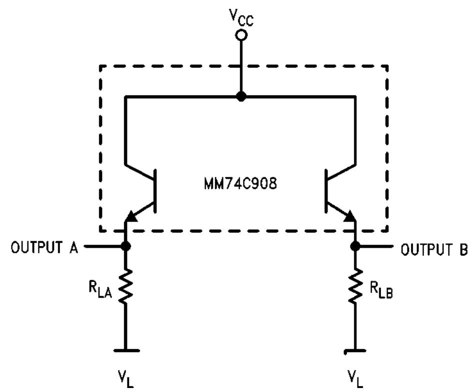
$T_J = T_A + \theta_{JA}\ [9\ (T_J - 25)\ (0.008) + 9]$: (6a)

$[I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]$

simplifying:

$$T_J = \frac{T_A + 7.2\ \theta_{JA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{JA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}$$

Equations (1), (4), and (6b) can be used in an iterative method to determine the output current, output resistance and junction temperature.



For example, let V_{CC} = 15V, $R_{LA} = 100\Omega$, $R_{LB} = 100\Omega$, V_L = 0V, T_A = 25°C, θ_{JA} = 110°C/W, Duty Cycle_A = 50%, Duty Cycle_B = 75%.

Assuming $R_{ON} = 11\Omega$, then:

$$I_{OA} = \frac{V_{CC} - V_L}{R_{ON} + R_{LA}} = \frac{15}{11 + 100} = 135.1\text{ mA},$$

$$I_{OB} = \frac{V_{CC} - V_L}{R_{ON} + R_{LB}} = 135.1\text{ mA}$$

and

$$T_J = \frac{T_A + 7.2\ \theta_{JA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{JA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}$$

$$T_J = \frac{25 + (7.2)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}{1 - (0.072)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}$$

T_J = 52.6°C

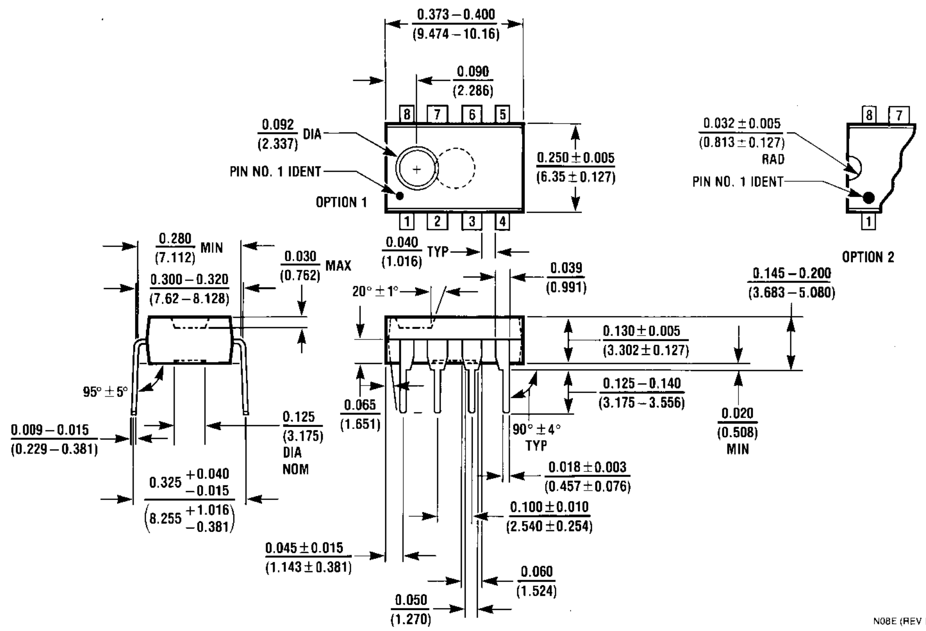
and $R_{ON} = 9\ (T_J - 25)\ (0.008) + 9$

$= 9(52.6 - 25)\ (0.008) + 9 = 11\Omega$

Applications

(See AN-177 for applications)

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N08E

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com