

MP75L43

Low Voltage CMOS Serial Input 12-Bit Digital-to-Analog Converter

FEATURES

- 3.3 V Operation
- 12-Bit DAC with Serial Digital Input Interface
- Full 4-Quadrant Multiplication
- Latch-Up Free
- Asynchronous CLEAR Input
- Serial Load On Positive or Negative Strobes
- Small Size
- Low Cost

BENEFITS

- Lower Assembly Costs
- Compatible with Serial Addressing Systems

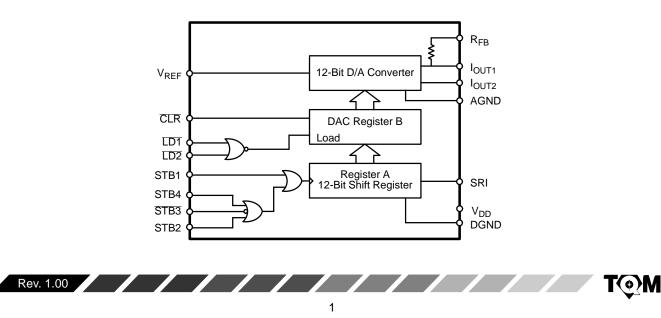
GENERAL DESCRIPTION

The MP75L43 is a precision, 12-bit CMOS 4-quadrant multiplying Digital-to-Analog Converter designed for serial interface applications.

The MP75L43 consists of two 12-bit registers, control logic and a 12-bit multiplying Digital-to-Analog Converter. The input register (register A) is a 12-bit serial-in parallel-out shift register. Serial data at the SRI pin is clocked into Register A on the leading or trailing edge (user selected) of the strobe input, with the MSB loaded first. Register B is a 12-bit parallel-in parallel-out register that follows register A. The contents of register A are loaded into register B under control of the Load inputs.

A CLEAR input is provided for the asynchronous resetting of register B to all 0's.

The MP75L43 is manufactured using an advanced thin film monolithic CMOS fabrication process. A unique decoding technique is utilized yielding excellent accuracy and stability. 12-bit linearity is achieved without laser trimming.



SIMPLIFIED BLOCK DIAGRAM

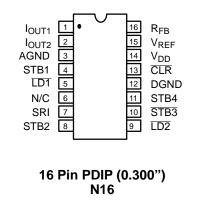


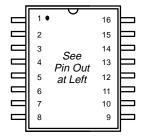
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP75L43JN	1	<u>+</u> 1	<u>+</u> 10
SOIC	–40 to +85°C	MP75L43JS	1	<u>+</u> 1	<u>+</u> 10

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions





16 Pin SOIC (Jedec, 0.300") S16

PIN OUT DEFINITIONS

NAME	DESCRIPTION	PIN NO.	NAME	DESCRIPTION
I _{OUT1}	DAC current output pin. Normally terminated at op amp virtual ground.	9	LD2	DAC Register B Load 2 input. When LD1 and LD2 go low the contents of
I _{OUT2}	DAC current output pin. Normally terminated at AGND.			Register A are loaded into DAC Register B.
AGND	Analog Ground.	10	STB3	Register A Strobe 3 input, See Table 1.
STB1	Register A Strobe 1 input, See Table 1.	11	STB4	Register A Strobe 4 input, See Table 1.
LD1	DAC Register B Load 1 input. When	12	DGND	Digital Ground.
LD1 and LD2 go low the contents of Register A are loaded into DAC Register B.		13	CLR	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000.
N/C	No Connection.	14	V _{DD}	Supply Input.
SRI	Serial Data Input to Register A.	15	V _{REF}	Reference input. Can be positive or
STB2	Register A Strobe 2 input, See Table 1.	16	R _{FB}	negative DC voltage or AC signal. DAC Feedback Resistor.
	I _{OUT1} I _{OUT2} AGND STB1 LD1 N/C SRI	IOUT1 DAC current output pin. Normally terminated at op amp virtual ground. IOUT2 DAC current output pin. Normally terminated at AGND. AGND Analog Ground. STB1 Register A Strobe 1 input, See Table 1. ID1 DAC Register B Load 1 input. When LD1 and LD2 go low the contents of Register B. N/C No Connection. SRI Serial Data Input to Register A.	IOUT1DAC current output pin. Normally terminated at op amp virtual ground.9IOUT2DAC current output pin. Normally terminated at AGND.10AGNDAnalog Ground.10STB1Register A Strobe 1 input, See Table 1.11ID1DAC Register B Load 1 input. When ID1 and ID2 go low the contents of Register B.13N/CNo Connection.14SRISerial Data Input to Register A.15STB2Register A Strobe 2 input, See Table 1.	IouT1DAC current output pin. Normally terminated at op amp virtual ground.9LD2IouT2DAC current output pin. Normally terminated at AGND.10STB3AGNDAnalog Ground.10STB3STB1Register A Strobe 1 input, See Table 1.11STB4LD1DAC Register B Load 1 input. When LD1 and LD2 go low the contents of Register B.12DGNDN/CNo Connection.14V_DDSRISerial Data Input to Register A.15V_REF

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ELECTRICAL CHARACTERISTICS

(V_{DD} = + 3 V, V_{REF} = +3 V unless otherwise noted)

			25°C		Tmin to	Tmax		
Parameter	Symbol	Min	Тур	Max	Min	Max	Units	Test Conditions/Comments
STATIC PERFORMANCE ¹								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity	INL						LSB	Best Fit Straight Line Spec.
(Relative Accuracy) J				<u>+</u> 1		<u>+</u> 1		(Max INL – Min INL) / 2
Differential Non-Linearity J	DNL			<u>+</u> 1		<u>+</u> 1	LSB	Monotonicity: 12 Bits Guaranteed
Gain Error J	GE			<u>+</u> 10		<u>+</u> 10	LSB	Using Internal R _{FB}
Gain Temperature Coefficient ²	TC _{GE}					<u>+</u> 2	ppm/°C	$\Delta Gain/\Delta Temperature$
Power Supply Rejection Ratio	PSRR			<u>+</u> 50		<u>+</u> 100	ppm/%	$ \Delta Gain/\Delta V_{DD} \Delta V_{DD} = \pm 5\%$
Output Leakage Current J	I _{OUT}			<u>+</u> 10		<u>+</u> 10	nA	
DYNAMIC PERFORMANCE								
Current Output Settling Time ²	t _S		2			2	μs	R _L =100Ω, C _L =13pF Full Scale Output Settles to 1/2 LSB of Final Value
AC Feedthrough at I _{OUT1} ²	F _T		2.5			2.5	mV p-p	$V_{REF} = 10$ kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R _{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS ³								
Logical "1" Voltage	V _{IH}	2.5			3.0		V	
Logical "0" Voltage Input Leakage Current	V _{IL} I _{LKG}			0.5 <u>+</u> 1		0.8 <u>+</u> 1	V μA	
ANALOG OUTPUTS ²								
Output Capacitance								
	C _{OUT1} C _{OUT1}			260 100		260 100	pF pF	DAC Inputs all 1's DAC Inputs all 0's
	C _{OUT2}			50		50	pF	DAC Inputs all 1's
	C _{OUT2}			210		210	pF	DAC Inputs all 0's
POWER SUPPLY								
Supply Voltage Supply Current	V _{DD} I _{DD}	3	3.3	3.6 100			V μA	All digital inputs = 0 V or all = 3 V





ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min Typ	Мах	Tmin to Tm Min M	nax lax	Units	Test Conditions/Comments
SWITCHING							
CHARACTERISTICS ^{2, 4}							
Serial Input to Strobe Set-up Time	t _{DS1}	50				ns	STB1 used as a strobe
Serial Input to Strobe Set-up Time	t _{DS4}	0				ns	STB4 used as a strobe
Serial Input to Strobe Set-up Time	t _{DS3}	0				ns	STB3 used as a strobe
Serial Input to Strobe Set-up Time	t _{DS2}	20				ns	STB2 used as a strobe
Serial Input to Strobe Hold Time	t _{DH1}	30				ns	STB1 used as a strobe
Serial Input to Strobe Hold Time	t _{DH4}	80				ns	STB4 used as a strobe
Serial Input to Strobe Hold Time	t _{DH3}	80				ns	STB3 used as a strobe
Serial Input to Strobe Hold Time	t _{DH2}	60				ns	STB2 used as a strobe
SRI Data Pulse Width	t _{SRI}	80				ns	
STB1 Pulse Width	t _{STB1}	80				ns	
STB4 Pulse Width	t _{STB4}	100				ns	
STB3 Pulse Width	t _{STB3}	100				ns	
STB2 Pulse Width	t _{STB2}	80				ns	
Load Pulse Width	^t LD1, 2	150				ns	
Minimum time between strobing	t _{ASB}	0				ns	
Reg. A and loading Reg. B							
CLR pulse width	t _{CLR}	200				ns	

NOTES:

¹ Full Scale Range (FSR) is 3 V for unipolar mode.

² Guaranteed but not production tested.

³ Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

⁴ See timing diagram.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2, 3}

V_{DD} to GND \ldots +5 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1} , I_{OUT2} to GND GND –0.5 to V_{DD} +0.5 V
V _{REF} to GND (2)
V _{RFB} to GND (2)
AGND to DGND
(Functionality Guaranteed <u>+</u> 0.5 V)

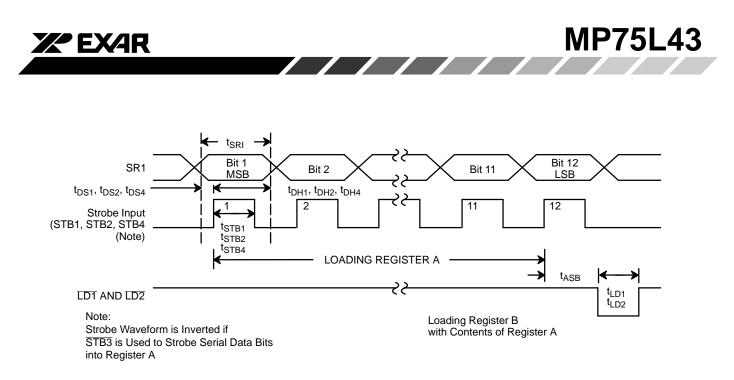
Storage Temperature65°C to +150°C
Lead Temperature (Soldering, 10 seconds) +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC 700mW
Derates above 75°C 10mW/°C

NOTES:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.
GND refers to AGND and DGND.

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MP75L43 Logic Inputs								
Register A Control Inputs Register B Control Inputs		MP75L43 Operation	Notes					
STB4	STB3	STB2	STB1	CLR	LD2	LD1		
0	1	0	~	х	Х	х	Data appearing at SRI strobed into Register A	2, 3
0	1	~	0	х	Х	Х	Data appearing at SRI strobed into Register A	2, 3
0	~	0	0	Х	Х	Х	Data appearing at SRI strobed into Register A	2, 3
Υ	1	0	0	Х	Х	Х	Data appearing at SRI strobed into Register A	
1	х	Х	Х					
Х	0	Х	Х				No Operation (Descriptor A)	3
Х	Х	1	Х				No Operation (Register A)	
Х	Х	Х	1					
				0	Х	Х	Clear Register B to code 0000 0000 0000 (Asynchronous)	1, 3
				1	1	Х	No Orientian (Devictor D)	3
				1	Х	1	No Operation (Register B)	
				1	0	0	Load Register B with the contents of Register A	3

NOTES

1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.

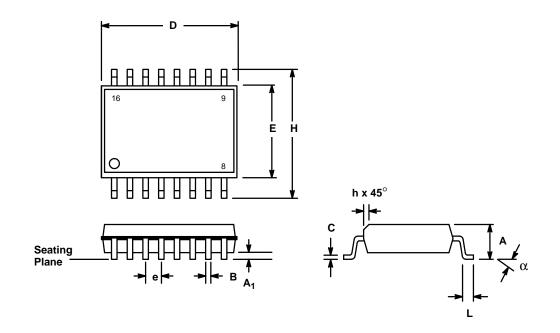
2. Serial data is loaded into Register A MSB first, on edges shown $\sqrt{-}$ is positive edge, $\sqrt{-}$ is negative edge. 3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table 1. Truth Table







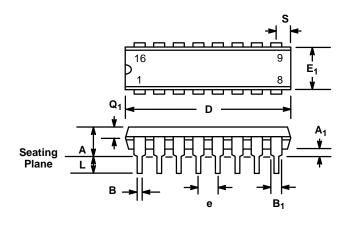


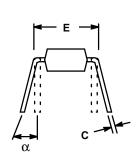
	INC	CHES	MILLIN	IETERS
SYMBOL	MIN	МАХ	MIN	MAX
А	0.097	0.104	2.46	2.64
A ₁	0.0050	0.0115	0.127	0.292
В	0.014	0.019	0.356	0.482
С	0.0091	0.0125	0.231	0.318
D	0.402	0.412	10.21	10.46
E	0.292	0.299	7.42	7.59
е	0.0	50 BSC	1.2	7 BSC
н	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°





16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP) N16





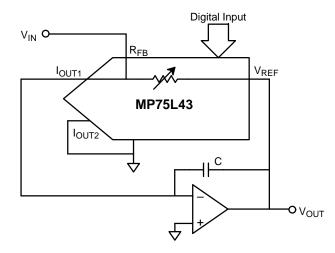
	INC	HES	MILLIN	IETERS
SYMBOL	MIN	MAX	MIN	МАХ
А		0.200		5.08
A ₁	0.015	—	0.38	_
В	0.014	0.023	0.356	0.584
B ₁ (1)	0.038	0.065	0.965	1.65
С	0.008	0.015	0.203	0.381
D	0.745	0.785	18.92	19.94
Е	0.295	0.325	7.49	8.26
E ₁	0.220	0.310	5.59	7.87
е	0.1	00 BSC	2.5	4 BSC
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q ₁	0.055	0.070	1.40	1.78
S	0.020	0.080	0.51	2.03

Note:	(1)	The minimum limit for dimensions B1 may be 0.023"
		(0.58 mm) for all four corner leads only.





APPLICATION NOTES Refer to Section 8 for Applications Information



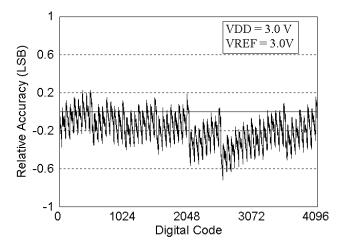


Figure 2. Digitally Programmable Gain Amplifier

Graph 1. Relative Accuracy vs. Digital Code

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