MP75L43

Low Voltage CMOS
Serial Input 12-Bit
Digital-to-Analog Converter

FEATURES

- **3.3 V Operation**
- **12-Bit DAC with Serial Digital Input Interface**
- **Full 4-Quadrant Multiplication**
- **Latch-Up Free**
- **Asynchronous CLEAR Input**
- **Serial Load On Positive or Negative Strobes**
- **Small Size**
- **Low Cost**

BENEFITS

- **Lower Assembly Costs**
- **Compatible with Serial Addressing Systems**

GENERAL DESCRIPTION

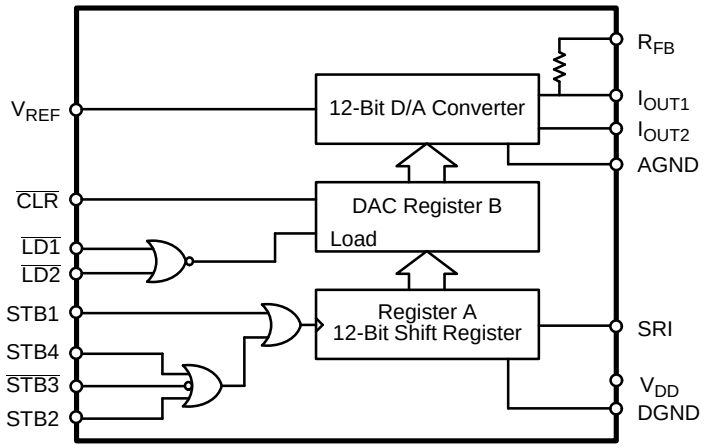
The MP75L43 is a precision, 12-bit CMOS 4-quadrant multiplying Digital-to-Analog Converter designed for serial interface applications.

The MP75L43 consists of two 12-bit registers, control logic and a 12-bit multiplying Digital-to-Analog Converter. The input register (register A) is a 12-bit serial-in parallel-out shift register. Serial data at the SRI pin is clocked into Register A on the leading or trailing edge (user selected) of the strobe input, with the MSB loaded first. Register B is a 12-bit parallel-in parallel-out register that follows register A. The contents of register A are loaded into register B under control of the Load inputs.

A CLEAR input is provided for the asynchronous resetting of register B to all 0's.

The MP75L43 is manufactured using an advanced thin film monolithic CMOS fabrication process. A unique decoding technique is utilized yielding excellent accuracy and stability. 12-bit linearity is achieved without laser trimming.

SIMPLIFIED BLOCK DIAGRAM

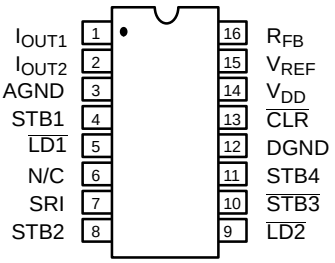


ORDERING INFORMATION

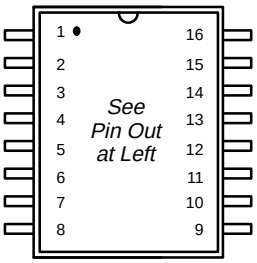
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP75L43JN	1	±1	±10
SOIC	–40 to +85°C	MP75L43JS	1	±1	±10

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



16 Pin PDIP (0.300")
N16



16 Pin SOIC (Jedec, 0.300")
S16

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	DAC current output pin. Normally terminated at op amp virtual ground.
2	I_{OUT2}	DAC current output pin. Normally terminated at AGND.
3	AGND	Analog Ground.
4	STB1	Register A Strobe 1 input, *See Table 1.*
5	$\overline{LD1}$	DAC Register B Load 1 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B.
6	N/C	No Connection.
7	SRI	Serial Data Input to Register A.
8	STB2	Register A Strobe 2 input, *See Table 1.*

PIN NO.	NAME	DESCRIPTION
9	$\overline{LD2}$	DAC Register B Load 2 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B.
10	$\overline{STB3}$	Register A Strobe 3 input, *See Table 1.*
11	STB4	Register A Strobe 4 input, *See Table 1.*
12	DGND	Digital Ground.
13	$\overline{CLR}$	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000.
14	V_{DD}	Supply Input.
15	V_{REF}	Reference input. Can be positive or negative DC voltage or AC signal.
16	R_{FB}	DAC Feedback Resistor.

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 3 V, V_{REF} = +3 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J				±1		±1		
Differential Non-Linearity	DNL						LSB	Monotonicity:
J				±1		±1		12 Bits Guaranteed
Gain Error	GE						LSB	Using Internal R_{FB}
J				±10		±10		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
J				±10		±10		
DYNAMIC PERFORMANCE								
Current Output Settling Time[2]	t_S		2			2	µs	R_L=100Ω, C_L=13pF Full Scale Output Settles to 1/2 LSB of Final Value
AC Feedthrough at I_{OUT1}[2]	F_T		2.5			2.5	mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical “1” Voltage	V_{IH}	2.5			3.0		V	
Logical “0” Voltage	V_{IL}			0.5		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}			260		260	pF	DAC Inputs all 1’s
	C_{OUT1}			100		100	pF	DAC Inputs all 0’s
	C_{OUT2}			50		50	pF	DAC Inputs all 1’s
	C_{OUT2}			210		210	pF	DAC Inputs all 0’s
POWER SUPPLY								
Supply Voltage	V_{DD}	3	3.3	3.6			V	
Supply Current	I_{DD}			100			µA	All digital inputs = 0 V or all = 3 V

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Serial Input to Strobe Set-up Time	t_{DS1}		50				ns	STB1 used as a strobe
Serial Input to Strobe Set-up Time	t_{DS4}		0				ns	STB4 used as a strobe
Serial Input to Strobe Set-up Time	t_{DS3}		0				ns	$\overline{STB3}$ used as a strobe
Serial Input to Strobe Set-up Time	t_{DS2}		20				ns	STB2 used as a strobe
Serial Input to Strobe Hold Time	t_{DH1}		30				ns	STB1 used as a strobe
Serial Input to Strobe Hold Time	t_{DH4}		80				ns	STB4 used as a strobe
Serial Input to Strobe Hold Time	t_{DH3}		80				ns	$\overline{STB3}$ used as a strobe
Serial Input to Strobe Hold Time	t_{DH2}		60				ns	STB2 used as a strobe
SRI Data Pulse Width	t_{SRI}		80				ns	
STB1 Pulse Width	t_{STB1}		80				ns	
STB4 Pulse Width	t_{STB4}		100				ns	
$\overline{STB3}$ Pulse Width	t_{STB3}		100				ns	
STB2 Pulse Width	t_{STB2}		80				ns	
Load Pulse Width	$t_{LD1, 2}$		150				ns	
Minimum time between strobing Reg. A and loading Reg. B	t_{ASB}		0				ns	
$\overline{CLR}$ pulse width	t_{CLR}		200				ns	

NOTES:

1 Full Scale Range (FSR) is 3 V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND . . . . . +5 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND . . . . . GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) . . . . . ±25 V
V_{RFB} to GND (2) . . . . . ±25 V
AGND to DGND . . . . . ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature . . . . . –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

Package Power Dissipation Rating to 75°C
PDIP, SOIC 700mW
Derates above 75°C . . . . . 10mW/°C

NOTES:
1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

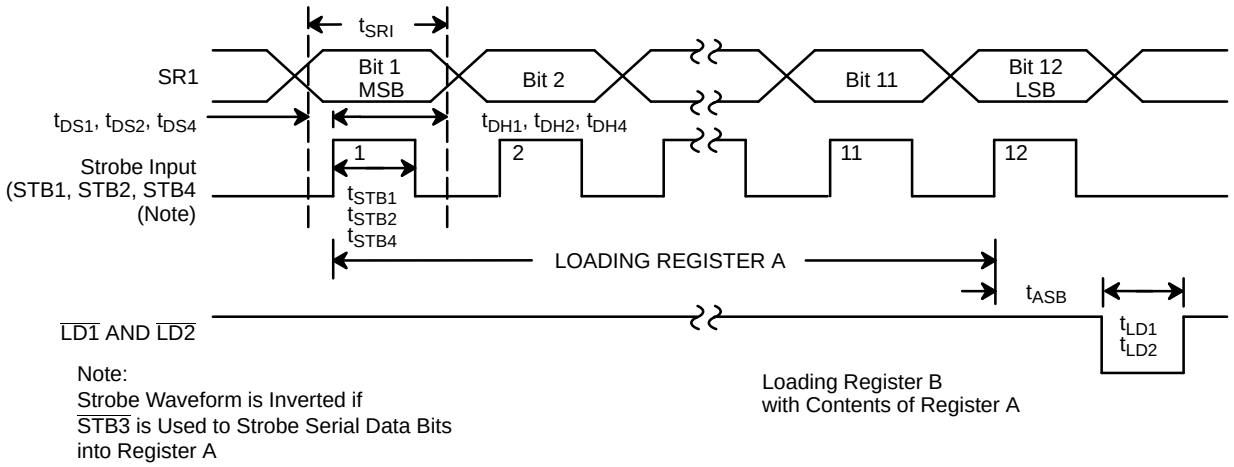


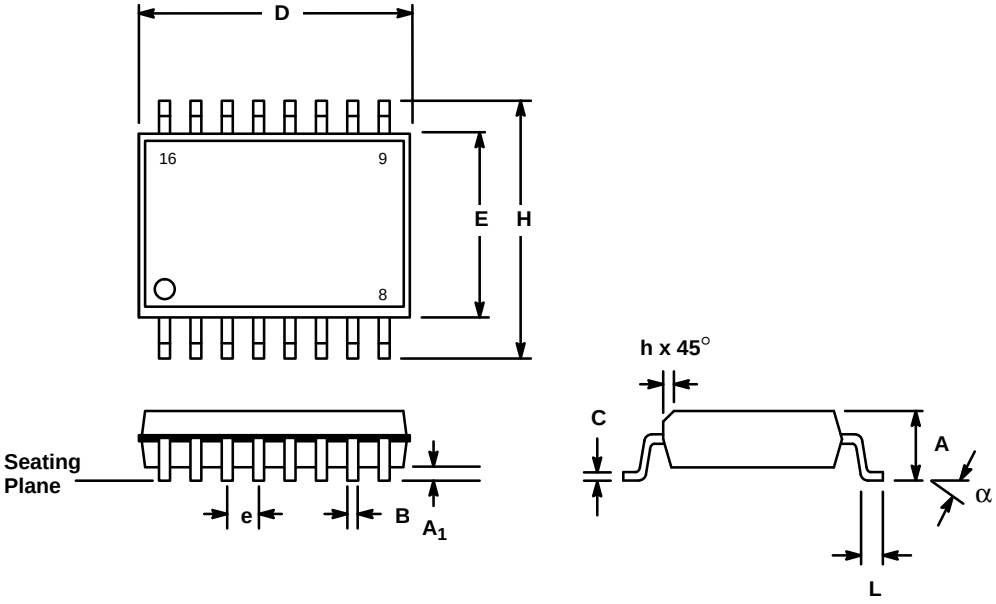
Figure 1. Timing Diagram

MP75L43 Logic Inputs							MP75L43 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↑	X	X	X	Data appearing at SRI strobed into Register A	2, 3
0	1	↑	0	X	X	X	Data appearing at SRI strobed into Register A	2, 3
0	↓	0	0	X	X	X	Data appearing at SRI strobed into Register A	2, 3
↑	1	0	0	X	X	X	Data appearing at SRI strobed into Register A	2, 3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B to code 0000 0000 0000 (Asynchronous)	1, 3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B with the contents of Register A	3

NOTES
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↑ is positive edge, ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

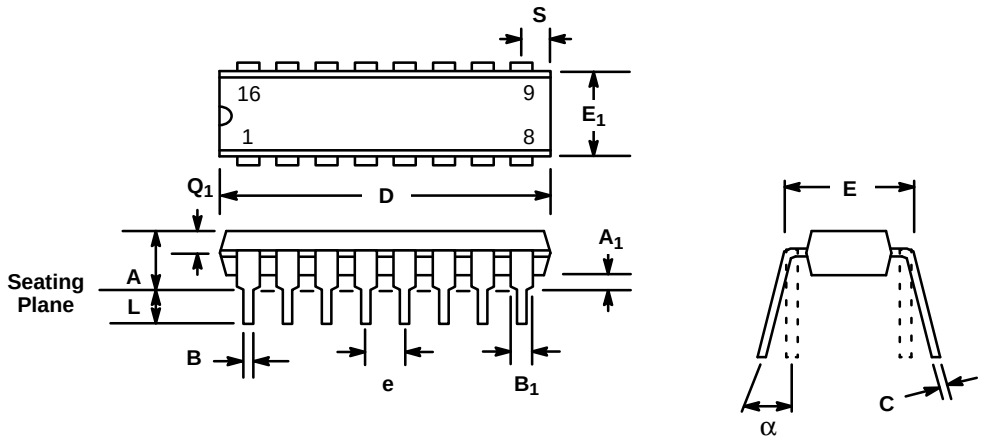
Table 1. Truth Table

16 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S16



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.46	2.64
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.482
C	0.0091	0.0125	0.231	0.318
D	0.402	0.412	10.21	10.46
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

16 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N16



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.745	0.785	18.92	19.94
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.080	0.51	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023” (0.58 mm) for all four corner leads only.

APPLICATION NOTES

Refer to Section 8 for Applications Information

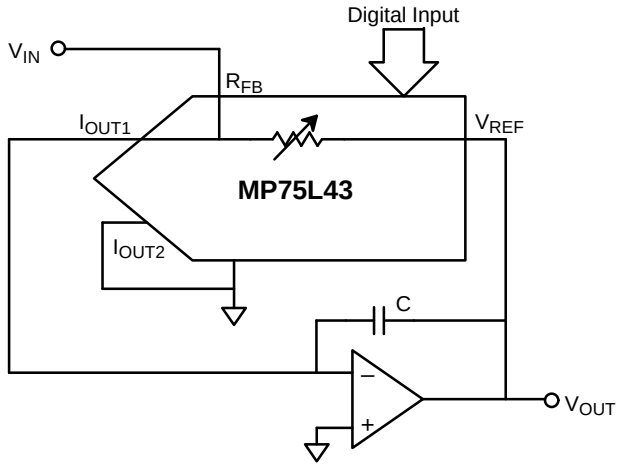
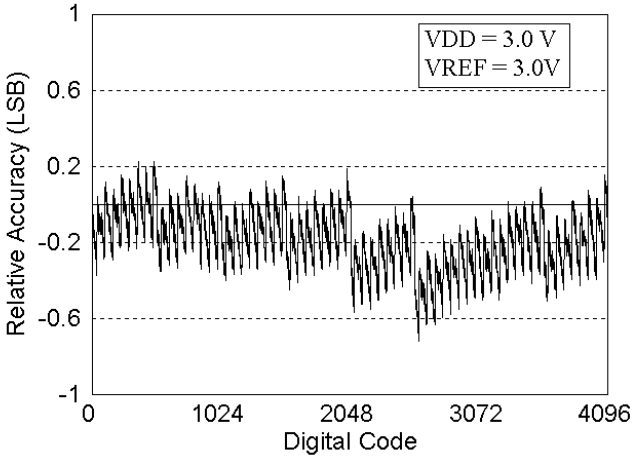


Figure 2. Digitally Programmable Gain Amplifier



Graph 1. Relative Accuracy vs. Digital Code