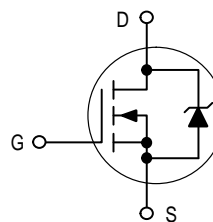


*Designer's™ Data Sheet*  
**TMOS E-FET™**  
**Power Field Effect Transistor**  
**N-Channel Enhancement-Mode Silicon Gate**

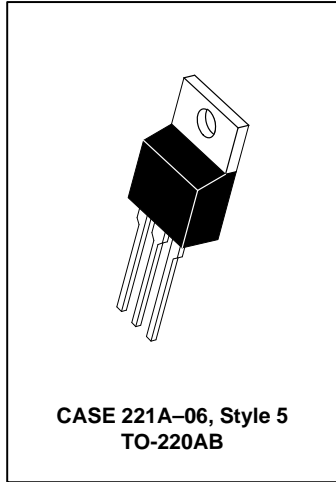
This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters, PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature



**MTP8N50E**

**TMOS POWER FET**  
**8.0 AMPERES**  
**500 VOLTS**  
 **$R_{DS(on)} = 0.8 \text{ OHM}$**



**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	500	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	500	Vdc
Gate-to-Source Voltage – Continuous – Non-repetitive ( $t_p \leq 10 \text{ ms}$ )	$V_{GS}$ $V_{GSM}$	$\pm 20$ $\pm 40$	Vdc Vpk
Drain Current — Continuous @ $T_C = 25^\circ\text{C}$ — Continuous @ $T_C = 100^\circ\text{C}$ — Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_D$ $I_D$ $I_{DM}$	8.0 5.0 32	Adc Adc Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	125 1.0	Watts W/°C
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy – STARTING $T_J = 25^\circ\text{C}$ ( $V_{DD} = 25 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , PEAK $I_L = 8.0 \text{ Apk}$ , $L = 16 \text{ mH}$ , $R_G = 25 \Omega$ )	EAS	510	mJ
Thermal Resistance – Junction-to-Case – Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 sec.	$T_L$	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

E-FET and Designer's are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

# MTP8N50E

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	500 —	— 500	— —	Vdc mV/°C	
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 500 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 400 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	— —	— —	250 1000	μAdc	
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	—	—	100	nAdc	
<b>ON CHARACTERISTICS (1)</b>						
Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0 —	2.8 6.3	4.0 —	Vdc mV/°C	
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 4.0 Adc)	R <sub>DS(on)</sub>	—	0.6	0.8	Ohms	
Drain-to-Source On-Voltage (V <sub>GS</sub> = 10 Vdc) (I <sub>D</sub> = 8.0 Adc) (I <sub>D</sub> = 4.0 Adc, T <sub>J</sub> = 125°C)	V <sub>DS(on)</sub>	— —	5.0 —	7.2 6.4	Vdc	
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 4.0 Adc)	g <sub>FS</sub>	4.0	—	—	mhos	
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	1450	1680	pF
Output Capacitance		C <sub>oss</sub>	—	190	246	
Transfer Capacitance		C <sub>rss</sub>	—	45.4	144	
<b>SWITCHING CHARACTERISTICS (2)</b>						
Turn-On Delay Time	(R <sub>go</sub> + C17n = 9.1 Ω)	t <sub>d(on)</sub>	—	15	50	ns
Rise Time		t <sub>r</sub>	—	33	72	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	40	150	
Fall Time		t <sub>f</sub>	—	32	60	
Gate Charge (see Figure 8)	(V <sub>DS</sub> = 400 Vdc, I <sub>D</sub> = 8.0 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>T</sub>	—	40	64	nC
		Q <sub>1</sub>	—	8.0	—	
		Q <sub>2</sub>	—	17	—	
		Q <sub>3</sub>	—	17.3	—	
<b>SOURCE-DRAIN DIODE CHARACTERISTICS</b>						
Forward On-Voltage (I <sub>S</sub> = 8.0 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 8.0 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	— —	1.2 1.1	2.0 —	Vdc	
Reverse Recovery Time	(I <sub>S</sub> = 8.0 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	320	—	ns
		t <sub>a</sub>	—	179	—	
		t <sub>b</sub>	—	141	—	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	—	3.0	—	μC
<b>INTERNAL PACKAGE INDUCTANCE</b>						
Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)	L <sub>D</sub>	—	4.5	—	nH	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>S</sub>	—	7.5	—		

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

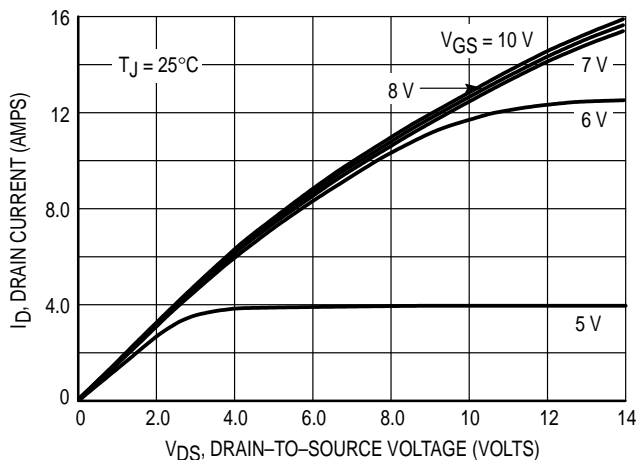


Figure 1. On-Region Characteristics

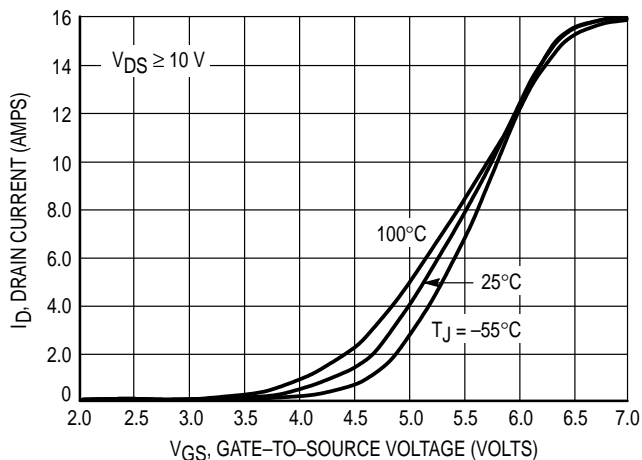


Figure 2. Transfer Characteristics

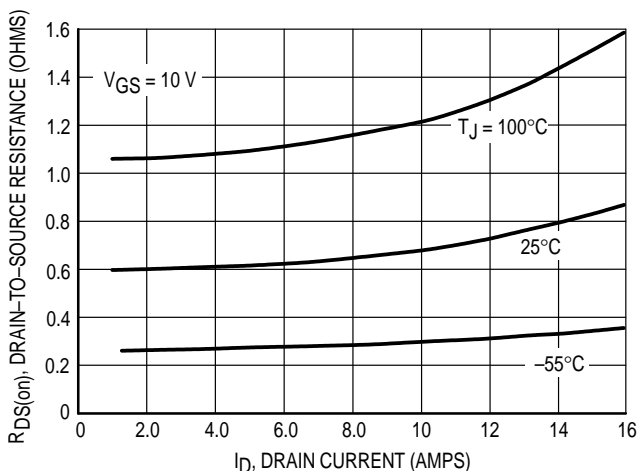


Figure 3. On-Resistance versus Drain Current and Temperature

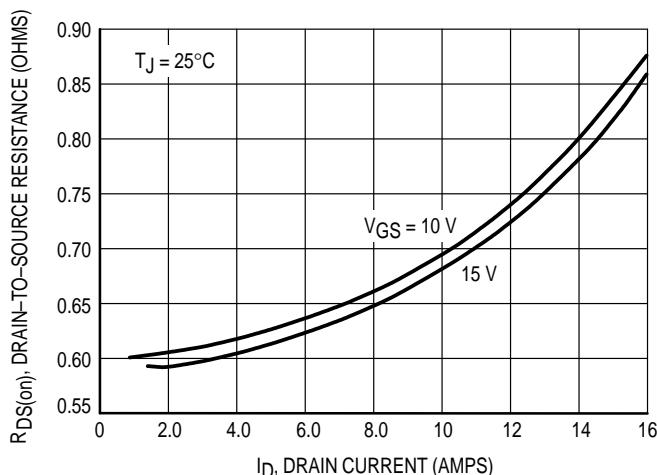


Figure 4. On-Resistance versus Drain Current and Gate Voltage

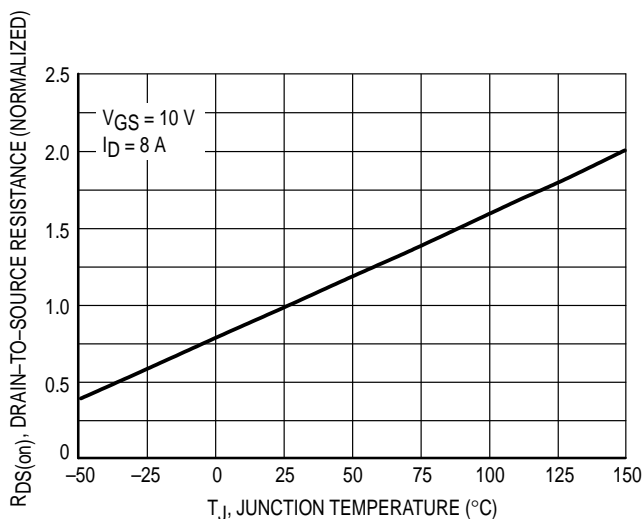


Figure 5. On-Resistance Variation with Temperature

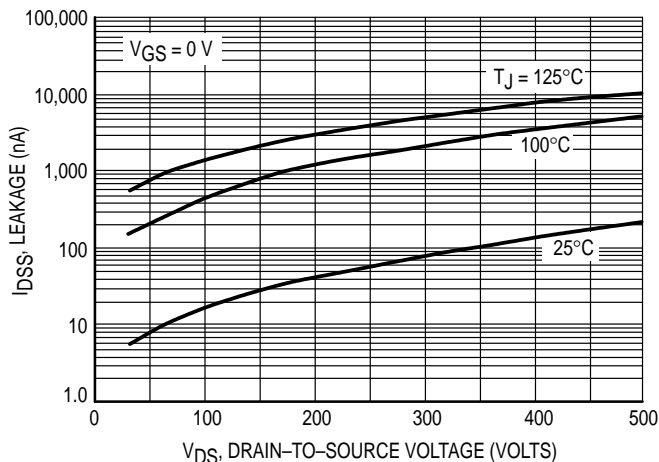


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

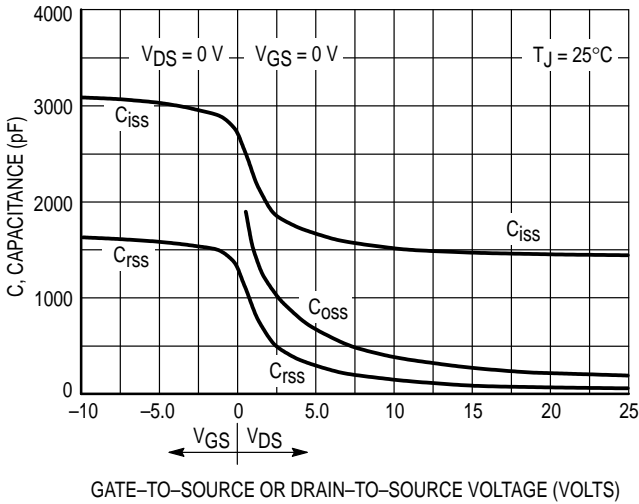


Figure 7. Capacitance Variation

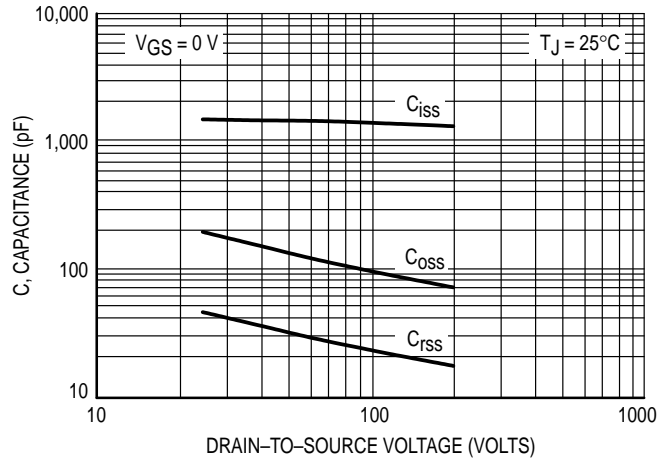


Figure 8. High Voltage Capacitance Variation

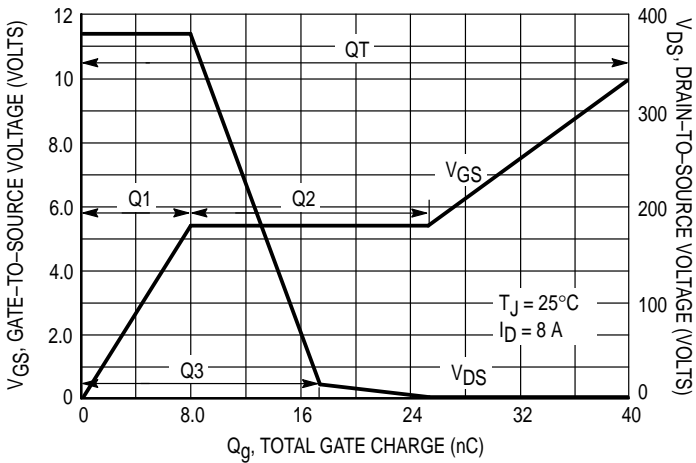


Figure 9. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

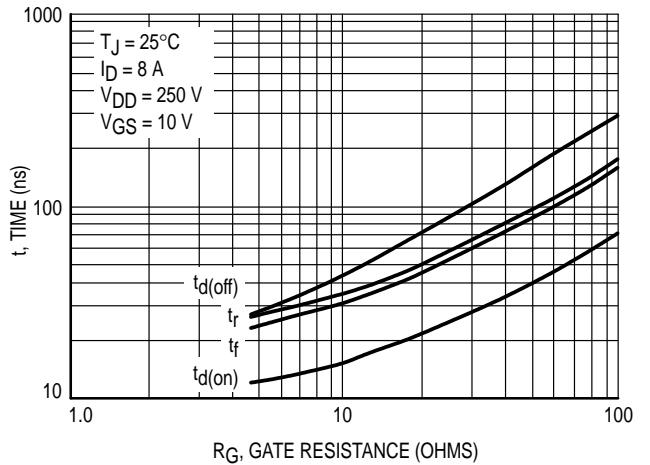


Figure 10. Resistive Switching Time Variation versus Gate Resistance

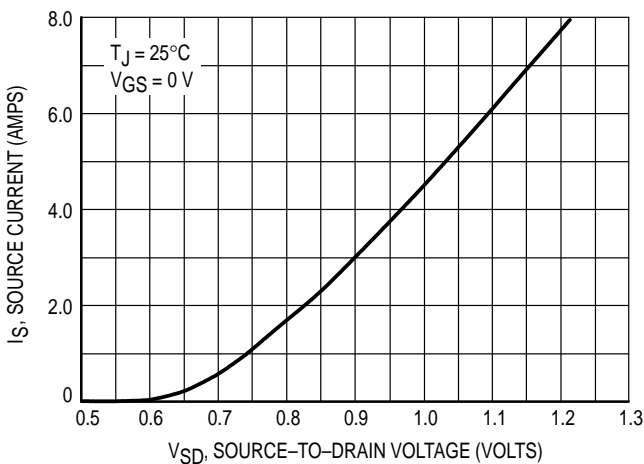


Figure 11. Diode Forward Voltage versus Current

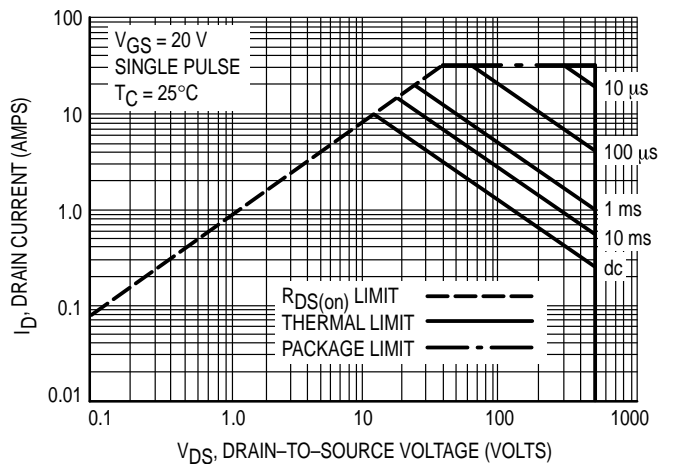


Figure 12. Maximum Rated Forward Biased Safe Operating Area

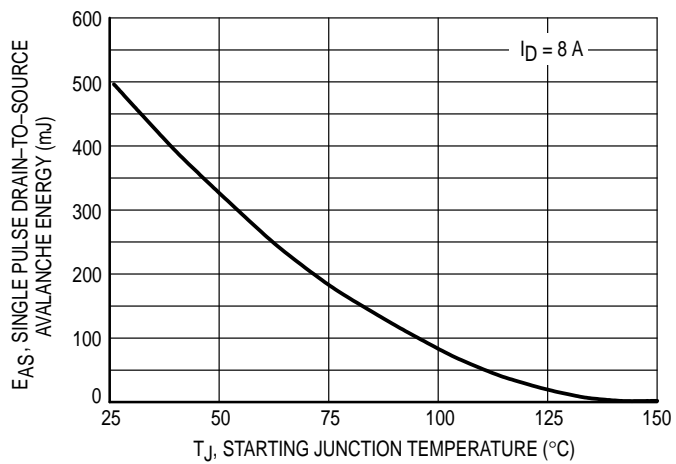


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

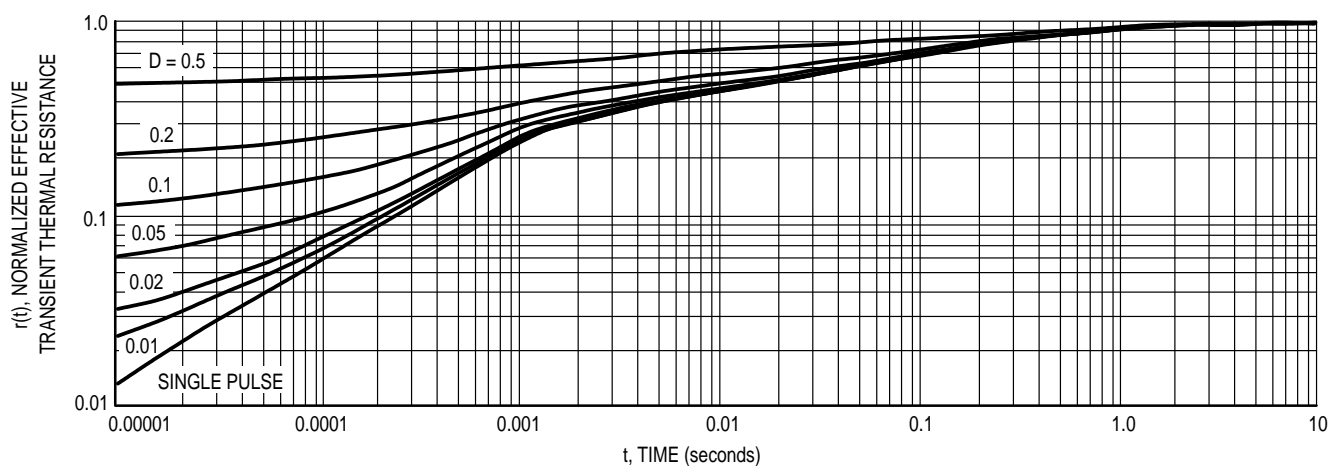
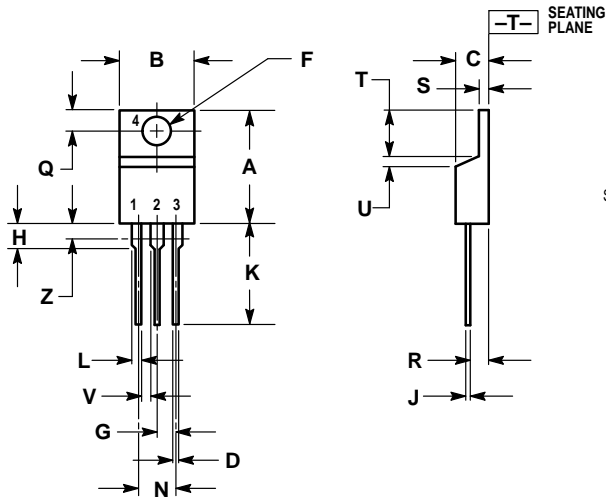


Figure 14. Thermal Response

PACKAGE DIMENSIONS




STYLE 5:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. DRAIN

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-06  
 ISSUE Y

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;  
 P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,  
 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

Mfax™: RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609  
 INTERNET: http://Design-NET.com

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

