ANALOG DEVICES

Ultralow Offset Voltage Operational Amplifier

OP07

FEATURES

Low V_{OS}: 75 μV maximum
Low V_{OS} drift: 1.3 μV/°C maximum
Ultrastable vs. time: 1.5 μV per month maximum
Low noise: 0.6 μV p-p maximum
Wide input voltage range: ±14 V typical
Wide supply voltage range: 3 V to 18 V
125°C temperature-tested dice

APPLICATIONS

Wireless base station control circuits
Optical network control circuits
Instrumentation
Sensors and controls
- **Thermocouples**
- **Resistor thermal detectors (RTDs)**
- **Strain bridges**
- **Shunt current measurements**

Precision filters

PIN CONFIGURATION

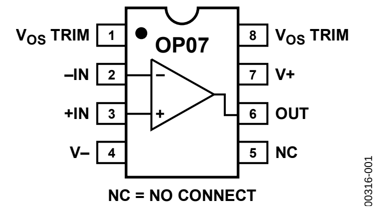


Figure 1.

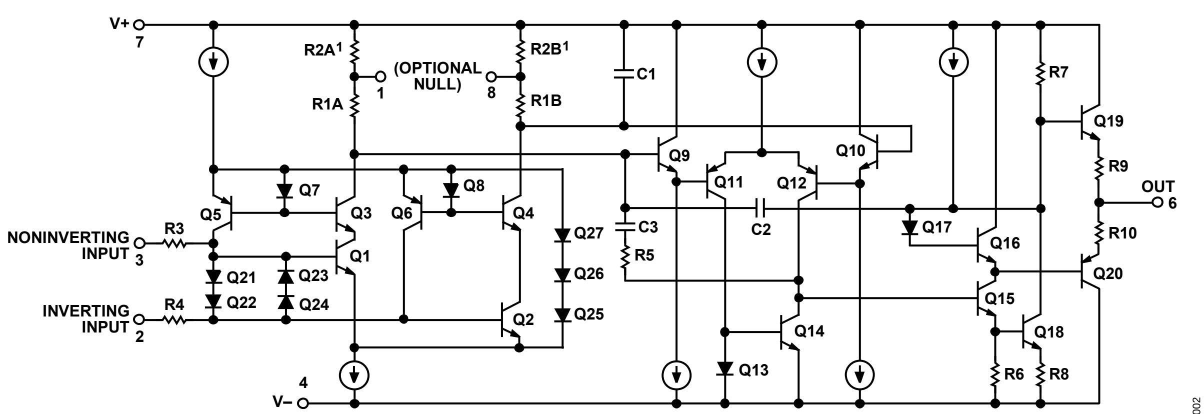
GENERAL DESCRIPTION

The OP07 has very low input offset voltage (75 μV maximum for OP07E) that is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP07 also features low input bias current (±4 nA for the OP07E) and high open-loop gain (200 V/mV for the OP07E). The low offset and high open-loop gain make the OP07 particularly useful for high gain instrumentation applications.

The wide input voltage range of ±13 V minimum combined with a high CMRR of 106 dB (OP07E) and high input impedance provide high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP07, even at high gain, combined with the freedom from external nulling have made the OP07 an industry standard for instrumentation applications.

The OP07 is available in two standard performance grades. The OP07E is specified for operation over the 0°C to 70°C range, and the OP07C is specified over the −40°C to +85°C temperature range.

The OP07 is available in epoxy 8-lead PDIP and 8-lead narrow SOIC packages. For CERDIP and TO-99 packages and standard microcircuit drawing (SMD) versions, see the OP77.



[1] R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

Figure 2. Simplified Schematic

Rev. E

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SPECIFICATIONS

OP07E ELECTRICAL CHARACTERISTICS

V_S = ±15 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
T_A = 25°C						
Input Offset Voltage[1]	V_{OS}			30	75	µV
Long-Term V_{OS} Stability[2]	V_{OS}/Time			0.3	1.5	µV/Month
Input Offset Current	I_{OS}			0.5	3.8	nA
Input Bias Current	I_B			±1.2	±4.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz		10.3	18.0	nV/√Hz
		f_O = 100 Hz[3]		10.0	13.0	nV/√Hz
		f_O = 1 kHz		9.6	11.0	nV/√Hz
Input Noise Current	I_n p-p			14	30	pA p-p
Input Noise Current Density	I_n	f_O = 10 Hz		0.32	0.80	pA/√Hz
		f_O = 100 Hz[3]		0.14	0.23	pA/√Hz
		f_O = 1 kHz		0.12	0.17	pA/√Hz
Input Resistance, Differential Mode[4]	R_{IN}		15	50		MΩ
Input Resistance, Common Mode	R_{INCM}			160		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	106	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		5	20	µV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	200	500		V/mV
		R_L ≥ 500 Ω, V_O = ±0.5 V, V_S = ±3 V[4]	150	400		V/mV
0°C ≤ T_A ≤ 70°C						
Input Offset Voltage[1]	V_{OS}			45	130	µV
Voltage Drift Without External Trim[4]	TCV_{OS}			0.3	1.3	µV/°C
Voltage Drift with External Trim[3]	TCV_{OSN}	R_P = 20 kΩ		0.3	1.3	µV/°C
Input Offset Current	I_{OS}			0.9	5.3	nA
Input Offset Current Drift	TCI_{OS}			8	35	pA/°C
Input Bias Current	I_B			±1.5	±5.5	nA
Input Bias Current Drift	TCI_B			13	35	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	103	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		7	32	µV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	180	450		V/mV
OUTPUT CHARACTERISTICS						
T_A = 25°C						
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±12.5	±13.0		V
		R_L ≥ 2 kΩ	±12.0	±12.8		V
		R_L ≥ 1 kΩ	±10.5	±12.0		V
0°C ≤ T_A ≤ 70°C						
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±12.6		V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
T_A = 25°C						
Slew Rate	SR	$R_L \geq 2$ kΩ[3]	0.1	0.3		V/µs
Closed-Loop Bandwidth	BW	$A_{VOL} = 1$[5]	0.4	0.6		MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$		60		Ω
Power Consumption	P_d	$V_S = \pm 15$ V, No load		75	120	mW
		$V_S = \pm 3$ V, No load		4	6	mW
Offset Adjustment Range		$R_P = 20$ kΩ		±4		mV

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
[2] Long-term input offset voltage stability refers to the averaged trend time of V_{OS} vs. the time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV. Refer to the Typical Performance Characteristics section. Parameter is sample tested.
[3] Sample tested.
[4] Guaranteed by design.
[5] Guaranteed but not tested.

OP07C ELECTRICAL CHARACTERISTICS

$V_S = \pm 15$ V, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
T_A = 25°C						
Input Offset Voltage[1]	V_{OS}			60	150	µV
Long-Term V_{OS} Stability[2]	V_{OS}/Time			0.4	2.0	µV/Month
Input Offset Current	I_{OS}			0.8	6.0	nA
Input Bias Current	I_B			±1.8	±7.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.38	0.65	µV p-p
Input Noise Voltage Density	e_n	$f_O = 10$ Hz		10.5	20.0	nV/√Hz
		$f_O = 100$ Hz[3]		10.2	13.5	nV/√Hz
		$f_O = 1$ kHz		9.8	11.5	nV/√Hz
Input Noise Current	I_n p-p			15	35	pA p-p
Input Noise Current Density	I_n	$f_O = 10$ Hz		0.35	0.90	pA/√Hz
		$f_O = 100$ Hz[3]		0.15	0.27	pA/√Hz
		$f_O = 1$ kHz		0.13	0.18	pA/√Hz
Input Resistance, Differential Mode[4]	R_{IN}		8	33		MΩ
Input Resistance, Common Mode	R_{INCM}			120		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13$ V	100	120		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3$ V to ±18 V		7	32	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	120	400		V/mV
		$R_L \geq 500$ Ω, $V_O = \pm 0.5$ V, $V_S = \pm 3$ V[4]	100	400		V/mV
−40°C ≤ T_A ≤ +85°C						
Input Offset Voltage[1]	V_{OS}			85	250	µV
Voltage Drift Without External Trim[4]	TCV_{OS}			0.5	1.8	µV/°C
Voltage Drift with External Trim[3]	TCV_{OSN}	$R_P = 20$ kΩ		0.4	1.6	µV/°C
Input Offset Current	I_{OS}			1.6	8.0	nA
Input Offset Current Drift	TCI_{OS}			12	50	pA/°C
Input Bias Current	I_B			±2.2	±9.0	nA
Input Bias Current Drift	TCI_B			18	50	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13$ V	97	120		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3$ V to ±18 V		10	51	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	100	400		V/mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
T_A = 25°C						
Output Voltage Swing	V_O	$R_L \geq 10$ kΩ	±12.0	±13.0		V
		$R_L \geq 2$ kΩ	±11.5	±12.8		V
		$R_L \geq 1$ kΩ		±12.0		V
−40°C ≤ T_A ≤ +85°C						
Output Voltage Swing	V_O	$R_L \geq 2$ kΩ	±12	±12.6		V
DYNAMIC PERFORMANCE						
T_A = 25°C						
Slew Rate	SR	$R_L \geq 2$ kΩ[3]	0.1	0.3		V/µs
Closed-Loop Bandwidth	BW	A_{VOL} = 1[5]	0.4	0.6		MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0		60		Ω
Power Consumption	P_d	V_S = ±15 V, No load		80	150	mW
		V_S = ±3 V, No load		4	8	mW
Offset Adjustment Range		R_P = 20 kΩ		±4		mV

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
[2] Long-term input offset voltage stability refers to the averaged trend time of V_{OS} vs. the time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV. Refer to the Typical Performance Characteristics section. Parameter is sample tested.
[3] Sample tested.
[4] Guaranteed by design.
[5] Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
Supply Voltage (V_S)	±22 V
Input Voltage[1]	±22 V
Differential Input Voltage	±30 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
S and P Packages	−65°C to +125°C
Operating Temperature Range	
OP07E	0°C to 70°C
OP07C	−40°C to +85°C
Junction Temperature	150°C
Lead Temperature, Soldering (60 sec)	300°C

[1] For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead PDIP (P-Suffix)	103	43	°C/W
8-Lead SOIC_N (S-Suffix)	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

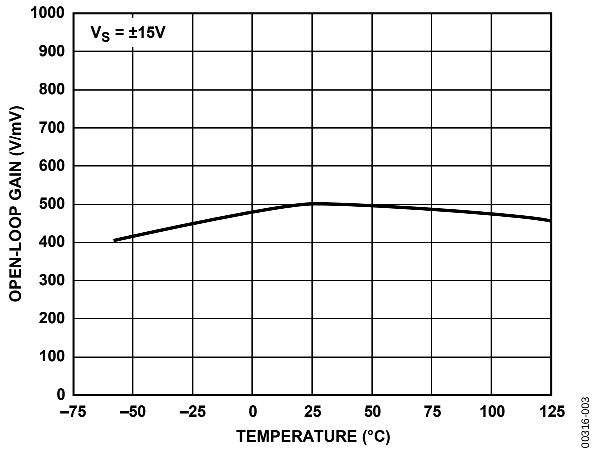

Figure 3. Open-Loop Gain vs. Temperature

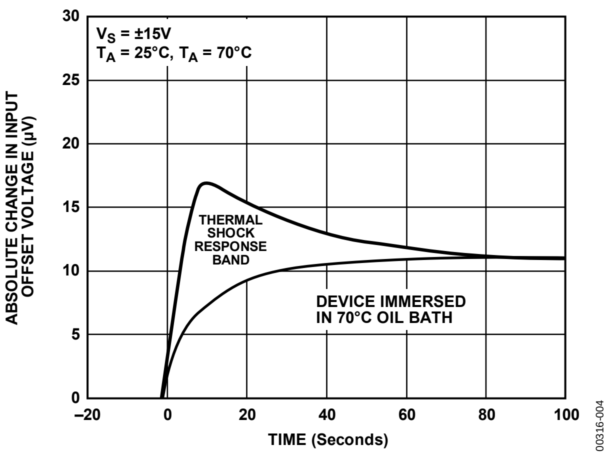

Figure 4. Offset Voltage Change due to Thermal Shock

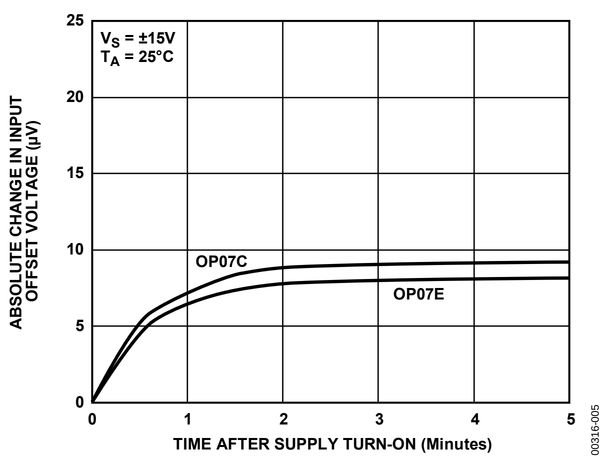

Figure 5. Warm-Up Drift

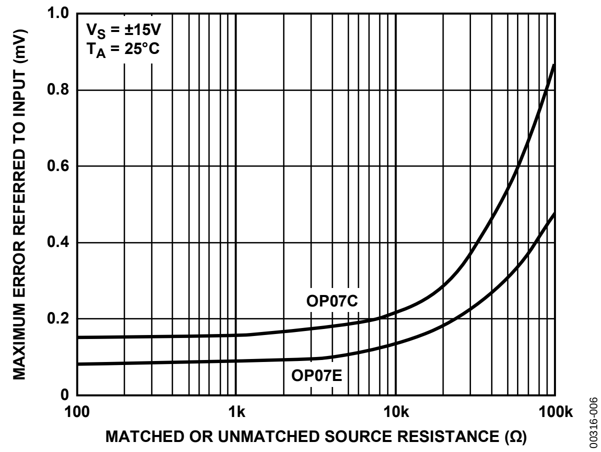

Figure 6. Maximum Error vs. Source Resistance

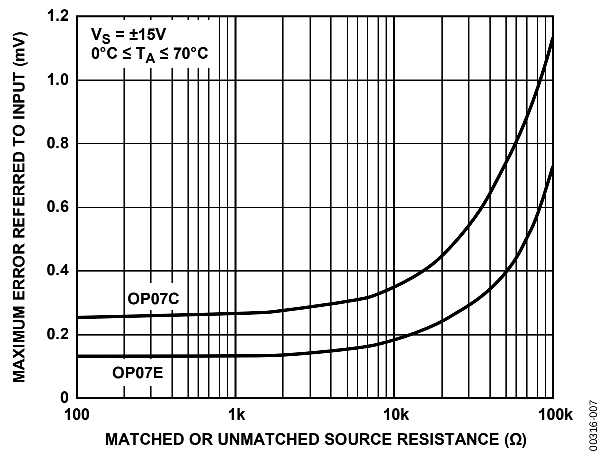

Figure 7. Maximum Error vs. Source Resistance

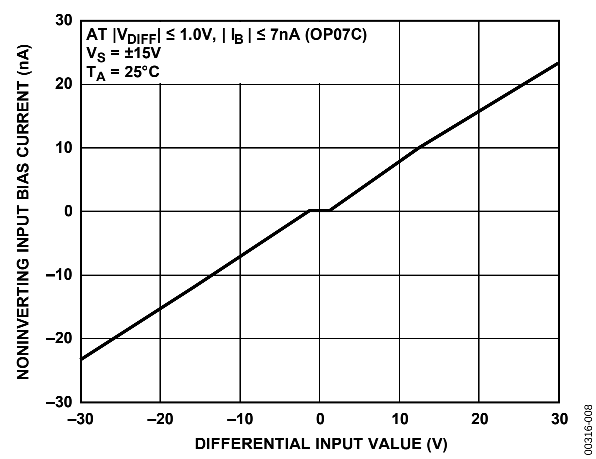

Figure 8. Input Bias Current vs. Differential Input Voltage

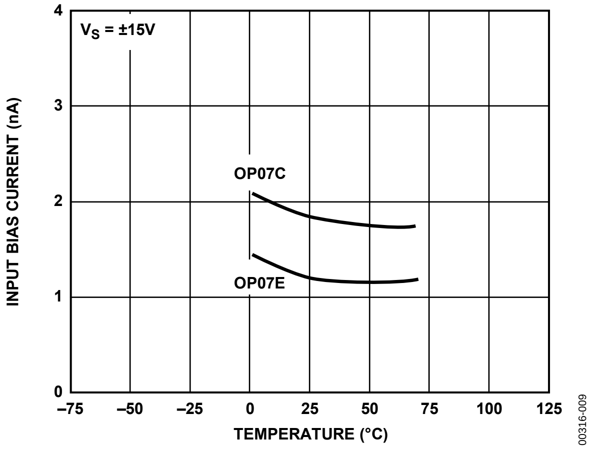

Figure 9. Input Bias Current vs. Temperature

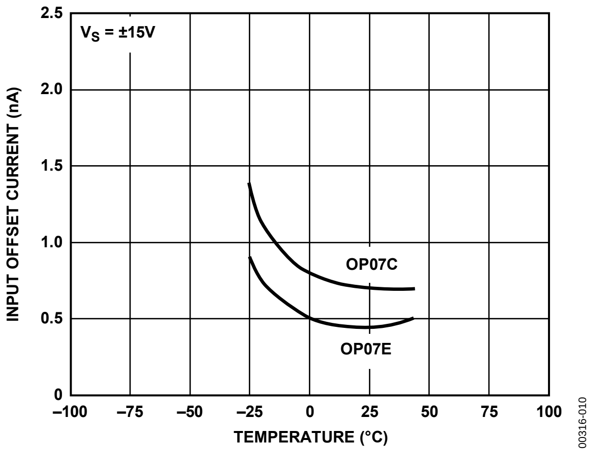

Figure 10. Input Offset Current vs. Temperature

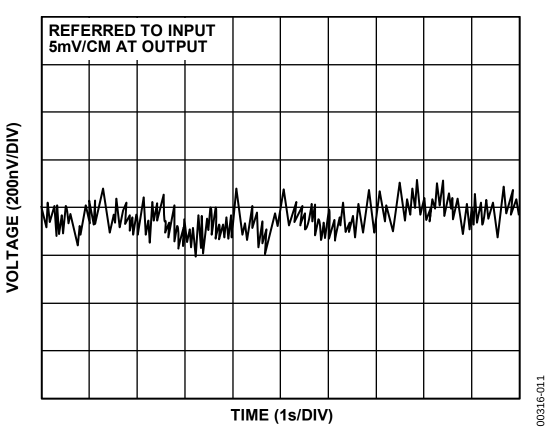

Figure 11. Low Frequency Noise

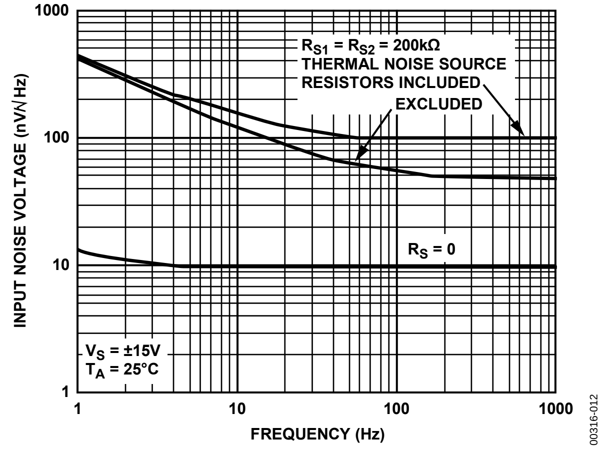

Figure 12. Total Input Noise Voltage vs. Frequency

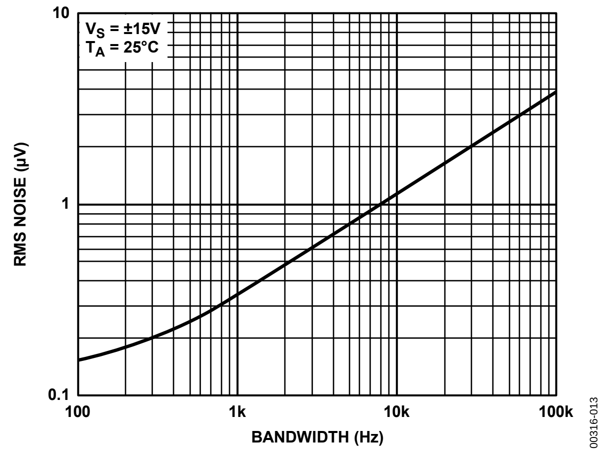

Figure 13. Input Wideband Noise vs. Bandwidth, 0.1 Hz to Frequency Indicated

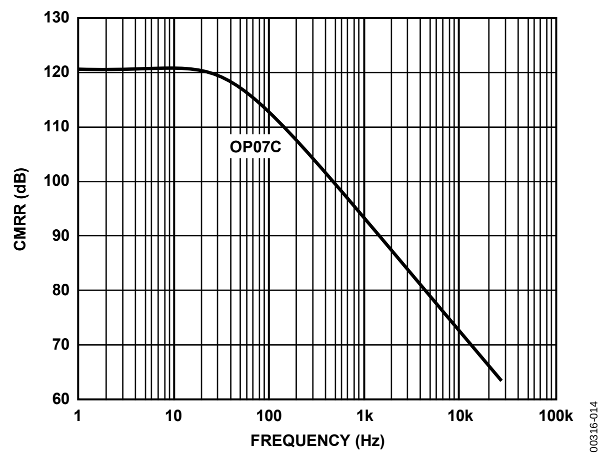

Figure 14. CMRR vs. Frequency

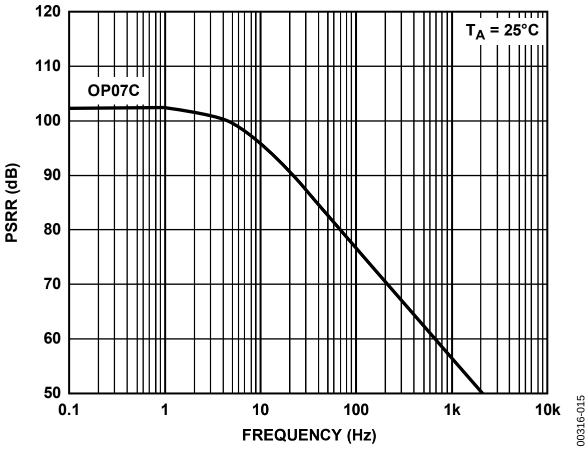

Figure 15. PSRR vs. Frequency

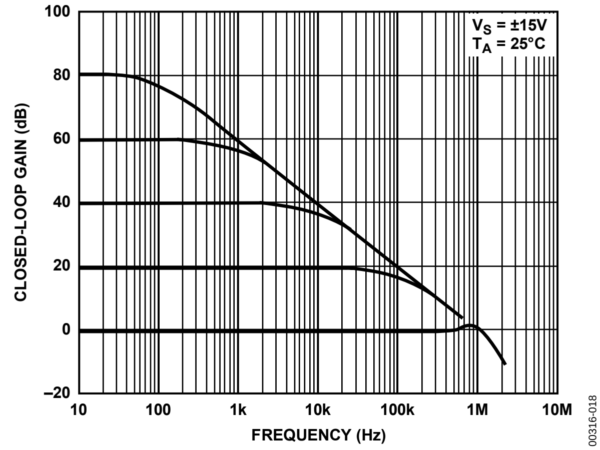

Figure 18. Closed-Loop Frequency Response for Various Gain Configurations

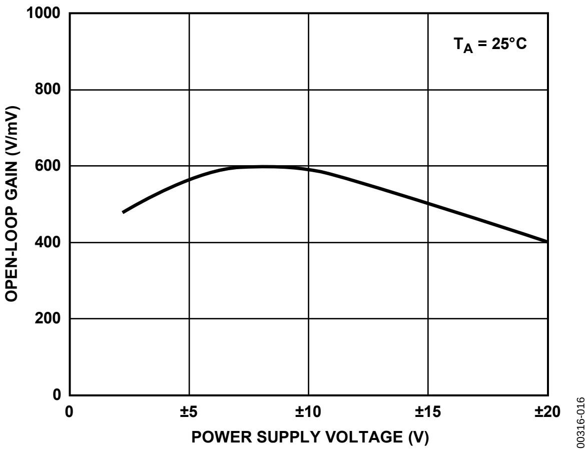

Figure 16. Open-Loop Gain vs. Power Supply Voltage

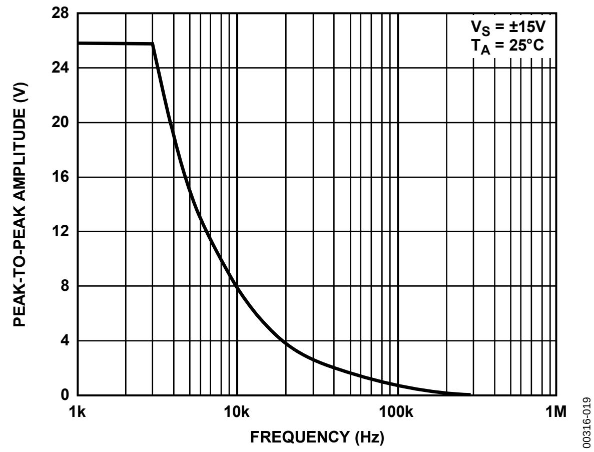

Figure 19. Maximum Output Swing vs. Frequency

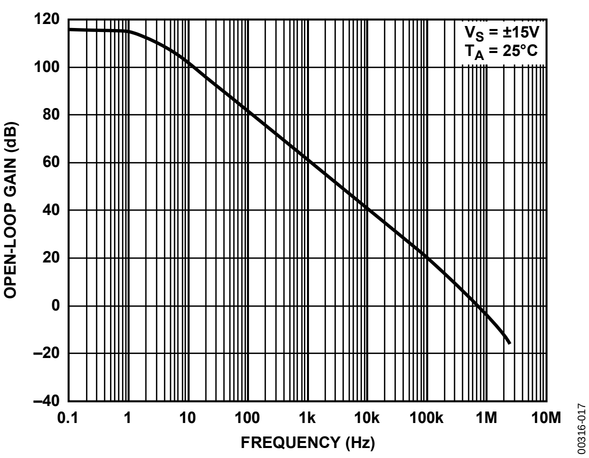

Figure 17. Open-Loop Frequency Response

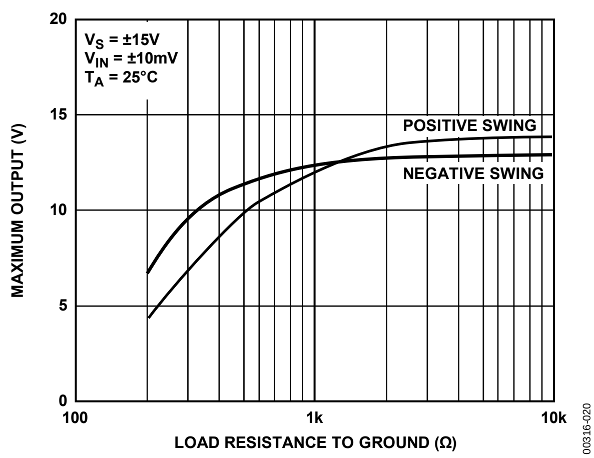

Figure 20. Maximum Output Voltage vs. Load Resistance

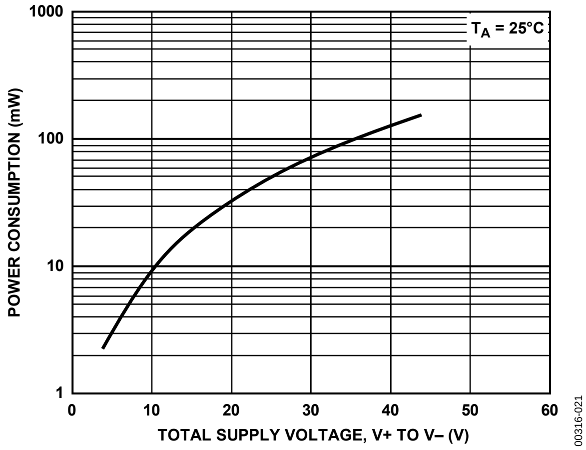

Figure 21. Power Consumption vs. Power Supply

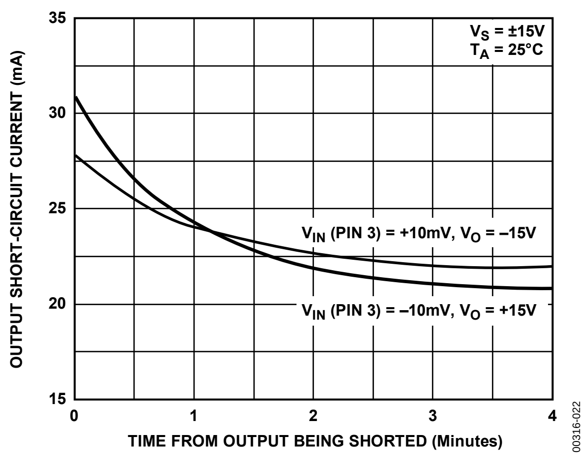

Figure 22. Output Short-Circuit Current vs. Time

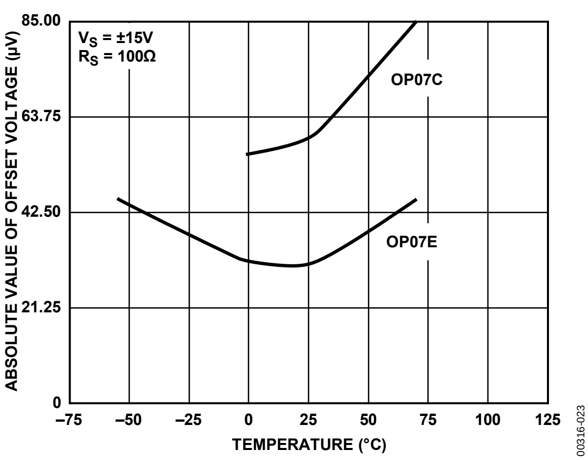

Figure 23. Untrimmed Offset Voltage vs. Temperature

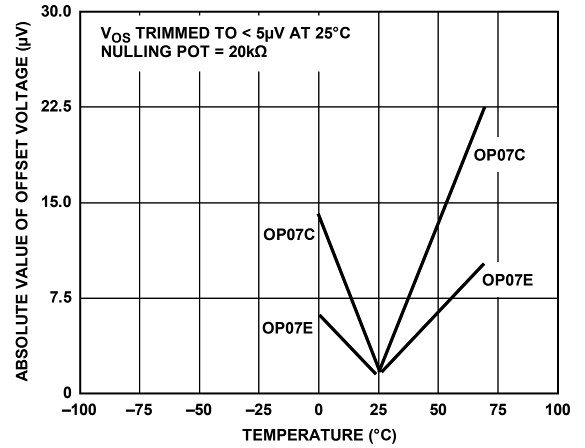

Figure 24. Trimmed Offset Voltage vs. Temperature

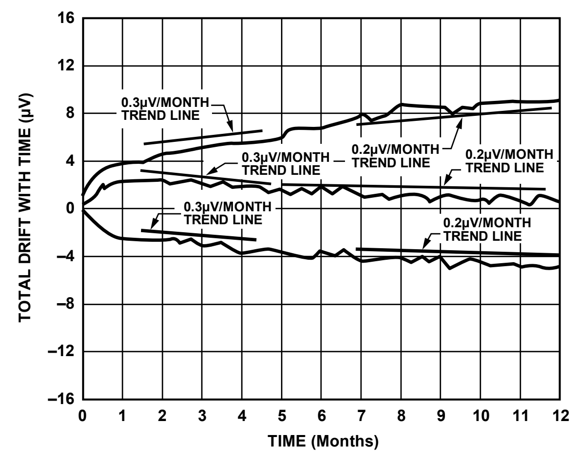

Figure 25. Offset Voltage Drift vs. Time

TYPICAL APPLICATIONS

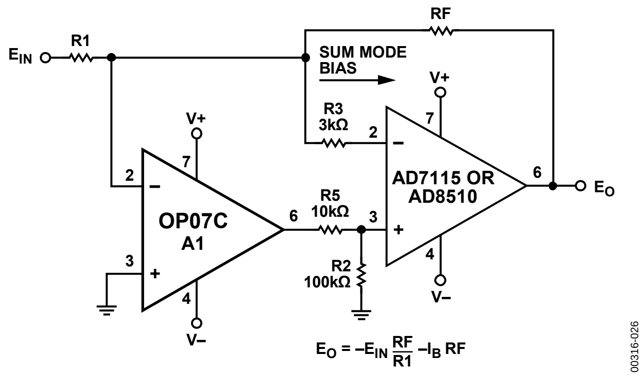

Figure 26. Typical Offset Voltage Test Circuit

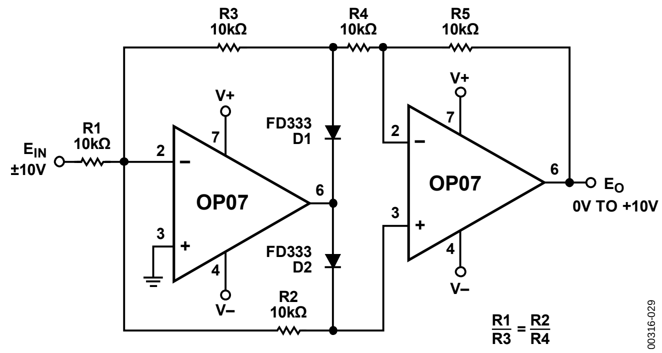

Figure 29. Absolute Value Circuit

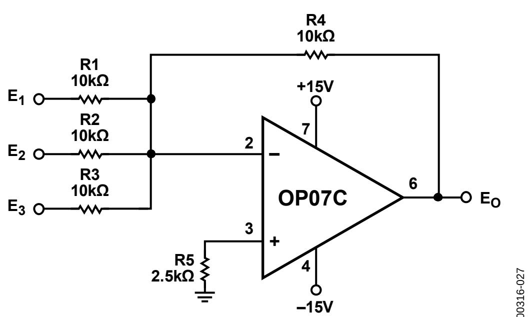

Figure 27. Typical Low Frequency Noise Circuit

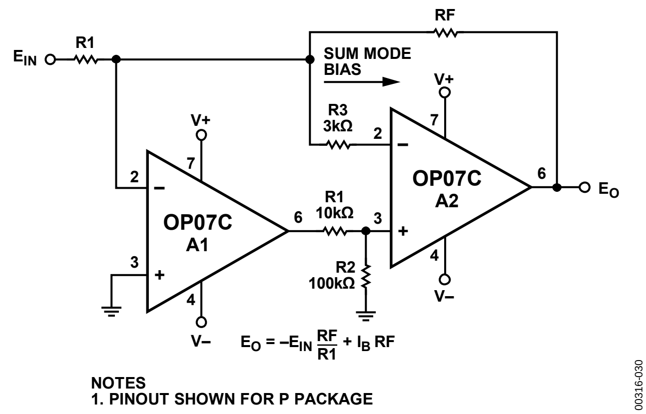

Figure 30. High Speed, Low V_{OS} Composite Amplifier

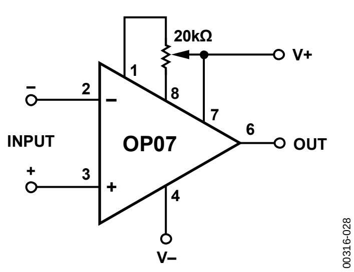

Figure 28. Optional Offset Nulling Circuit

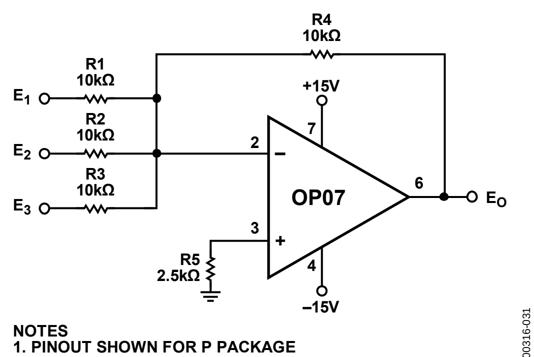

Figure 31. Adjustment-Free Precision Summing Amplifier

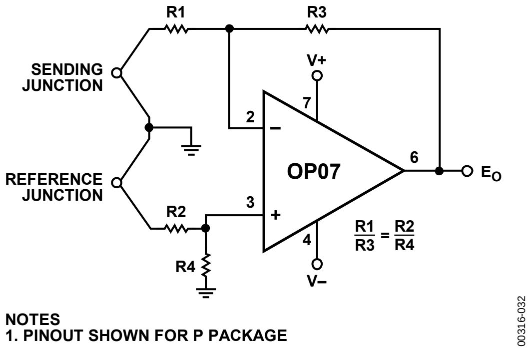

Figure 32. High Stability Thermocouple Amplifier

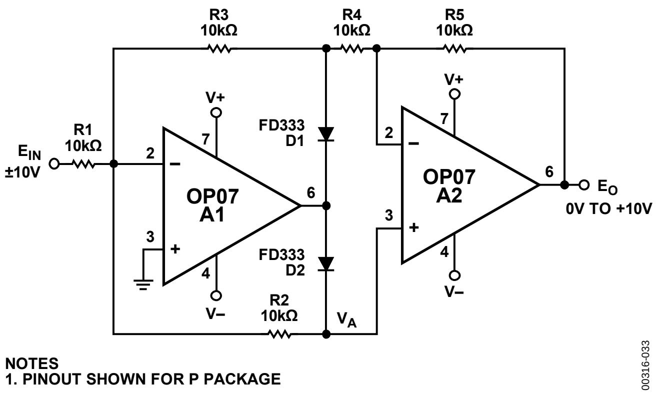

Figure 33. Precision Absolute-Value Circuit

APPLICATIONS INFORMATION

The OP07 provides stable operation with load capacitance of up to 500 pF and ±10 V swings; larger capacitances should be decoupled with a 50 Ω decoupling resistor.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation is obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

OUTLINE DIMENSIONS

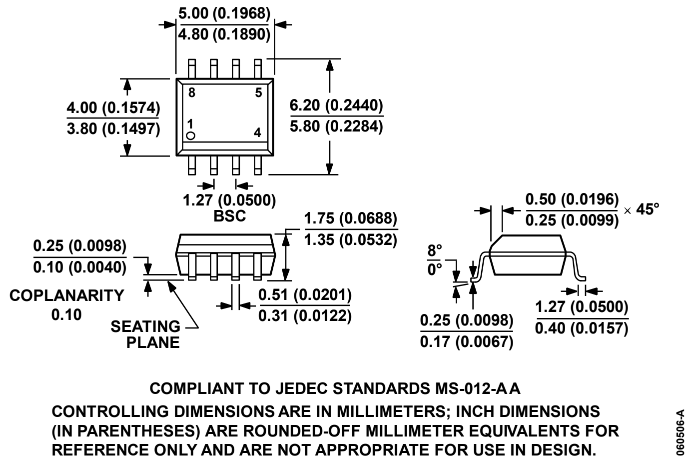

Figure 34. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body S-Suffix
(R-8)
Dimensions shown in millimeters and (inches)

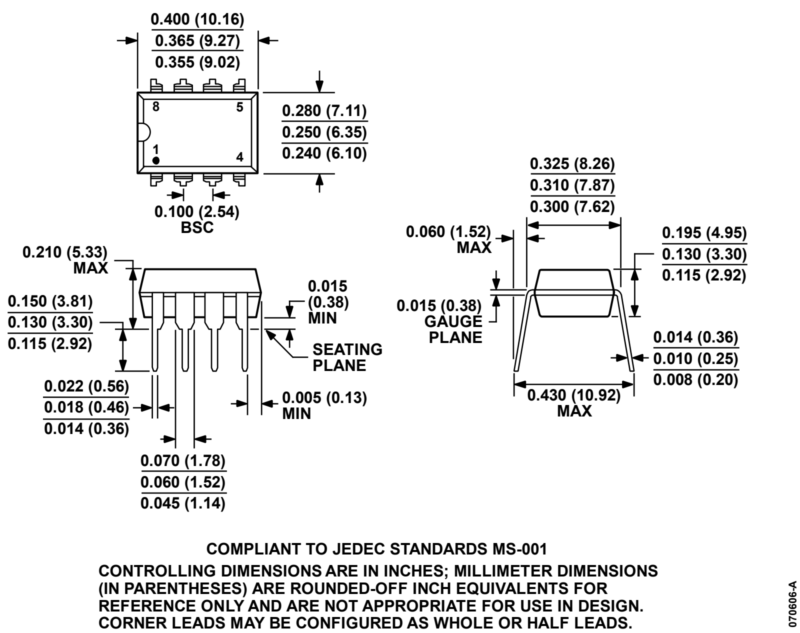

Figure 35. 8-Lead Plastic Dual-in-Line Package [PDIP]
P-Suffix
(N-8)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP07EP	0°C to 70°C	8-Lead PDIP	N-8 (P-Suffix)
OP07EPZ[1]	0°C to 70°C	8-Lead PDIP	N-8 (P-Suffix)
OP07CP	0°C to 70°C	8-Lead PDIP	N-8 (P-Suffix)
OP07CPZ[1]	−40°C to +85°C	8-Lead PDIP	N-8 (P-Suffix)
OP07CS	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP07CSZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP07CSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP07CSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)

[1] Z = RoHS Compliant Part.

NOTES

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