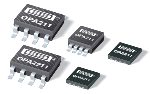


1.1 nV/√Hz Noise, Low Power, Precision Operational Amplifier

Check for Samples: OPA211-HT

FEATURES

- Low Voltage Noise: 1.1 nV/√Hz at 1 kHz
- Input Voltage Noise:
  80 nV_{PP} (0.1 Hz to 10 Hz)
- THD+N: –136 dB (G = 1, f = 1 kHz)
- Offset Voltage: 240 µV (max)
- Offset Voltage Drift: 0.35 µV/°C (typ)
- Low Supply Current: 6.0 mA/Ch (typ)
- Unity-Gain Stable
- Gain Bandwidth Product:
  80 MHz (G = 100)
  45 MHz (G = 1)
- Slew Rate: 27 V/µs
- 16-Bit Settling: 700 ns
- Wide Supply Range:
  ±2.25 V to ±18 V, 4.5 V to 36 V
- Rail-To-Rail Output
- Output Current: 30 mA

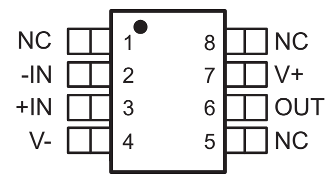
APPLICATIONS

- Down-Hole Drilling
- High Temperature Environments

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extreme (–55°C/210°C) Temperature Range(1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.

HKJ PACKAGE
(TOP VIEW)



NC denotes no internal connection

(1) Custom temperature ranges available

DESCRIPTION

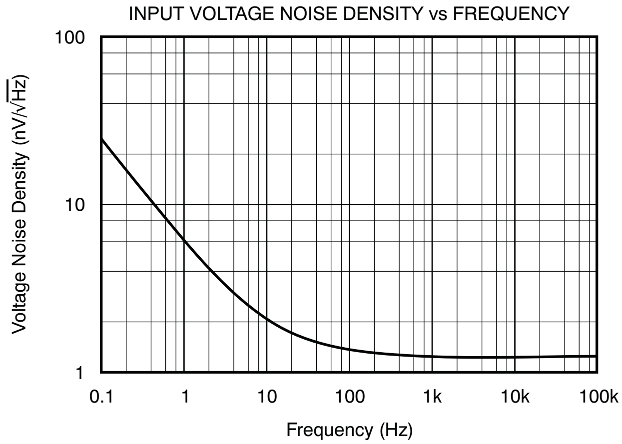
The OPA211 series of precision operational amplifiers achieves very low 1.1 nV/√Hz noise density with a supply current of only 3.6 mA. This series also offers rail-to-rail output swing, which maximizes dynamic range.

The extremely low voltage and low current noise, high speed, and wide output swing of the OPA211 series make these devices an excellent choice as a loop filter amplifier in PLL applications.

In precision data acquisition applications, the OPA211 series of op amps provides 700-ns settling time to 16-bit accuracy throughout 10-V output swings. This ac performance, combined with only 240-µV of offset and 0.35-µV/°C of drift over temperature, makes the OPA211 ideal for driving high-precision 16-bit analog-to-digital converters (ADCs) or buffering the output of high-resolution digital-to-analog converters (DACs).

The OPA211 series is specified over a wide dual-power supply range of ±2.25 V to ±18 V, or for single-supply operation from 4.5 V to 36 V.

This series of op amps is specified from T_A = –55°C to 210°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

			VALUE	UNIT
V_S = (V=) – (V-)	Supply Voltage		40	V
V_{IN}	Input Voltage		(V–) – 0.5 to (V+) + 0.5	V
I_{IN}	Input Current (Any pin except power-supply pins)		±10	mA
	Output Short-Circuit(2)		Continuous	
T_A	Operating Temperature		–55 to 210	°C
T_{STG}	Storage Temperature		–65 to 210	°C
T_J	Junction Temperature		210	°C
	ESD Ratings	Human Body Model (HBM)	3000	V
		Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Short-circuit to V_S/2 (ground in symmetrical dual supply setups), one amplifier per package.

THERMAL CHARACTERISTICS FOR HKJ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance (to botom of case)			5.7	°C/W
	Junction-to-case thermal resistance (to top of case lid - as if formed dead bug)			13.7	

Table 1. ORDERING INFORMATION(1)

TA	PACKAGE (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	HKJ	OPA211SHKJ	OPA211SHKJ
	KGD	OPA211SKGD1	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	V-	Al-Si-Cu (0.5%)

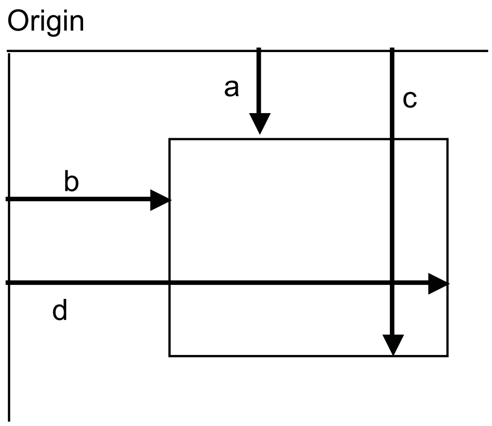
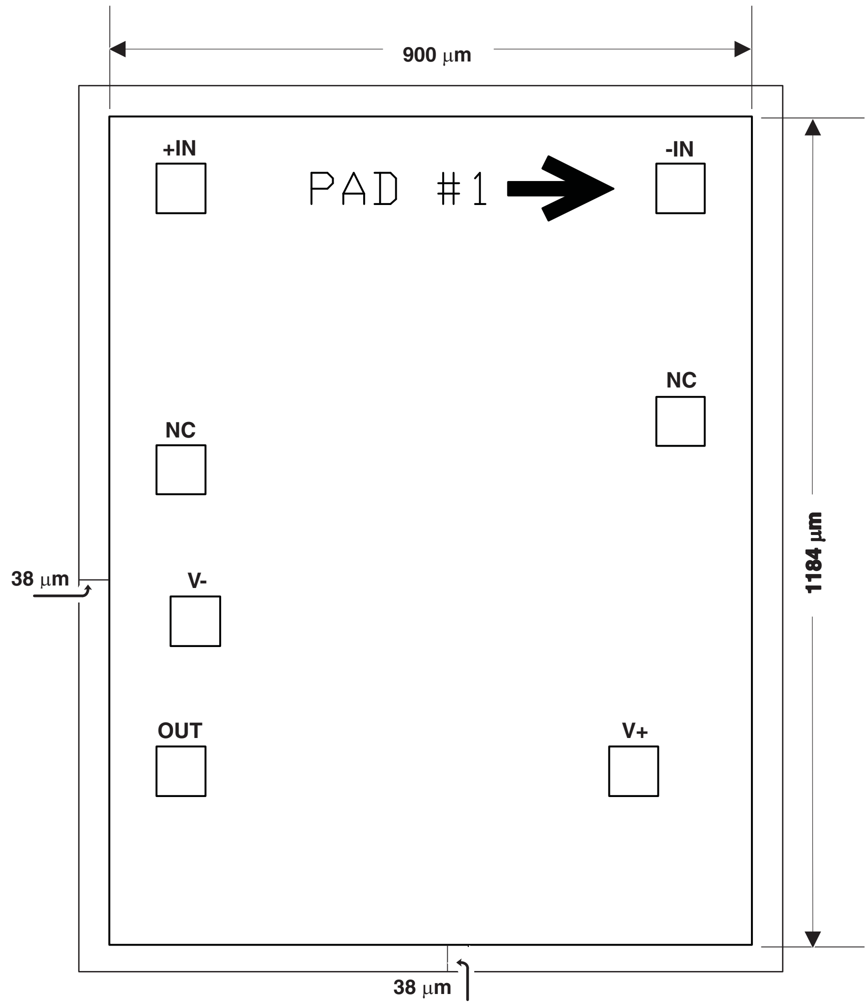


Table 2. BOND PAD COORDINATES

DESCRIPTION	PAD NUMBER	a	b	c	d
-IN	1	34.400	792.000	109.400	867.000
+IN	2	34.400	33.000	109.400	108.000
NC	3	461.850	33.000	536.850	108.000
V-	4	692.650	54.600	767.650	129.600
OUT	5	920.400	33.000	995.400	108.000
V+	6	920.400	720.150	995.400	795.150
NC	7	388.050	792.000	463.050	795.150



ELECTRICAL CHARACTERISTICS: V_S = ±2.25 V to ±18 V

At T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

			T_A = –55 to 125°C			T_A = 210°C			
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}	V_S = ±15V		±30	±180		±70	±260	μV
Drift	dV_{OS}/dT			0.35	1.5		0.35	2.0	μV/°C
vs Power Supply	PSRR	V_S = ±2.25V to ±18V		0.1	3		0.1	3	μV/V
INPUT BIAS CURRENT									
Input Bias Current	I_B	V_{CM} = 0V		±60	±200		±60	±250	nA
Offset Current	I_{OS}	V_{CM} = 0V		±25	±150		±25	±150	nA
NOISE									
Input Voltage Noise	e_n	f = 0.1Hz to 10Hz		80			80		nV_{PP}
Input Voltage Noise Density		f = 10Hz		2			2		$nV/\sqrt{Hz}$
		f = 100Hz		1.4			1.4		$nV/\sqrt{Hz}$
		f = 1kHz		1.1			1.1		$nV/\sqrt{Hz}$
Input Current Noise Density	I_n	f = 10Hz		3.2			3.2		$pA/\sqrt{Hz}$
		f = 1kHz		1.7			1.7		$pA/\sqrt{Hz}$
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V_{CM}	V_S ≥ ±5V	(V–) + 1.8		(V+) – 1.4	(V–) + 1.8		(V+) – 1.4	V
		V_S < ±5V	(V–) + 2		(V+) – 1.4	(V–) + 2		(V+) – 1.4	V
Common-Mode Rejection Ratio	CMRR	V_S ≥ ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V	114	120		113	120		dB
		V_S < ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V	108	120		93	100		dB
INPUT IMPEDANCE									
Differential				20k || 8			20k || 8		Ω || pF
Common-Mode				10^9 || 2			10^9 || 2		Ω || pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	A_{OL}	(V–) + 0.2V ≤ V_O ≤ (V+) – 0.2V, R_L = 10kΩ	114	130		112	118		dB
	A_{OL}	(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 600Ω	110	114		90	93		dB
FREQUENCY RESPONSE									
Gain-Bandwidth Product	GBW	G = 100		80			80		MHz
		G = 1		45			45		MHz
Slew Rate	SR			27			27		V/μs
Settling Time, 0.01%	t_S	V_S = ±15V, G = –1, 10V Step, C_L = 100pF		490			580		ns
0.0015% (16-bit)		V_S = ±15V, G = –1, 10V Step, C_L = 100pF		700			750		ns
Overload Recovery Time		G = –10		500			500		ns
Total Harmonic Distortion + Noise	THD+N	G = 1, f = 1kHz, V_O = $3V_{RMS}$, R_L = 600Ω		0.00001 5			0.000015		%
				–136			–136		dB

ELECTRICAL CHARACTERISTICS: V_S = ±2.25 V to ±18 V (continued)

At T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	T_A = –55 to 125°C MIN	TYP	MAX	T_A = 210°C MIN	TYP	MAX	UNIT
OUTPUT									
Voltage Output	V_{OUT}	R_L = 10kΩ, A_{OL} ≥ 114dB	(V–) + 0.2		(V+) – 0.2	(V–) + 0.2		(V+) – 0.2	V
		R_L = 600Ω, A_{OL} ≥ 110dB, ±18V	(V–) + 0.6		(V+) – 0.6	(V–) + 1.2		(V+) – 0.6	V
Short-Circuit Current	I_{SC}			+35/–50			+30/–45		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics						
Open-Loop Output Impedance	Z_O	f = 1MHz		5					Ω
POWER SUPPLY									
Specified Voltage	V_S		±2.25		±18	±2.25		±18	V
Quiescent Current (per channel)	I_Q	I_{OUT} = 0A		3.6	6		6.0	7.5	mA
TEMPERATURE RANGE									
Specified range		–55°C to 210°C							
Operating range		–55°C to 210°C							

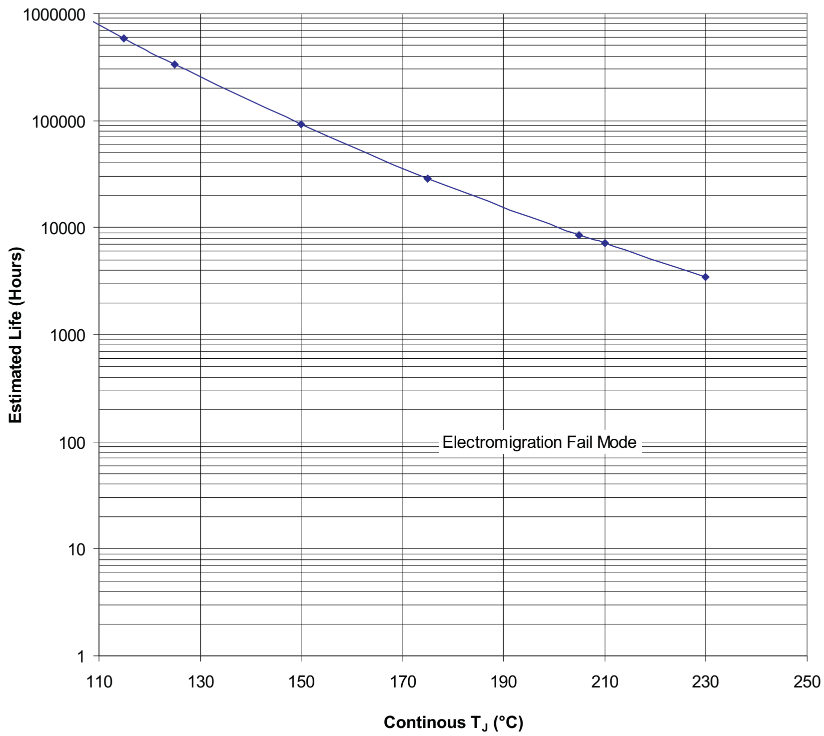


Figure 1. OPA211SKGD1 Operating Life Derating Chart

Notes:

1. See datasheet for absolute maximum and minimum recommended operating conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

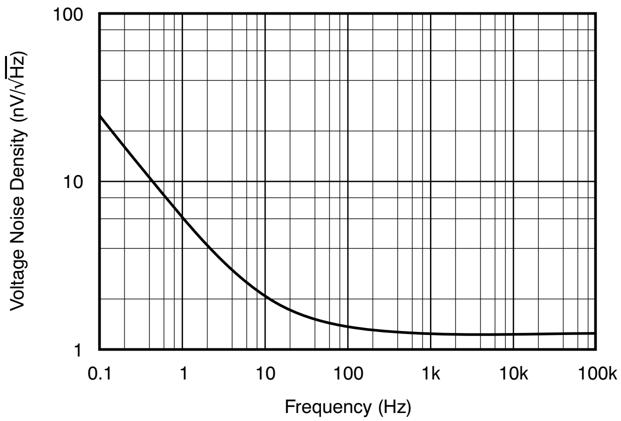


Figure 2.

INPUT CURRENT NOISE DENSITY vs FREQUENCY

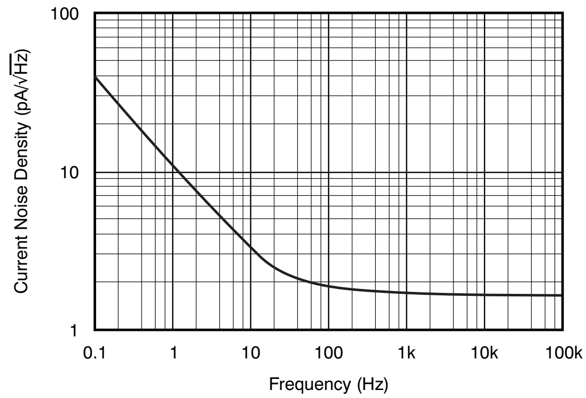


Figure 3.

THD+N RATIO vs FREQUENCY

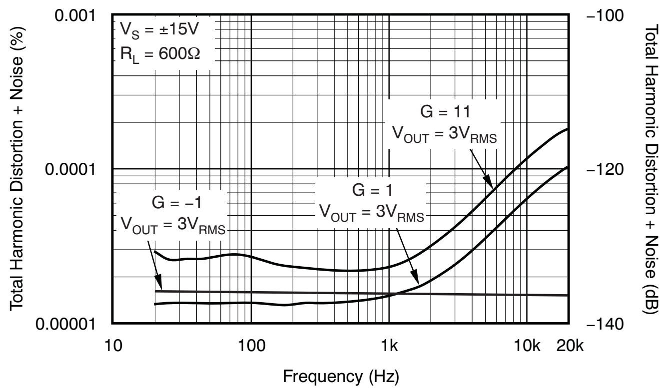


Figure 4.

THD+N RATIO vs OUTPUT VOLTAGE AMPLITUDE

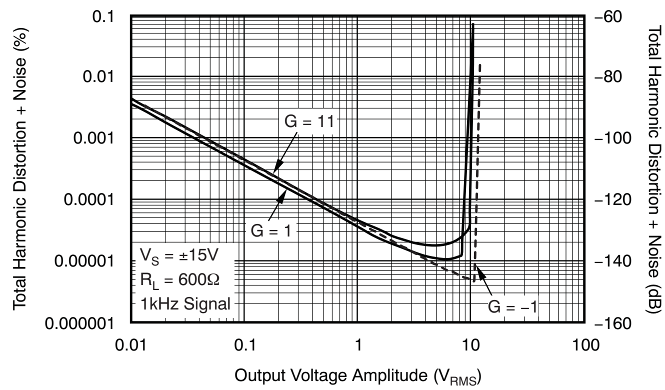


Figure 5.

0.1-Hz TO 10-Hz NOISE

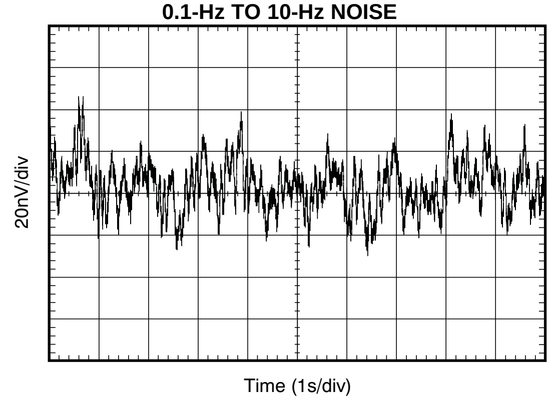


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY (Referred to Input)

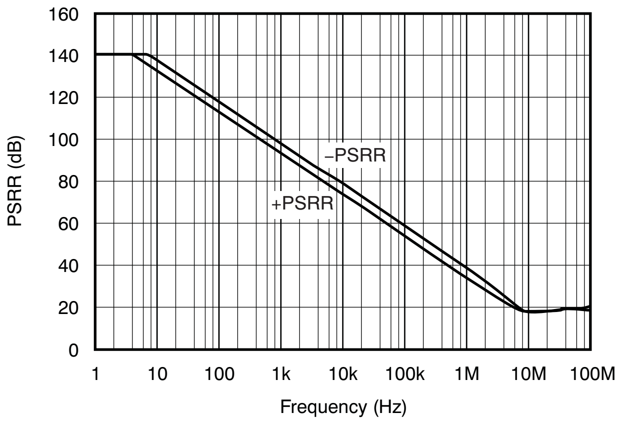


Figure 7.

COMMON-MODE REJECTION RATIO vs FREQUENCY

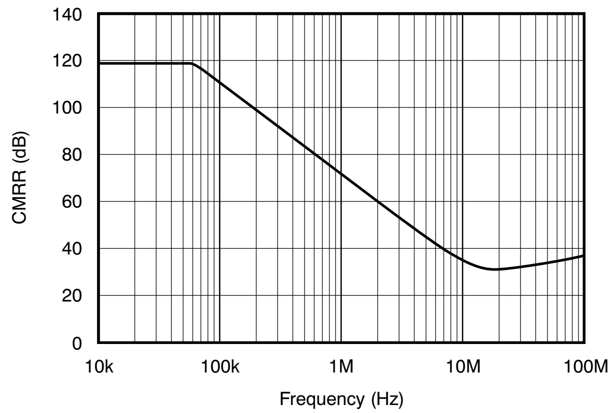


Figure 8.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

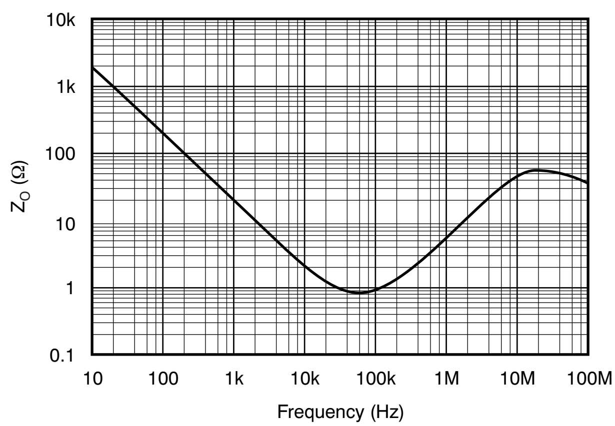


Figure 9.

GAIN AND PHASE vs FREQUENCY

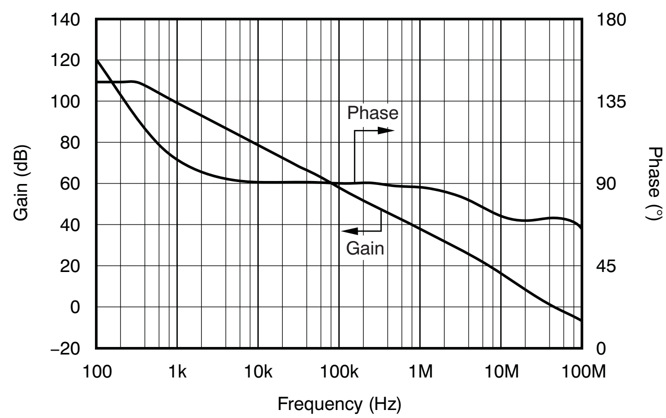


Figure 10.

OPEN-LOOP GAIN vs TEMPERATURE (R_L = 10 kΩ)

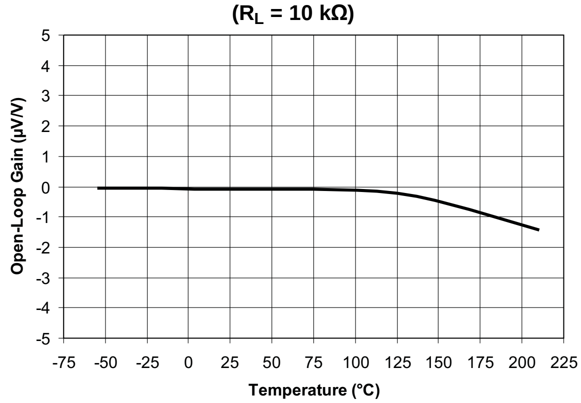


Figure 11.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

I_B AND I_{OS} CURRENT vs TEMPERATURE

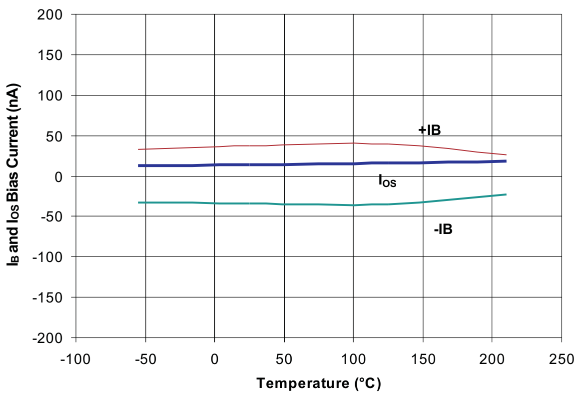


Figure 12.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

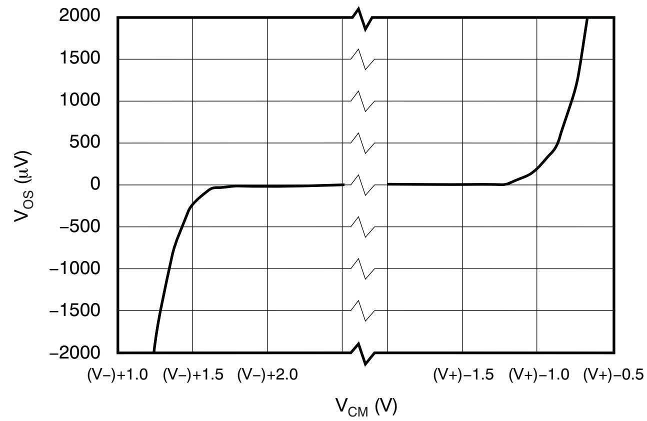


Figure 13.

V_{OS} WARMUP

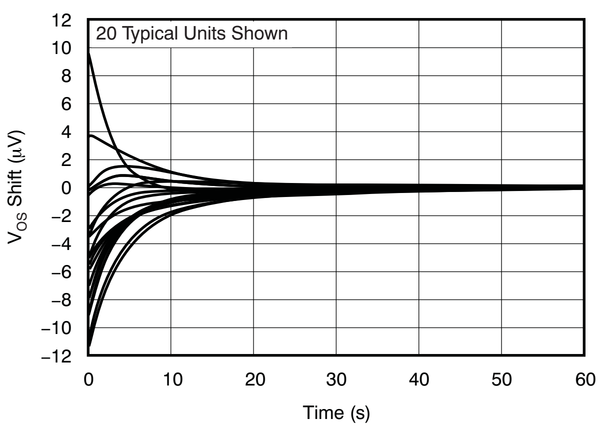


Figure 14.

INPUT OFFSET CURRENT vs SUPPLY VOLTAGE

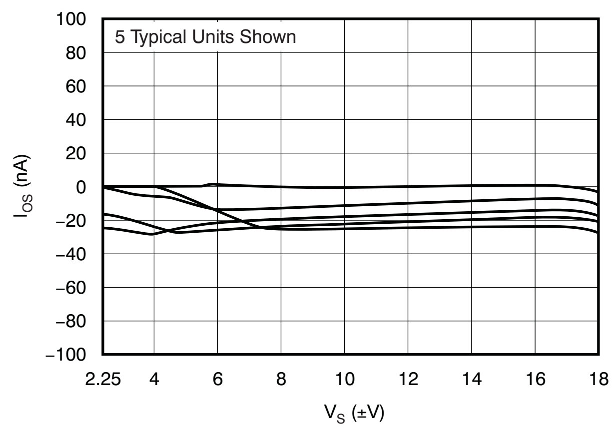


Figure 15.

INPUT OFFSET CURRENT vs COMMON-MODE VOLTAGE

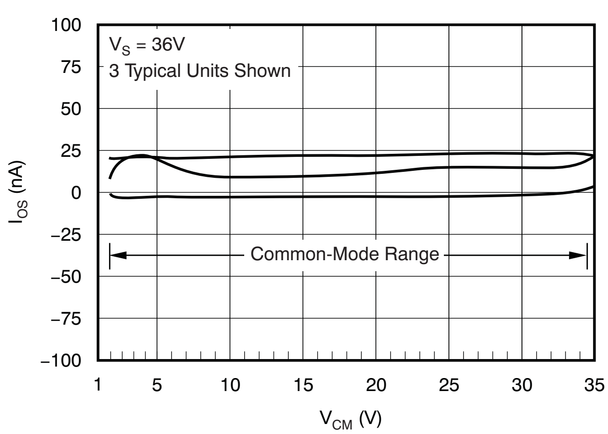


Figure 16.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

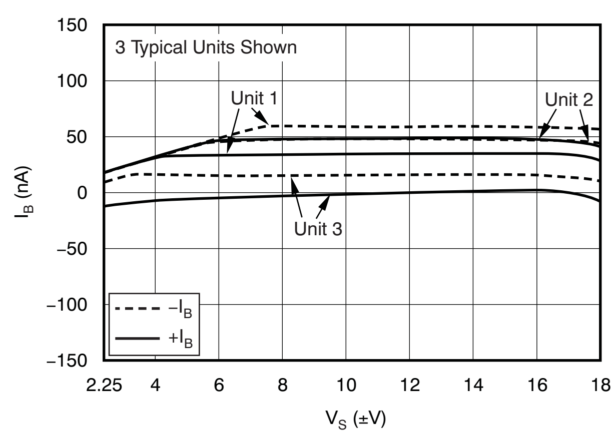


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

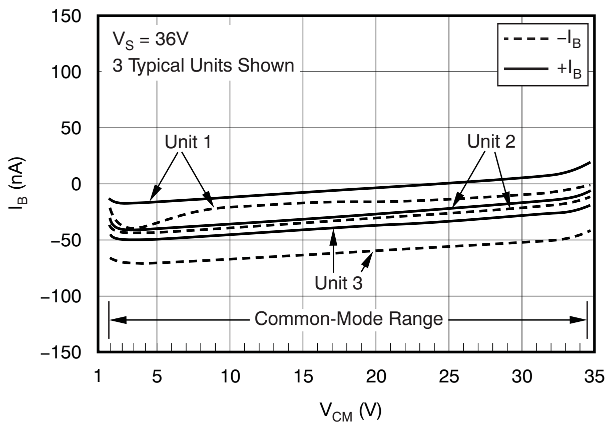


Figure 18.

QUIESCENT CURRENT vs TEMPERATURE

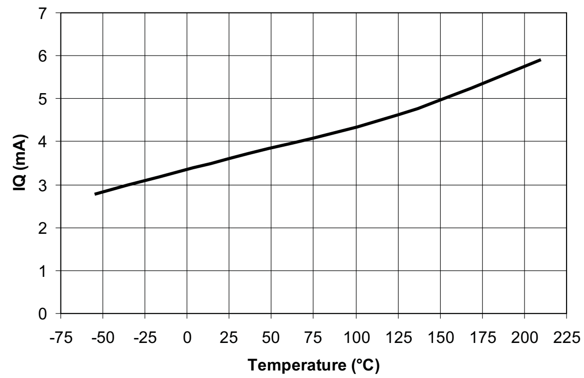


Figure 19.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

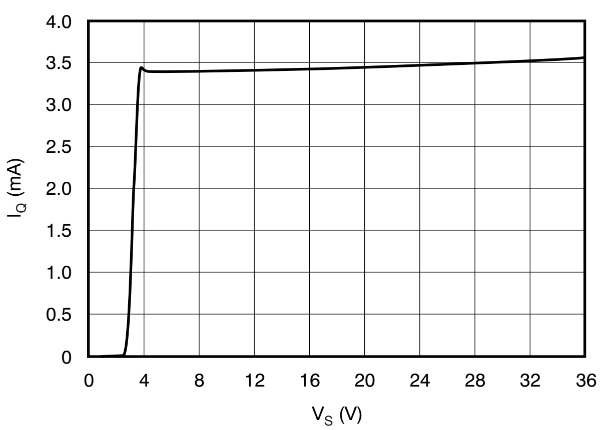


Figure 20.

NORMALIZED QUIESCENT CURRENT vs TIME

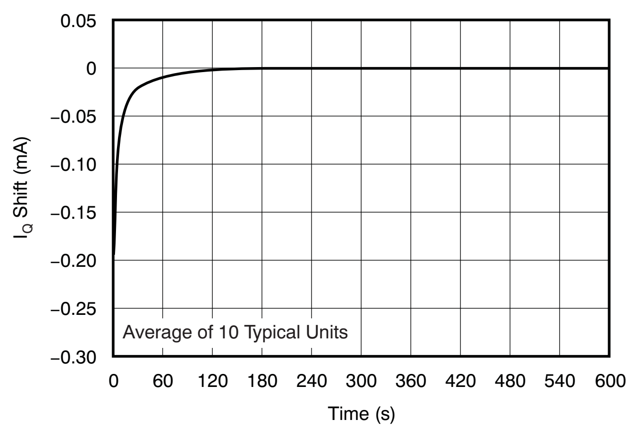


Figure 21.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

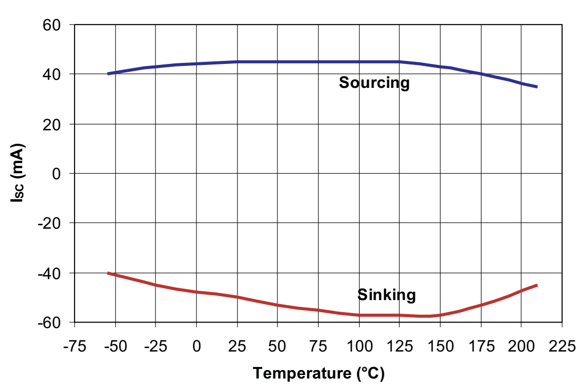


Figure 22.

SMALL-SIGNAL STEP RESPONSE (100 mV)

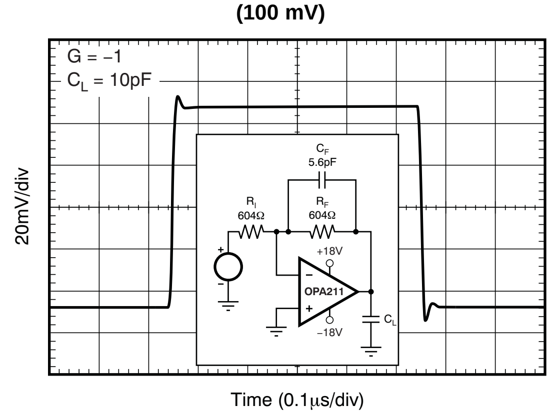


Figure 23.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE (100 mV)

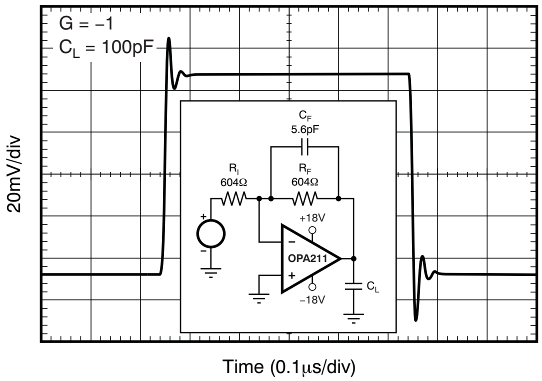


Figure 24.

SMALL-SIGNAL STEP RESPONSE (100 mV)

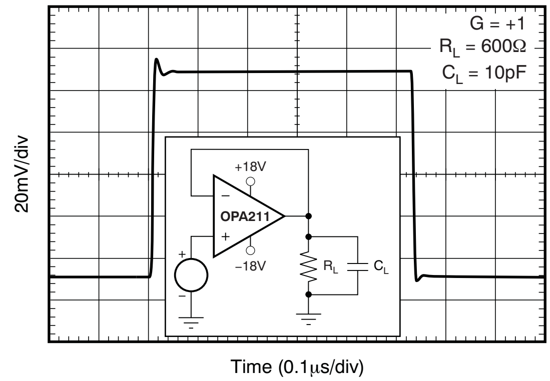


Figure 25.

SMALL-SIGNAL STEP RESPONSE (100 mV)

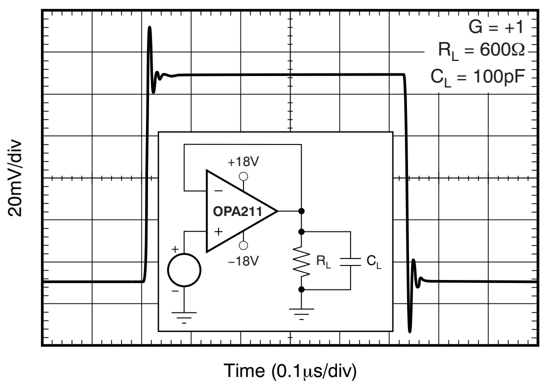


Figure 26.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

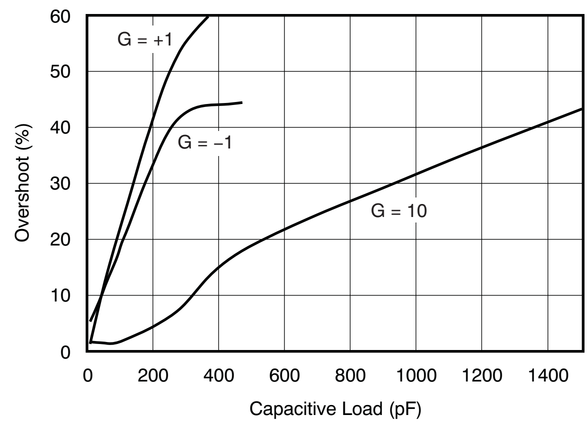


Figure 27.

LARGE-SIGNAL STEP RESPONSE

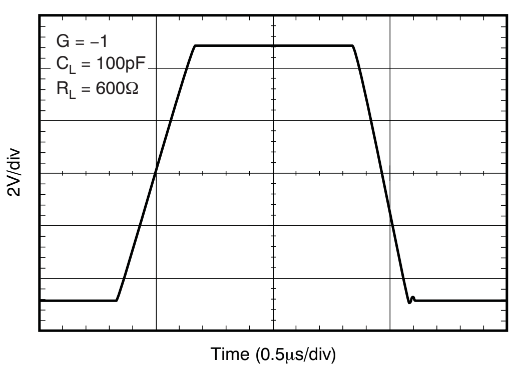


Figure 28.

LARGE-SIGNAL STEP RESPONSE

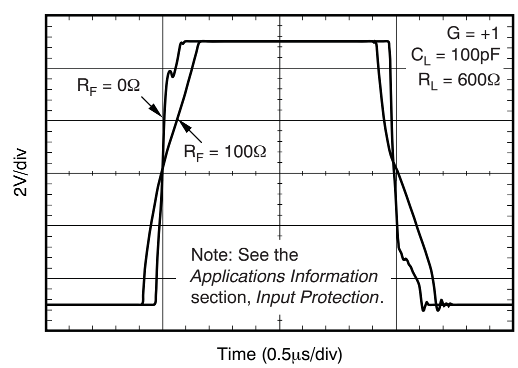


Figure 29.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

LARGE-SIGNAL POSITIVE SETTLING TIME ($10\ V_{PP}$, C_L = 100 pF)

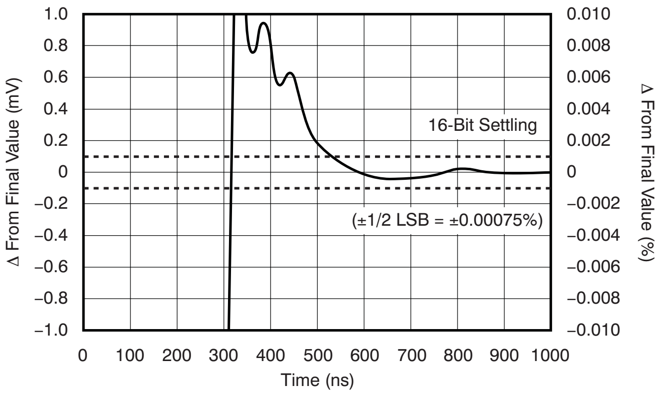


Figure 30.

LARGE-SIGNAL POSITIVE SETTLING TIME ($10\ V_{PP}$, C_L = 10 pF)

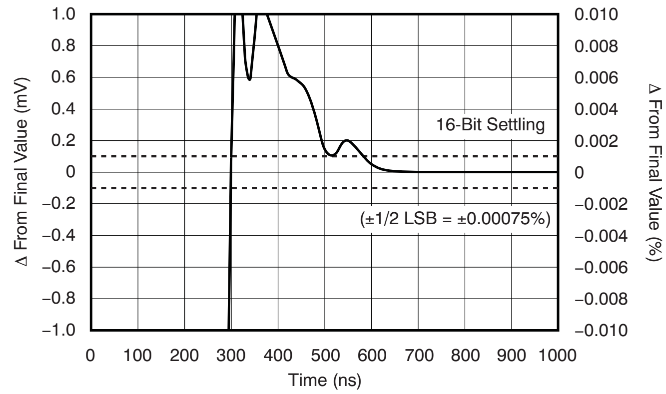


Figure 31.

LARGE-SIGNAL NEGATIVE SETTLING TIME ($10\ V_{PP}$, C_L = 100 pF)

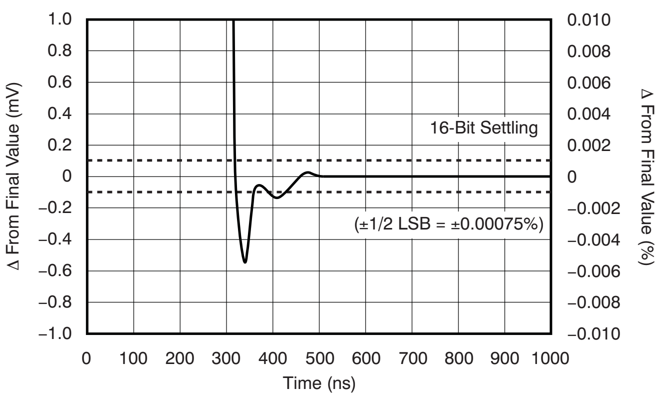


Figure 32.

LARGE-SIGNAL NEGATIVE SETTLING TIME ($10\ V_{PP}$, C_L = 10 pF)

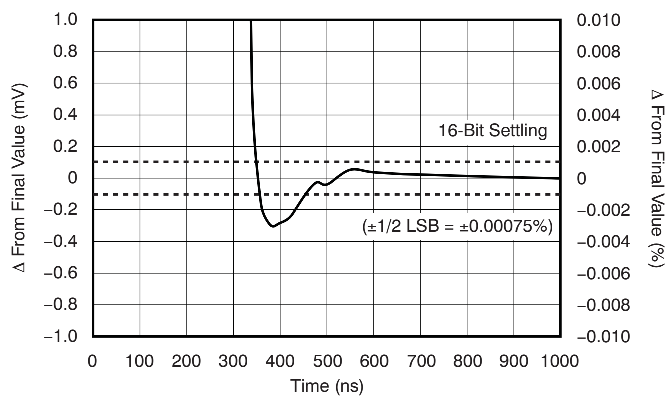
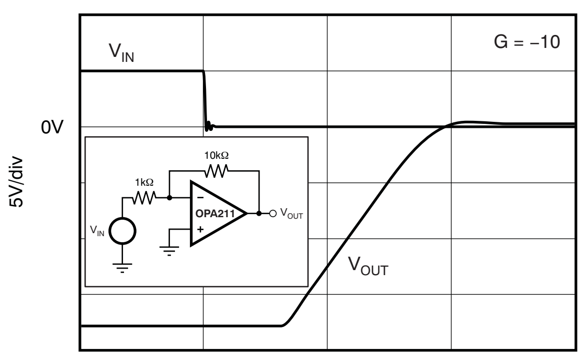


Figure 33.

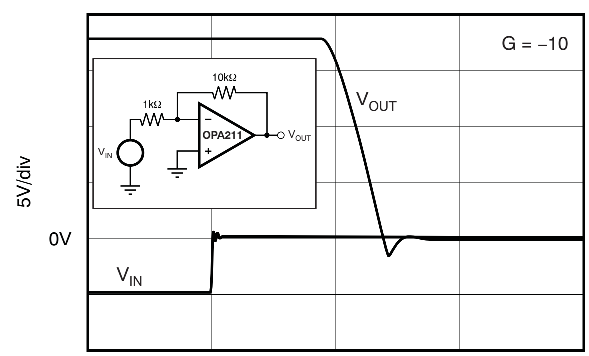
NEGATIVE OVERLOAD RECOVERY



Time (0.5µs/div)

Figure 34.

POSITIVE OVERLOAD RECOVERY



Time (0.5µs/div)

Figure 35.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±18 V, and R_L = 10 kΩ, unless otherwise noted.

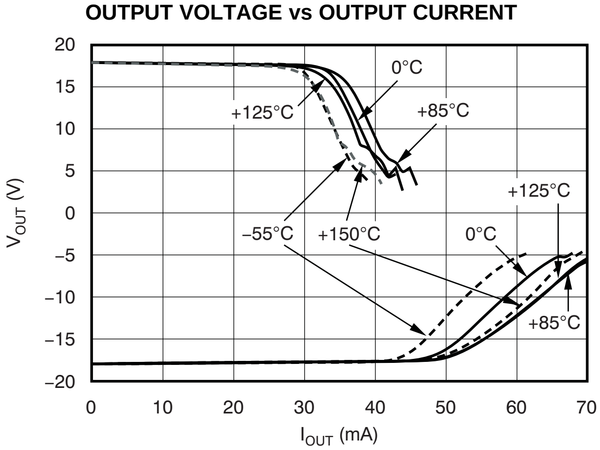


Figure 36.

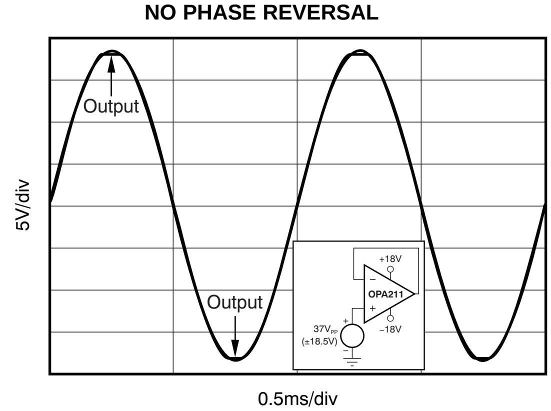


Figure 37.

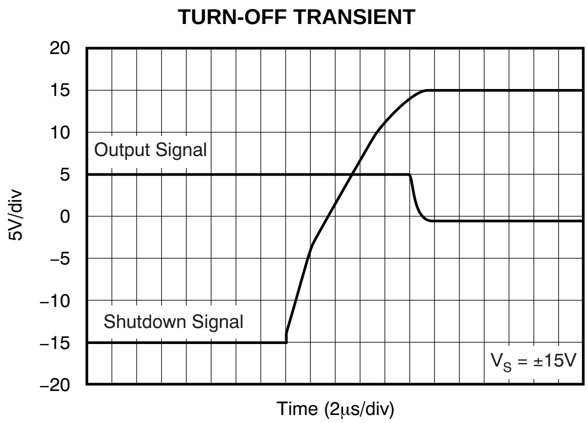


Figure 38.

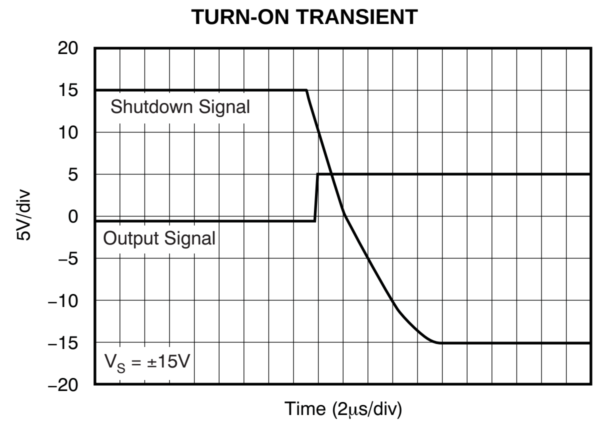


Figure 39.

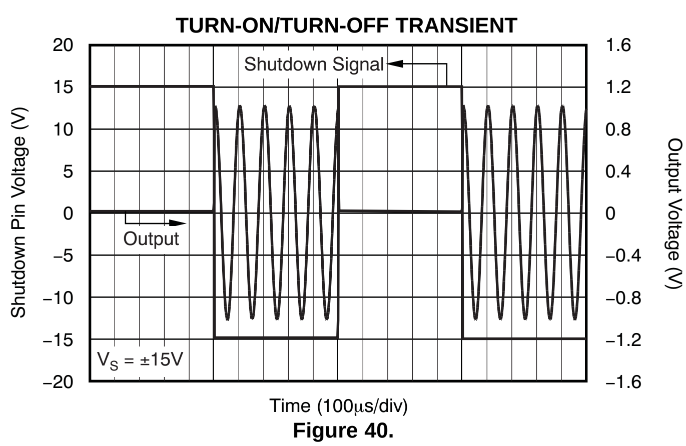


Figure 40.

APPLICATION INFORMATION

The OPA211 is a unity-gain stable, precision op amp with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate. Figure 41 shows a simplified schematic of the OPA211. This die uses a SiGe bipolar process and contains 180 transistors.

OPERATING VOLTAGE

OPA211 series op amps operate from ±2.25-V to ±18-V supplies while maintaining excellent performance. The OPA211 series can operate with as little as 4.5 V between the supplies and with up to 36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA211 series, power-supply voltages do not need to be equal. For example, the positive supply could be set to 25 V with the negative supply at –5 V or vice-versa.

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range, T_A = –55°C to 210°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

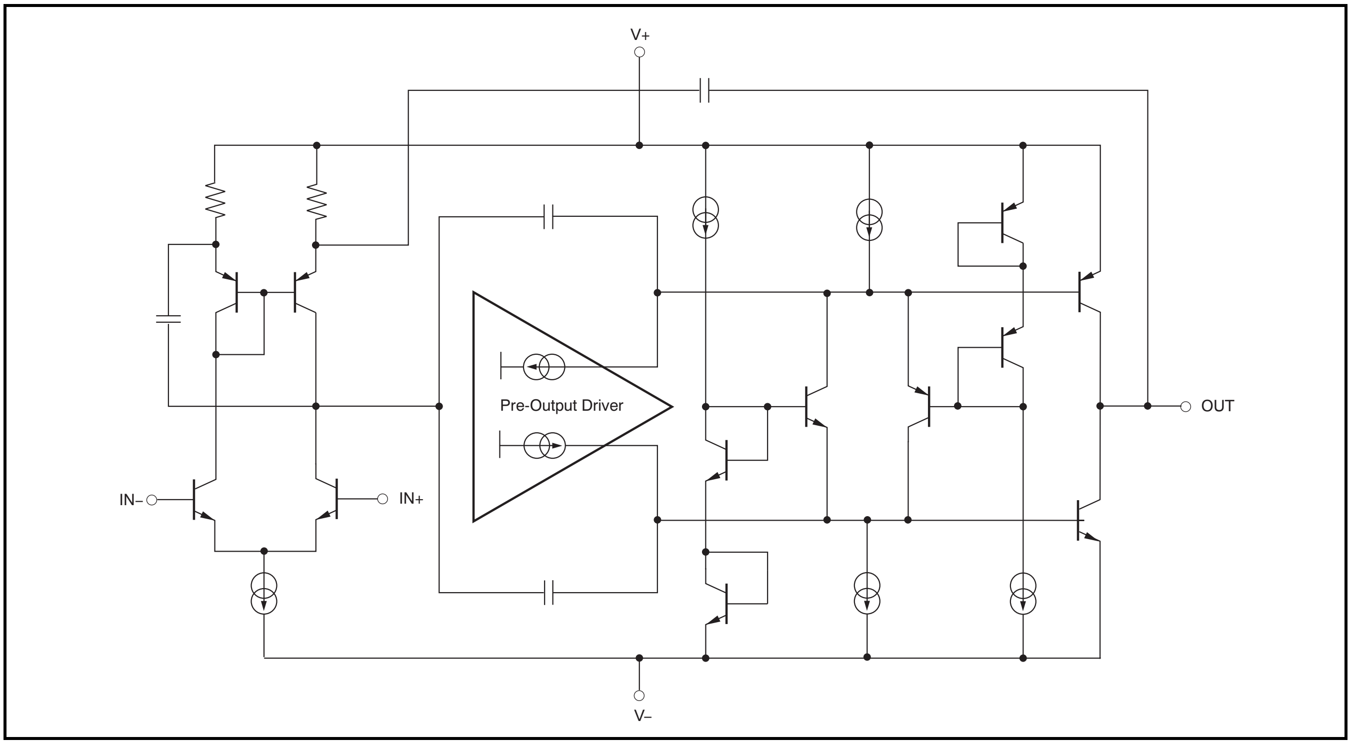


Figure 41. OPA211 Simplified Schematic

INPUT PROTECTION

The input terminals of the OPA211 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 42. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 29 of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA211, and is discussed in the *Noise Performance* section of this data sheet. Figure 42 shows an example implementing a current-limiting feedback resistor.

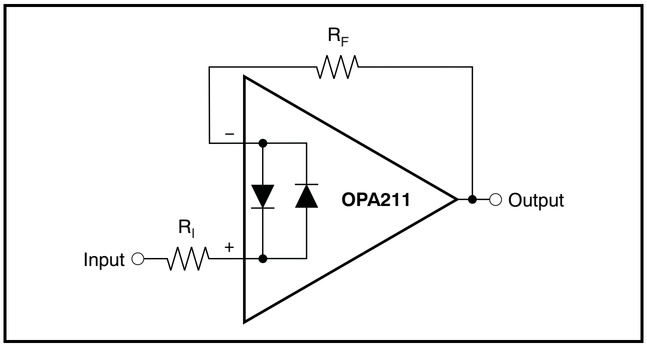


Figure 42. Pulsed Operation

NOISE PERFORMANCE

Figure 43 shows total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with total circuit noise calculated. The OPA211 has very low voltage noise, making it ideal for low source impedances (less than 2 kΩ). A similar precision op amp, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10 kΩ to 100 kΩ). Above 100 kΩ, a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation in Figure 43 is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, I_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38×10^{-23} J/K, and T is temperature in K.

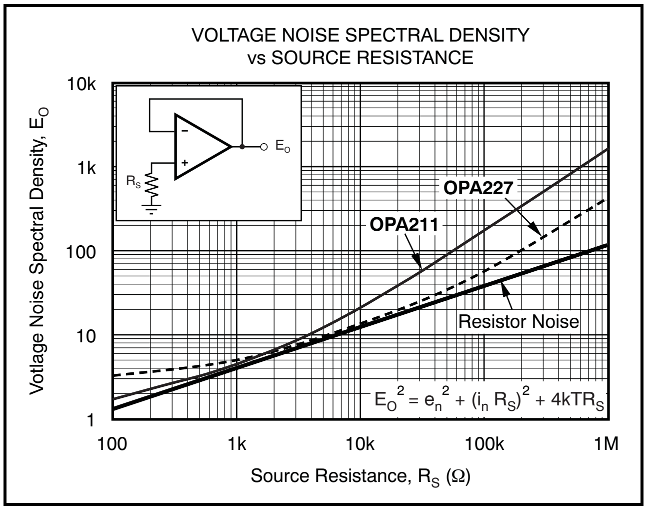


Figure 43. Noise Performance of the OPA211 and OPA227 in Unity-Gain Buffer Configuration

BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 43. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 43 depicts total noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 44 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

TOTAL HARMONIC DISTORTION MEASUREMENTS

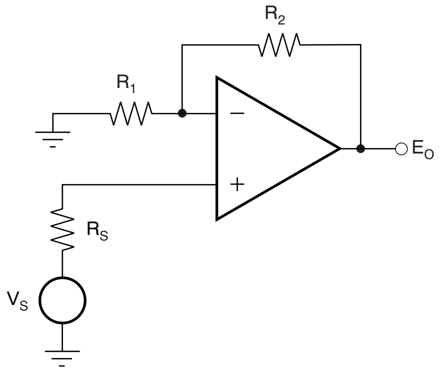
OPA211 series op amps have excellent distortion characteristics. THD + Noise is below 0.0001% (G = 1, V_O = 3 V_{RMS}) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600-Ω load.

The distortion produced by OPA211 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in Figure 45 can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 45 shows a circuit that causes the op amp distortion to be 101 times greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

Noise in Noninverting Gain Configuration



Noise at the output:

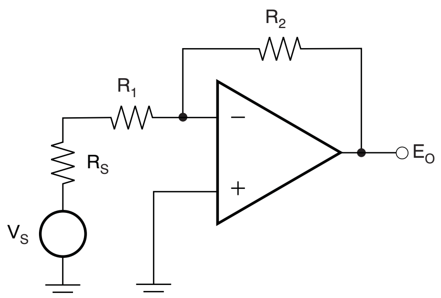
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_nR_2)^2 + e_S^2 + (i_nR_S)^2\left(1 + \frac{R_2}{R_1}\right)^2$$

$$\text{Where } e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right) = \text{thermal noise of } R_S$$

$$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right) = \text{thermal noise of } R_1$$

$$e_2 = \sqrt{4kTR_2} = \text{thermal noise of } R_2$$

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_nR_2)^2 + e_S^2$$

$$\text{Where } e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right) = \text{thermal noise of } R_S$$

$$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right) = \text{thermal noise of } R_1$$

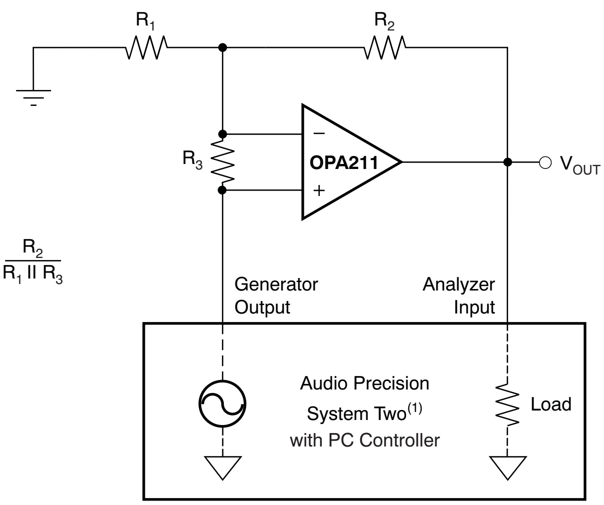
$$e_2 = \sqrt{4kTR_2} = \text{thermal noise of } R_2$$

For the OPA211 series op amps at 1kHz, $e_n = 1.1\text{nV}/\sqrt{\text{Hz}}$ and $i_n = 1.7\text{pA}/\sqrt{\text{Hz}}$.

Figure 44. Noise Calculation in Gain Configurations

$$\text{Signal Gain} = 1 + \frac{R_2}{R_1}$$

$$\text{Distortion Gain} = 1 + \frac{R_2}{R_1 \text{ II } R_3}$$



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω

Figure 45. Distortion Test Circuit

ELECTRICAL OVERSTRESS

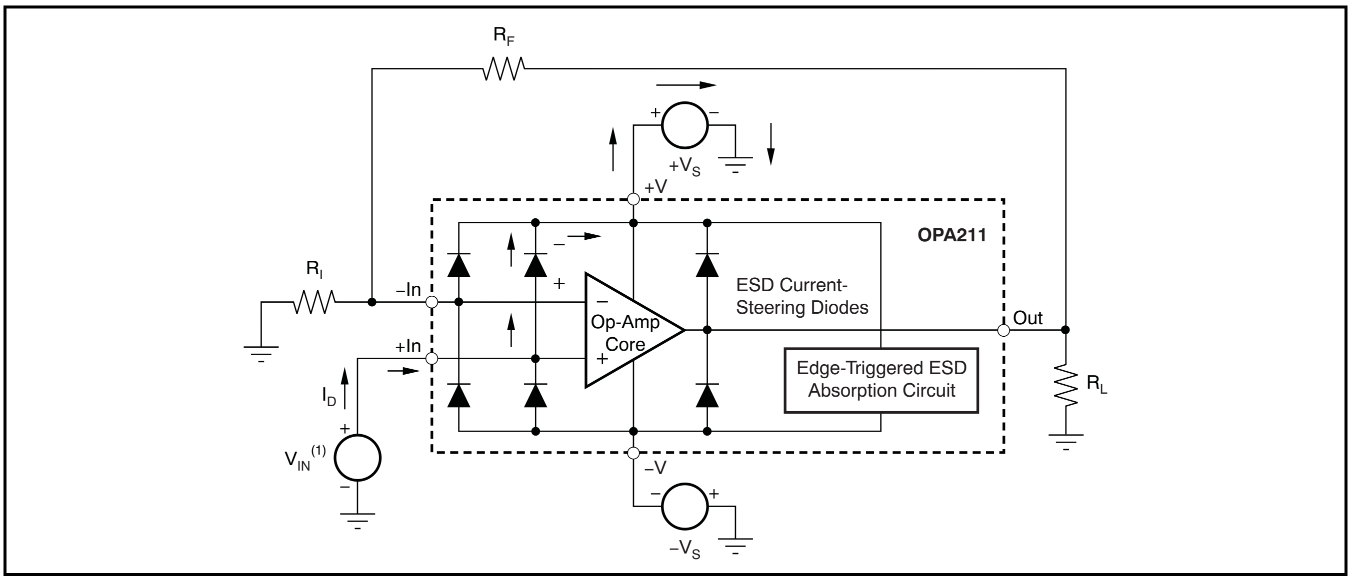
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 46 illustrates the ESD circuits contained in the OPA211 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA211 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 46, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.



(1) $V_{IN} = +V_S + 500mV$.

Figure 46. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

Figure 46 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V_S can sink the current, one of the upper input steering diodes conducts and directs current to V_S. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while V_S and $-V_S$ are applied. If this event happens, a direct current path is established between the V_S and $-V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V_S and/or $-V_S$ are at 0 V. Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA211SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	
OPA211SKGD1	ACTIVE	XCEPT	KGD	0	400	TBD	Call TI	N / A for Pkg Type	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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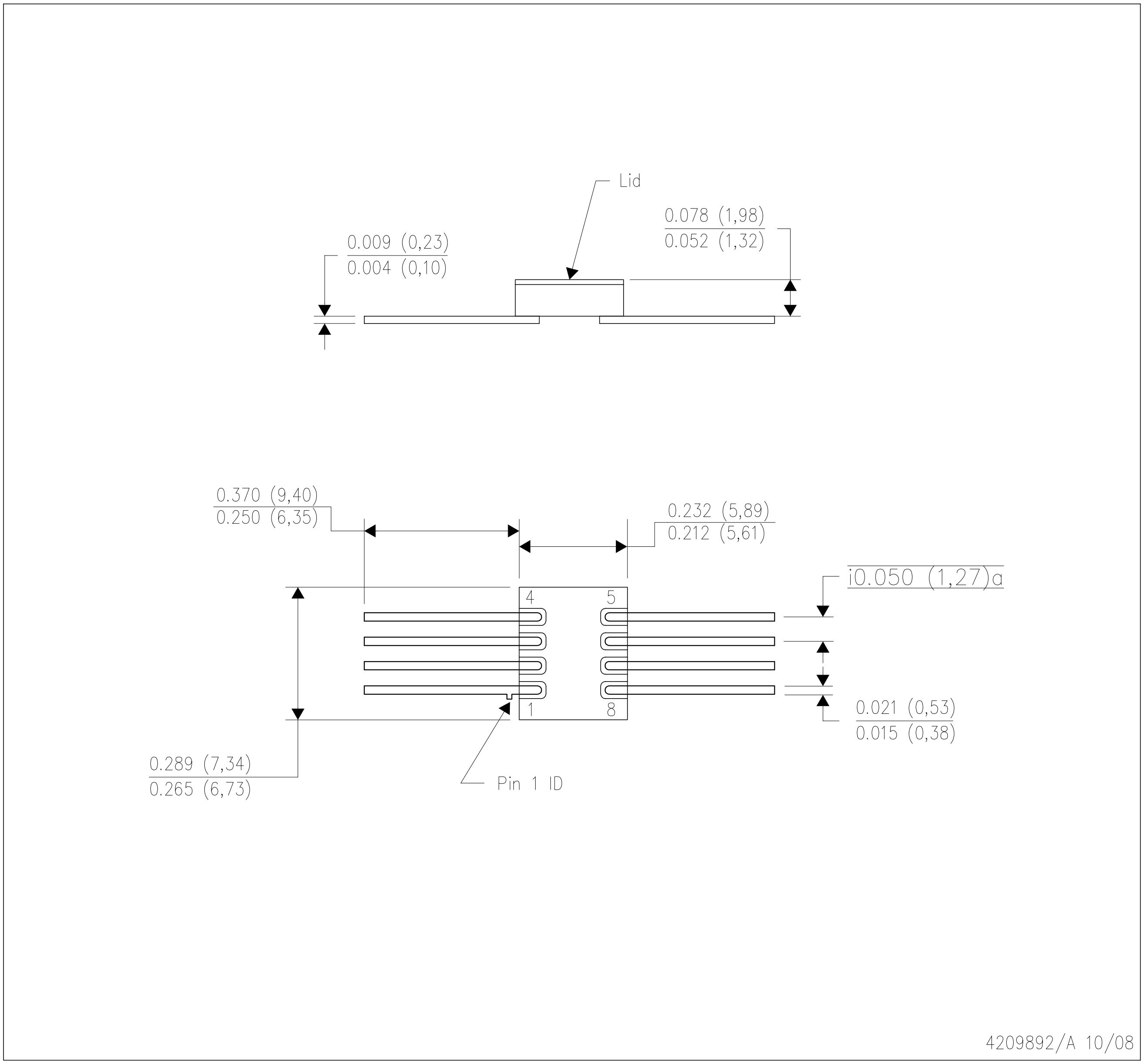
OTHER QUALIFIED VERSIONS OF OPA211-HT :

- Catalog: OPA211

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

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