



Reprogrammable CMOS  
PAL® Device

Features

- Advanced second generation PAL architecture
- Low power
  - 90 mA max. standard
  - 100 mA max. military
- CMOS EPROM technology for reprogrammability
- Variable product terms
  - 2 x (8 through 16) product terms
- User-programmable macrocell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
  - "15" commercial and industrial
    - 10 ns  $t_{CO}$
    - 10 ns  $t_s$
    - 15 ns  $t_{PD}$
    - 50 MHz

- "15" and "20" military
  - 10/15 ns  $t_{CO}$
  - 10/17 ns  $t_s$
  - 15/20 ns  $t_{PD}$
  - 50/31 MHz
- Up to 22 input terms and 10 outputs
- Enhanced test features
  - Phantom array
  - Top test
  - Bottom test
  - Preload
- High reliability
  - Proven EPROM technology
  - 100% programming and functional testing
- Windowed DIP, windowed LCC, DIP, LCC, PLCC available

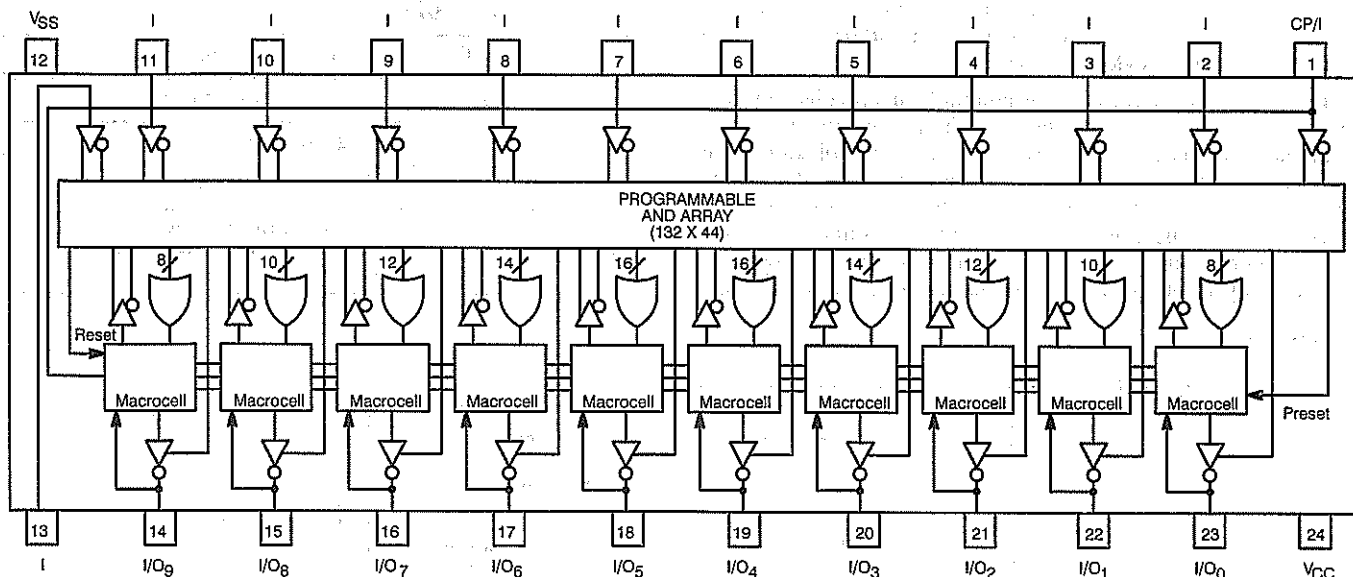
Functional Description

The Cypress PALC22V10B is a CMOS second-generation programmable logic array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "Programmable Macrocell."

The PALC22V10B is executed in a 24-pin 300-mil molded DIP, a 300-mil windowed cerDIP, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 22V10B is erased and can then be reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as "registered" or "combinatorial." Polarity of each output may also be

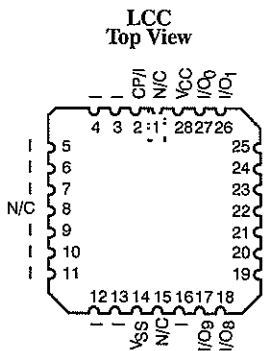
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Logic Block Diagram (PDIP/CDIP)

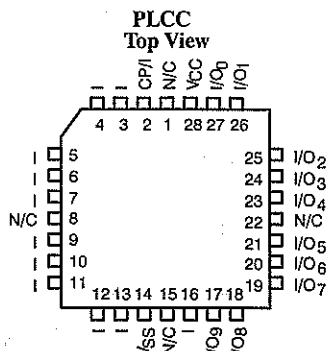


V10B-1

Pin Configurations



V10B-2



V10B-3

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### Functional Description (continued)

individually selected, allowing complete flexibility of output configuration. Further configurability is provided through "array" configurable "output enable" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

PALC22V10B features a "variable product term" architecture. There are 5 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure, the PALC22V10B is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unusable product terms and lower performance.

Additional features of the Cypress PALC22V10B include a synchronous preset and an asynchronous reset product term. These product terms are common to all macrocells, eliminating the need to dedicate standard product terms for initialization function. The device automatically resets upon power-up.

For testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage  $V_{PP}$ , which puts the output drivers in a high-impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A 0 on the I/O pin preloads the register with a 0 and a 1 preloads the register with a 1. The actual signal on the output pin will be the inversion of the input data. The data on the I/O pins is then removed, and pin 8 returned to a normal TTL voltage. Care should be exercised to power sequence the device properly.

The PALC22V10B featuring programmable macrocells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output and down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled using product terms. Any output pin may be permanently selected as an out-

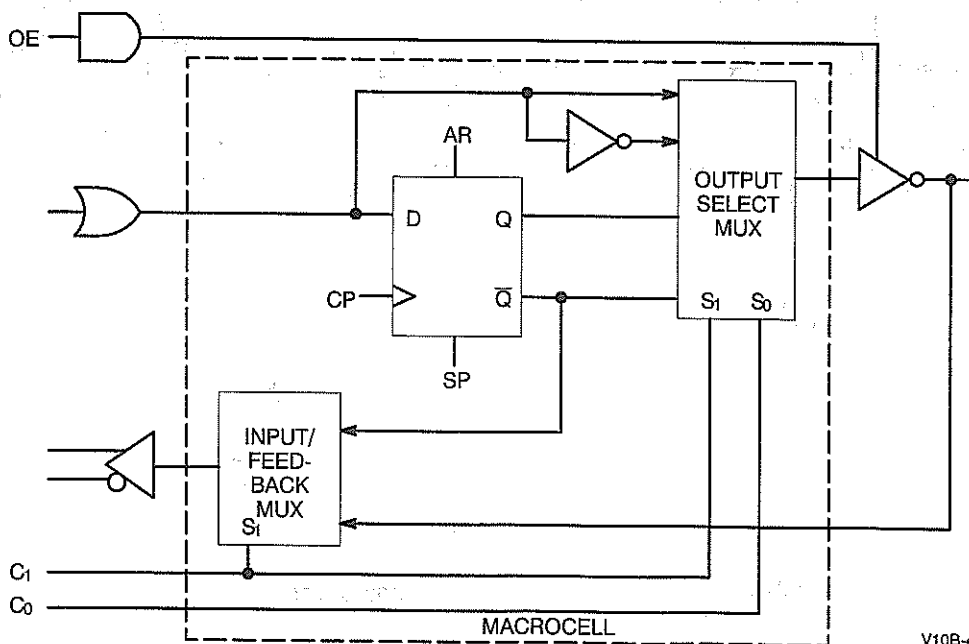
put or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macrocell. These macrocells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array, providing current status information to the array. This information is available for establishing the next result in applications such as control-state-machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macrocell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of a programmable logic.

Along with this increase in functional density, the Cypress PALC22V10B provides lower-power operation through the use of CMOS technology, increased testability with a register preload feature, and guaranteed AC performance through the use of a phantom array. This phantom array ( $P_0 - P_3$ ) and the "top test" and "bottom test" features allow the 22V10B to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PALC22V10B at incoming inspection before committing the device to a specific function through programming. Preload facilitates testing programmed devices by loading initial values into the registers.

Configuration Table 2

Registered/Combinatorial		
$C_1$	$C_0$	Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

### Macrocell



**Selection Guide**

Generic Part Number	I <sub>CC1</sub> mA		t <sub>PD</sub> ns		t <sub>S</sub> ns		t <sub>CO</sub> ns	
	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
22V10B-15	90	100	15	15	10	10	10	10
22V10B-20	-	100	-	20	-	17	-	15

**Maximum Rating**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12)	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V
Output Current into Outputs (Low)	16 mA
UV Exposure	7258 Wsec/cm <sup>2</sup>

DC Programming Voltage	13.0V
Latch-Up Current	>200 mA
Static Discharge Voltage (per MIL-STD 883 Method 3015)	>2001V

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +75°C	5V ±10%
Military <sup>[1]</sup>	- 55°C to +125°C	5V ±10%
Industrial	-40°C to +85°C	5V ±10%

**Electrical Characteristics Over the Operating Range<sup>[2]</sup>**

Parameters	Description	Test Conditions		Min.	Max.	Units
V <sub>OH1</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -3.2 mA	Com'l/Ind	2.4	V
			I <sub>OH</sub> = -2 mA	Mil		
V <sub>OH2</sub>	HIGH Level CMOS Output Voltage <sup>[3]</sup>	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> - 1.0V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 16 mA	Com'l/Ind	0.5	V
			I <sub>OL</sub> = 12 mA	Mil		
V <sub>IH</sub>	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[4]</sup>			2.0	V
V <sub>IL</sub>	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs <sup>[4]</sup>			0.8	V
I <sub>IX</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , V <sub>CC</sub> = Max.			-10	10 μA
I <sub>OZ</sub>	Output Leakage Current	V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>			-40	40 μA
I <sub>SC</sub>	Output Short Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[3,5]</sup>			-30	-90 mA
I <sub>CC1</sub>	Standby Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND Outputs Open for Unprogrammed Device	Com'l/Ind		90	mA
			Mil		100	mA
I <sub>CC2</sub>	Operating Power Supply Current	f <sub>toggle</sub> = F <sub>MAX</sub> <sup>[3]</sup> Device Programmed with Worst Case Pattern, Outputs Three-States	Com'l/Ind		90	mA
			Mil		100	mA

**Notes:**

- t<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

**Capacitance<sup>[3]</sup>**

Parameters	Description	Typical	Max.	Units
C <sub>IN</sub>	Input Capacitance	11		pF
C <sub>OUT</sub>	Output Capacitance	9		pF

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**PLDS**

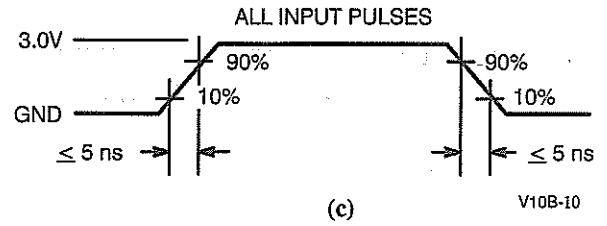
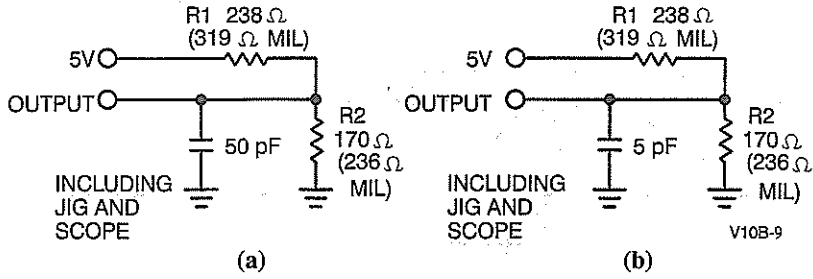
**Switching Characteristics PALC22V10<sup>[2, 6]</sup>**

Parameters	Description	Commercial & Industrial		Military		Military		Units
		B-15		B-15		B-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PD}$	Input to Output Propagation Delay <sup>[7]</sup>		15		15		20	ns
$t_{EA}$	Input to Output Enable Delay		15		15		20	ns
$t_{ER}$	Input to Output Disable Delay <sup>[8]</sup>		15		15		20	ns
$t_{CO}$	Clock to Output Delay <sup>[9]</sup>		10		10		15	ns
$t_S$	Input or Feedback Set-Up Time	10		10		17		ns
$t_H$	Input Hold Time	0		0		0		ns
$t_P$	External Clock Period ( $t_{CO} + t_S$ )	20		20		32		ns
$t_{WH}$	Clock Width HIGH <sup>[3]</sup>	6		6		12		ns
$t_{WL}$	Clock Width LOW <sup>[3]</sup>	6		6		12		ns
$f_{MAX1}$	External Maximum Frequency ( $1/(t_{CO} + t_S)$ ) <sup>[10]</sup>	50.0		50		31.2		MHz
$f_{MAX2}$	Data Path Maximum Frequency ( $1/(t_{WH} + t_{WL})$ ) <sup>[3, 11]</sup>	83.3		83.3		41.6		MHz
$f_{MAX3}$	Internal Feedback Maximum Frequency ( $1/(t_{CF} + t_S)$ ) <sup>[12]</sup>	80.0		80		33.3		MHz
$t_{CF}$	Register Clock to Feedback Input <sup>[13]</sup>		2.5		2.5		13	ns
$t_{AW}$	Asynchronous Reset Width	15		15		20		ns
$t_{AR}$	Asynchronous Reset Recovery Time	10		12		20		ns
$t_{AP}$	Asynchronous Reset to Registered Output Delay		20		20		25	ns
$t_{SPR}$	Synchronous Preset Recovery Time	10		20		20		ns
$t_{PR}$	Power-Up Reset Time <sup>[14]</sup>	1.0		1.0		1.0		$\mu$ s

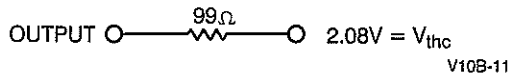
**Notes:**

- Part (a) of AC Test Loads and Waveforms used for all parameters except  $t_{EA}$ ,  $t_{ER}$ ,  $t_{PZX}$ , and  $t_{PXZ}$ . Part (b) of AC Test Loads and Waveforms used for  $t_{EA}$ ,  $t_{ER}$ ,  $t_{PZX}$  and  $t_{PXZ}$ .
- This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction which may be subtracted from  $t_{PD}$  for cases in which fewer outputs are changing state per access cycle.
- This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below  $V_{OH\ min.}$  or a previous LOW level has risen to 0.5 volts above  $V_{OL\ max.}$  Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
- This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction which may be subtracted from  $t_{CO}$  for cases in which fewer outputs are changing state per access cycle.
- This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
- This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
- This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
- This parameter is calculated from the clock period at  $f_{MAX}$  internal ( $1/f_{MAX3}$ ) as measured (see Note 12 above) minus  $t_S$ .
- The registers in the PALC22V10B has been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in  $V_{CC}$  must be monotonic and the timing constraints depicted in Power-Up Reset Waveform must be satisfied.

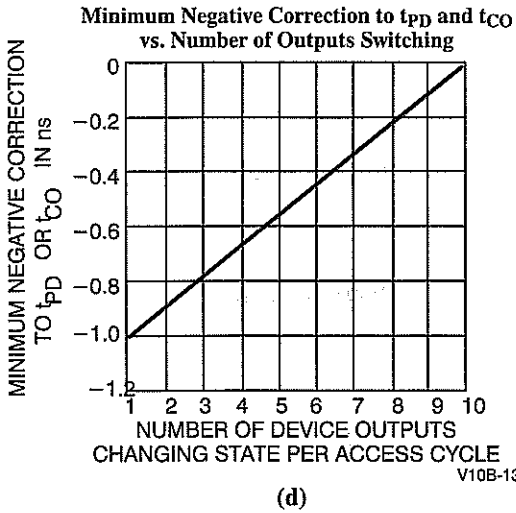
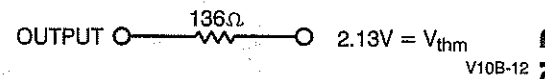
AC Test Loads and Waveforms (Commercial)



Equivalent to: THEVENIN EQUIVALENT (Commercial)



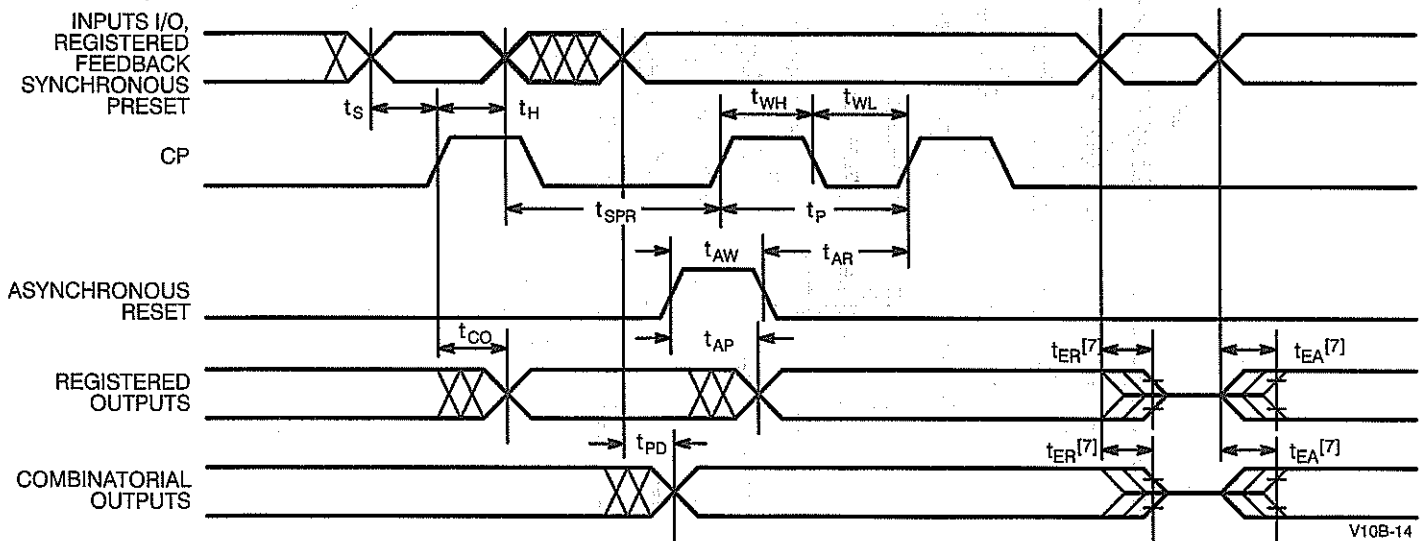
Equivalent to: THEVENIN EQUIVALENT (Military)



Parameter	V <sub>X</sub>	Output Waveform—Measurement Level
t <sub>BR</sub> (-)	1.5V	V <sub>OH</sub> 0.5V V <sub>X</sub> V10B-5
t <sub>BR</sub> (+)	2.6V	V <sub>OL</sub> 0.5V V <sub>X</sub> V10B-6
t <sub>EA</sub> (+)	V <sub>thc</sub>	V <sub>X</sub> 0.5V V <sub>OH</sub> V10B-7
t <sub>EA</sub> (-)	V <sub>thc</sub>	V <sub>X</sub> 0.5V V <sub>OL</sub> V10B-8

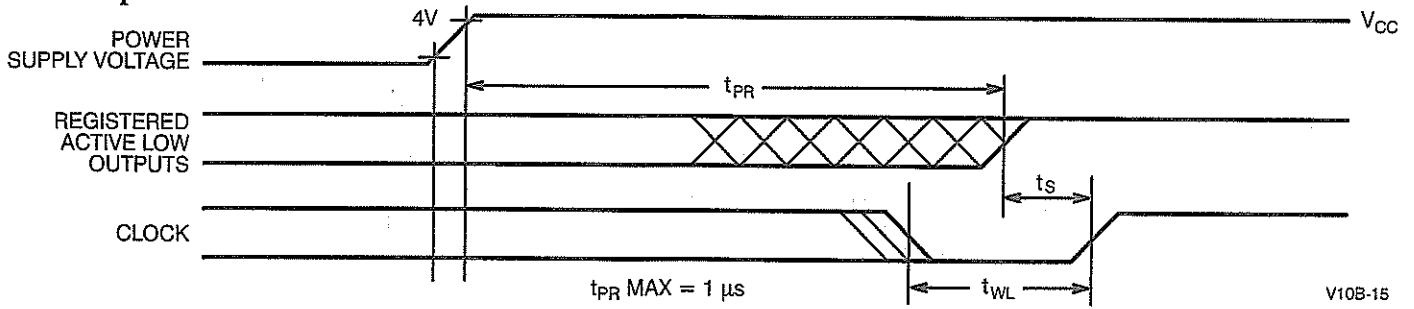
(e) Test Waveforms

Switching Waveform

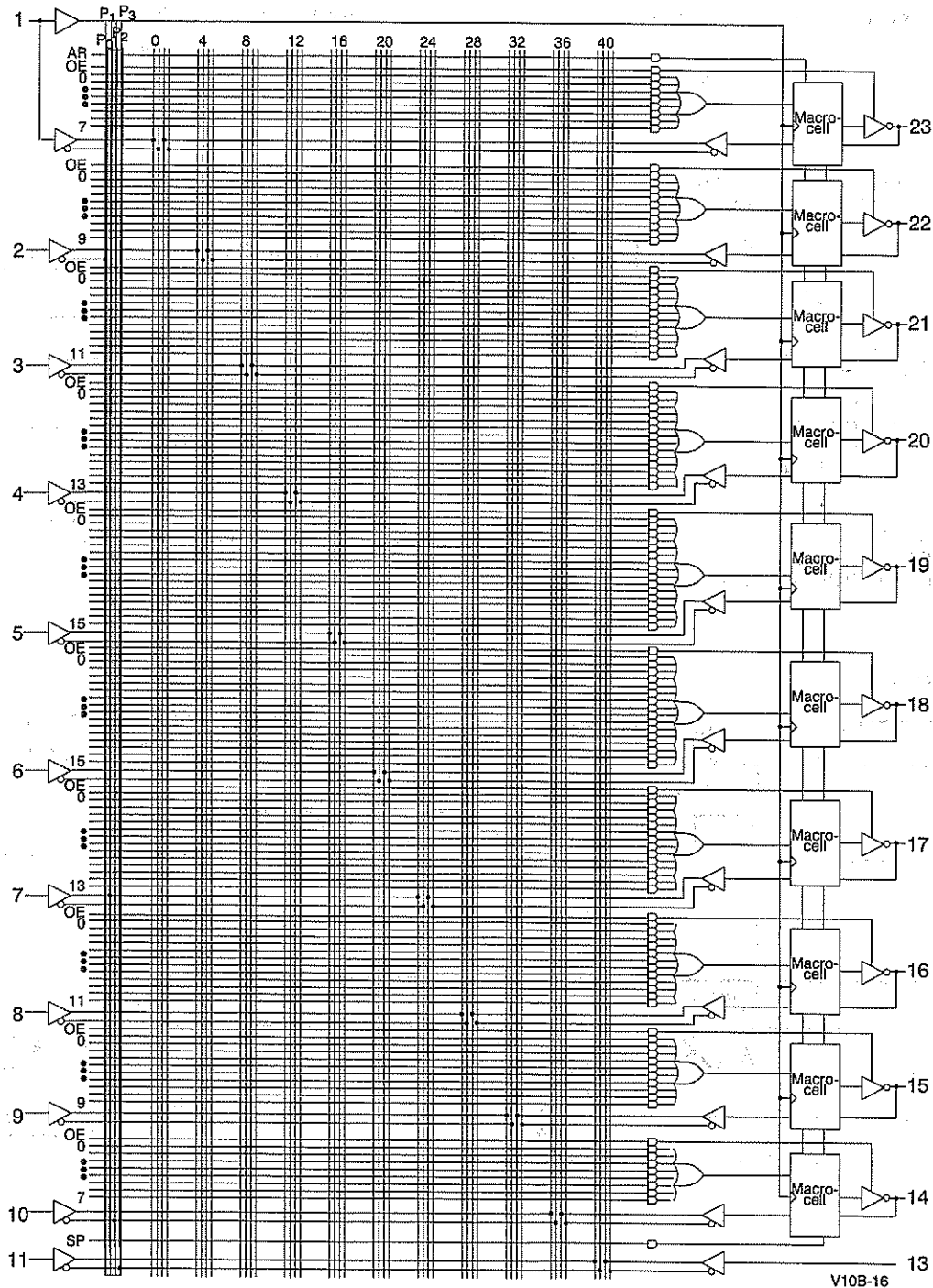


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Power-Up Reset Waveform<sup>[14]</sup>



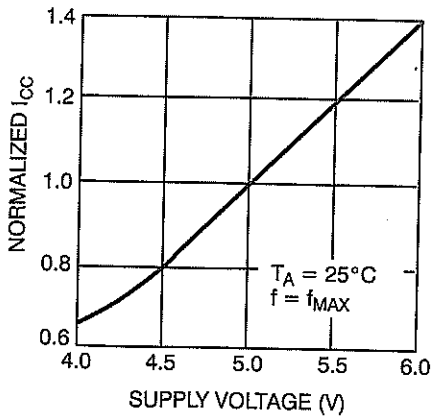
Functional Logic Diagram for PALC22V10B



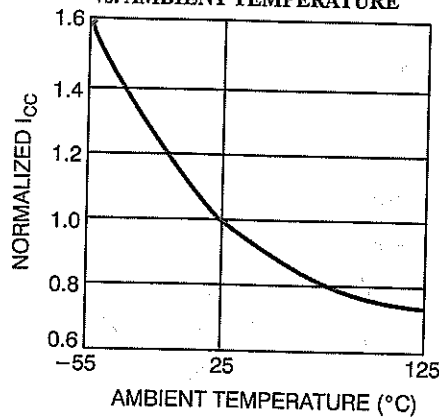
Typical DC and AC Characteristics

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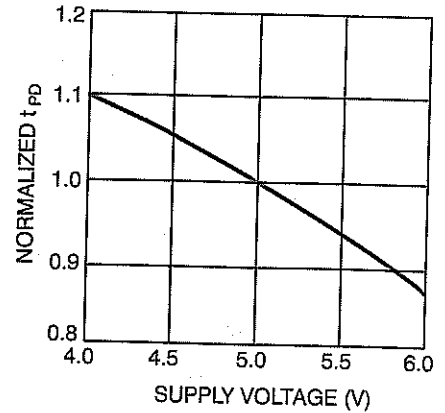
NORMALIZED STANDBY SUPPLY CURRENT ( $I_{CC1}$ ) vs. SUPPLY VOLTAGE



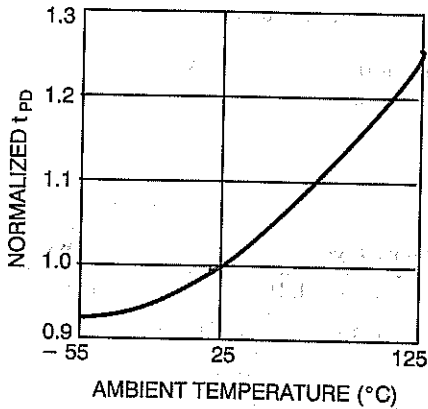
NORMALIZED STANDBY SUPPLY CURRENT ( $I_{CC1}$ ) vs. AMBIENT TEMPERATURE



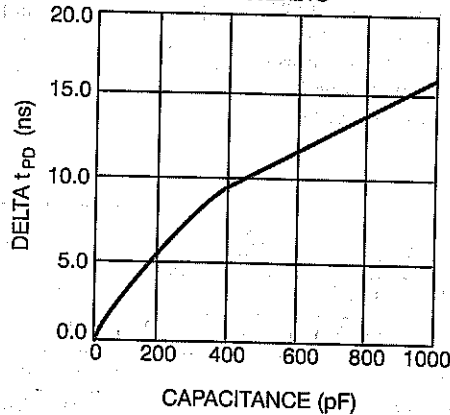
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



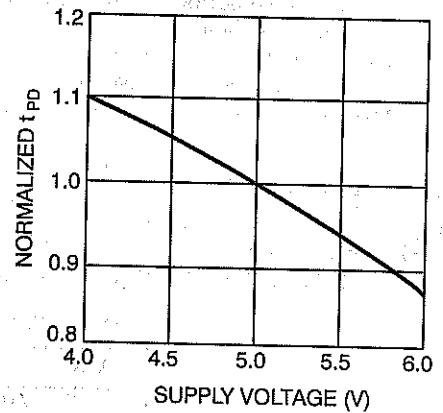
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



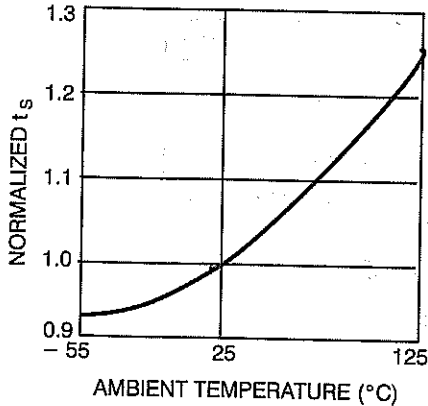
DELTA PROPAGATION TIME vs. OUTPUT LOADING



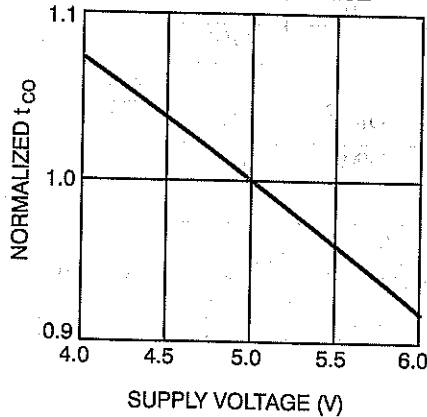
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



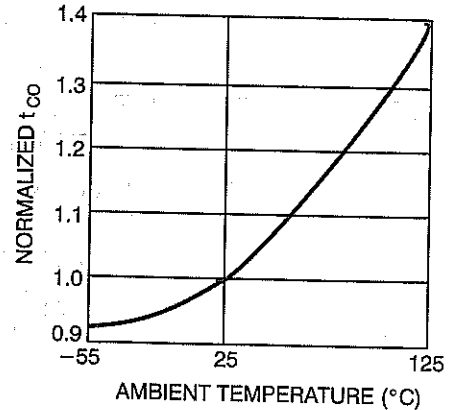
NORMALIZED SET-UP TIME vs. TEMPERATURE

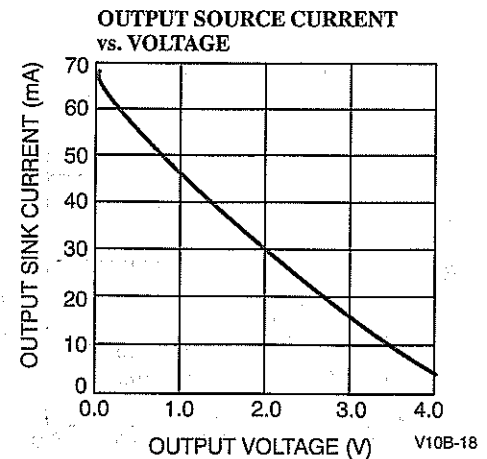
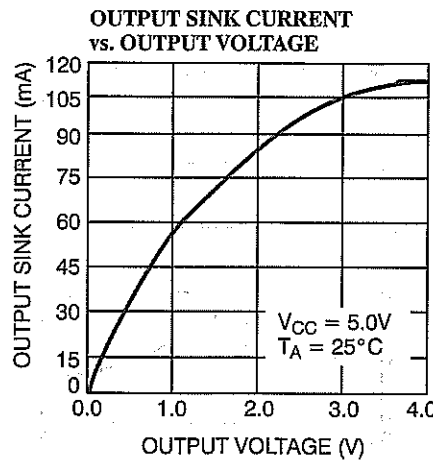
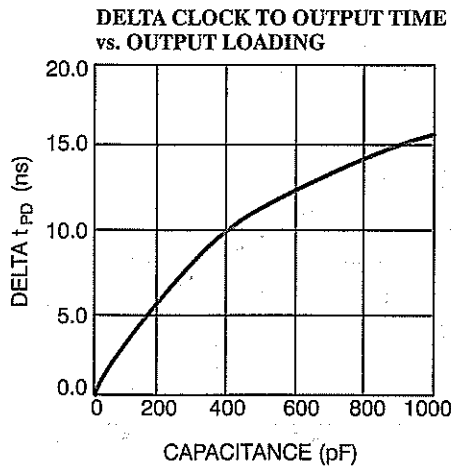


NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



**Typical DC and AC Characteristics (continued)**

**Erasure Characteristics**

Wavelengths of light less than 4000 Angstroms begin to erase the PALC22V10B. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs that may cause "blank" check failures or "verify errors" when programming windowed parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure would be approximately 35 minutes. The PALC22V10B needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

**Ordering Information**

I <sub>CC</sub> (mA)	t <sub>PD</sub> (ns)	t <sub>S</sub> (ns)	t <sub>CO</sub> (ns)	Ordering Code	Package Name	Package Type	Operating Range
90	15	10	10	PALC22V10B-15PC/PI	P13	24-Lead (300-Mil) Molded DIP	Commercial/ Industrial
				PALC22V10B-15WC/WI	W14	24-Lead (300-Mil) Windowed CerDIP	
				PALC22V10B-15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10B-15HC	H64	28-Pin Windowed Leaded Chip Carrier	
100	15	10	10	PALC22V10B-15DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10B-15WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
				PALC22V10B-15HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PALC22V10B-15LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10B-15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PALC22V10B-15KMB	K73	24-Lead Rectangular Cerpack	
100	20	17	15	PALC22V10B-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10B-20WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
				PALC22V10B-20HMB	H64	28-Pin Windowed Leaded Chip Carrier	
				PALC22V10B-20LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10B-20QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
				PALC22V10B-20KMB	K73	24-Lead Rectangular Cerpack	



**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing****DC Characteristics**

Parameters	Subgroups
$V_{OH}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{IH}$	1, 2, 3
$V_{IL}$	1, 2, 3
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{CC}$	1, 2, 3

**Switching Characteristics**

Parameters	Subgroups
$t_{pD}$	7, 8, 9, 10, 11
$t_{CO}$	7, 8, 9, 10, 11
$t_s$	7, 8, 9, 10, 11
$t_{fj}$	7, 8, 9, 10, 11

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