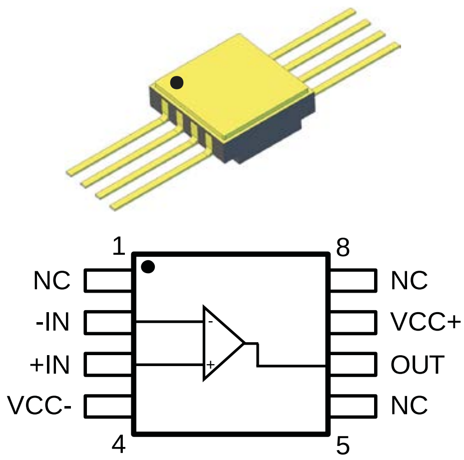
RHF43B

Rad-hard precision bipolar single operational amplifier

Datasheet - production data

Ceramic Flat-8



The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package

Features

- Rail-to-rail output
- Bandwidth: 8 MHz gain at 16 V
- Low input offset voltage: 100 µV typ
- Supply current: 2.2 mA typ
- Operating from 3 to 16 V
- Input bias current: 30 nA typ
- ESD internal protection ≥ 2 kV
- Latch-up immunity: 200 mA
- ELDRS free up to 300 krad
- SEL immune at 120 MEV.cm^2/mg

Applications

- Space probes and satellites
- Defense systems
- Scientific instrumentation
- Nuclear systems

Description

The RHF43B is a precision, bipolar operational amplifier available in a ceramic Flat-8 package and in die form. In addition to its low offset voltage, rail-to-rail feature, and wide supply voltage, the RHF43B is designed for increased tolerance to radiation. Its intrinsic ELDRS-free rad-hard design allows this product to be used in space applications and in applications operating in harsh environments.

Table 1: Device summary

Parameter	RHF43BK1	RHF43BK-01V
SMD (1)	—	5962F06237
Quality level	Engineering model	QML-V flight
Package Mass	Flat-8 0.45 g	
EPPL (2)	—	Yes
Temp. range	-55 °C to 125 °C	

Notes:

(1)SMD: supplier manufacturing drawing

(2)EPPL = ESA preferred part list

Contact your ST sales office for information on the specific conditions for products in die form and QML-Q versions.

This is information on a product in full production.

Contents

1 Absolute maximum ratings and operating conditions

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	18	V
V_{id}	Differential input voltage [2]	±1.2	
V_{in}	Input voltage range [3]	V_{DD} - 0.3 to 16	
I_{in}	Input current	45	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Maximum junction temperature	150	
R_{thja}	Thermal resistance junction to ambient area [4][5]	125	°C/W
R_{thjc}	Thermal resistance junction to case [4][5]	40	
ESD	HBM: human body model [6]	2	kV
	Latch-up immunity	200	mA
	Lead temperature (soldering, 10 s)	260	°C

Notes:

(1) The supply voltage is defined as the difference between the voltages applied on the VCC and VDD pins.

(2) The differential voltage is the non-inverting input terminal with respect to the inverting input terminal

(3) The magnitude of the input and output voltage must never exceed V_{CC} + 0.3 V.

(4) Short-circuits can cause excessive heating and destructive dissipation.

(5) R_{th} are typical values.

(6) Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

Table 3: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 16	V
V_{icm}	Common-mode input voltage	V_{DD} to V_{CC}	
T_{oper}	Operating free-air temperature range	-55 to 125	°C

2 Electrical characteristics

Table 4: 16 V supply: VCC = 16 V, VDD = 0 V, load to VCC/2 (unless otherwise specified)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
DC performance							
I_{CC}	Supply current	No load	125 °C			2.9	mA
			25 °C		2.5	2.9	
			-55 °C			2.9	
V_{io}	Offset voltage	Vicm = Vcc/2	125 °C	-500		500	µV
			25 °C	-300	100	300	
			-55 °C	-500		500	
DV_{io}	Input offset voltage drift				1		µV/°C
I_{ib}	Input bias current	Vicm = Vcc/2	125 °C	-100		100	nA
			25 °C	-60	30	60	
			-55 °C	-100		100	
DI_{ib}	Input offset current temperature drift	Vicm = Vcc/2			100		pA/°C
I_{io}	Input offset current	Vicm = Vcc/2	125 °C	-35		35	nA
			25 °C	-15	1	15	
			-55 °C	-35		35	
R_{in}	Differential input resistance between in+ and in-		25 °C		0.16		MΩ
	Input resistance between in+ (or in-) and GND				2000		
C_{in}	Differential input capacitance between in+ and in-		25°C		8		pF
	Input capacitance between in+ (or in-) and GND				2		
CMR	Common mode rejection ratio	0 < Vicm < 16 V	125 °C	72			dB
			25 °C	72	110		
			-55 °C	72			
SVR	Supply voltage rejection ratio	3 V < Vcc < 16 V, Vicm = Vcc/2	125 °C	80			
			25 °C	90	120		
			-55 °C	80			
A_{VD}	Large signal voltage gain	Vout = 0.5 V to 15.5 V, RL = 1 kΩ, 0 < Vicm < 16 V	125 °C	60			
			25 °C	74	85		
			-55 °C	60			
V_{OH}	High level output voltage	RL = 1 kΩ	125 °C	15.6			V
			25 °C	15.7	15.8		
			-55 °C	15.6			
		RL = 10 kΩ	125 °C	15.8			

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage	RL = 10 kΩ	25 °C	15.9	15.96		V
			-55 °C	15.8			
V_{OL}	Low level output voltage	RL = 1 kΩ	125 °C			0.3	
			25 °C		0.1	0.2	
			-55 °C			0.3	
		RL = 10 kΩ	125 °C			0.1	
			25 °C		0.04	0.06	
			-55 °C			0.1	
I_{out}	Output sink current	Vout = Vcc	125 °C	15			mA
			25 °C	20	30		
			-55 °C	15			
	Output source current	Vout = Vcc	125 °C	10			
			25 °C	15	25		
			-55 °C	10			
AC performance							
GBP	Gain bandwidth product	f = 100 kHz, RL = 1 kΩ, CL = 100 pF	125 °C	3.5			MHz
			25 °C	6	8		
			-55 °C	3.5			
F_u	Unity gain frequency	RL = 1 kΩ, CL = 100 pF	25 °C		5		
ϕm	Phase margin	Gain = 5, RL = 1 kΩ, CL = 100 pF	25 °C		50		Degrees
SR	Slew rate	RL = 1 kΩ, CL = 100 pF	125 °C	1.7			V/µs
			25 °C	2	3		
			-55 °C	1.7			
e_n	Equivalent input noise voltage	f = 1 kHz	25 °C		7.5		nV/√Hz
i_n	Equivalent input noise current	f = 1 kHz	25 °C		1		pA/√Hz
THD+e_n	Total harmonic distortion + noise	Vout = (Vcc - 1 V)/5, Gain = -5.1, Vicm = Vcc/2	25 °C		0.01		%

Table 5: 3 V supply: VCC = 3 V, VDD = 0 V, load to VCC/2 (unless otherwise specified)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
DC performance							
I_{CC}	Supply current	No load	125 °C			2.6	mA
			25 °C		2.2	2.6	
			-55 °C			2.6	
V_{io}	Offset voltage	Vicm = Vcc/2	125 °C	-500		500	µV
			25 °C	-300	100	300	
			-55 °C	-500		500	
DV_{io}	Input offset voltage drift				1		µV/°C
I_{ib}	Input bias current	Vcc = 4 V, Vicm = Vcc/2	125 °C	-100		100	nA
			25 °C	-60	30	60	
			-55 °C	-100		100	
DI_{ib}	Input offset current temperature drift	Vcc = 4 V, Vicm = Vcc/2			100		pA/°C
I_{io}	Input offset current	Vcc = 4 V, Vicm = Vcc/2	125 °C	-35		35	nA
			25 °C	-15	1	15	
			-55 °C	-35		35	
R_{in}	Differential input resistance between in+ and in-		25 °C		0.16		MΩ
	Input resistance between in+ (or in-) and GND				2000		
C_{in}	Differential input capacitance between in+ and in-		25°C		8		pF
	Input capacitance between in+ (or in-) and GND				2		
CMR	Common mode rejection ratio	0 < Vicm < 3 V	125 °C	72			dB
			25 °C	72	90		
			-55 °C	72			
A_{VD}	Large signal voltage gain	Vout = 0.5 V to 2.5 V, RL = 1 kΩ, 0 < Vicm < 3 V	125 °C	60			
			25 °C	74	85		
			-55 °C	60			
V_{OH}	High level output voltage	RL = 1 kΩ	125 °C	2.8			V
			25 °C	2.9	2.95		
			-55 °C	2.8			
		RL = 10 kΩ	125 °C	2.9			
			25 °C	2.94	2.98		
			-55 °C	2.9			
V_{OL}	Low level output voltage	RL = 1 kΩ	125 °C			0.2	
			25 °C		0.05	0.1	
			-55 °C			0.2	

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	RL = 10 kΩ	125 °C			0.1	V
			25 °C		0.02	0.06	
			-55 °C			0.1	
I_{out}	Output sink current	Vout = Vcc	125 °C	15			mA
			25 °C	20	30		
			-55 °C	15			
	Output source current	Vout = Vcc	125 °C	10			
			25 °C	15	25		
			-55 °C	10			
AC performance							
GBP	Gain bandwidth product	f = 100 kHz, RL = 1 kΩ, CL = 100 pF	125 °C	3.5			MHz
			25 °C	6	7.5		
			-55 °C	3.5			
F_u	Unity gain frequency	RL = 1 kΩ, CL = 100 pF	25 °C		5		
ϕm	Phase margin	Gain = 5, RL = 1 kΩ, CL = 100 pF	25 °C		50		Degrees
SR	Slew rate	RL = 1 kΩ, CL = 100 pF	125 °C	1.7			V/μs
			25 °C	2	2.7		
			-55 °C	1.7			
e_n	Equivalent input noise voltage	f = 1 kHz	25 °C		7		nV/√Hz
i_n	Equivalent input noise current	f = 1 kHz	25 °C		0.8		pA/√Hz
THD+e_n	Total harmonic distortion + noise	Vout = (Vcc - 1 V)/5, Gain = -5.1, Vicm = Vcc/2	25 °C		0.01		%

Figure 1: Input offset voltage distribution

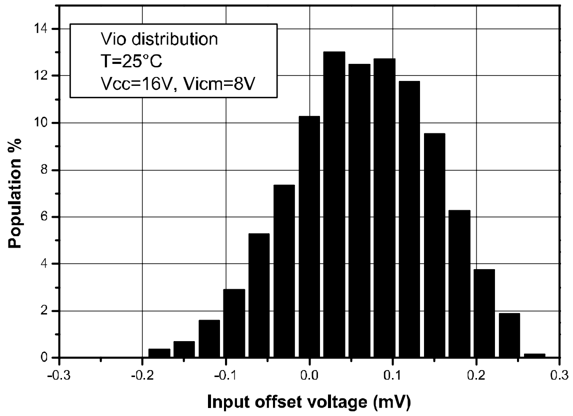


Figure 2: Input bias current vs. supply voltage

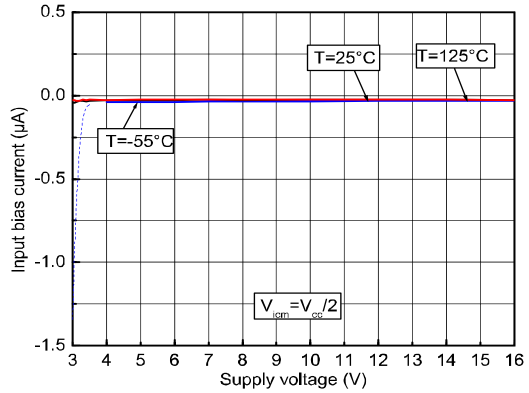


Figure 3: Input bias current vs Vicm at VCC = 3 V

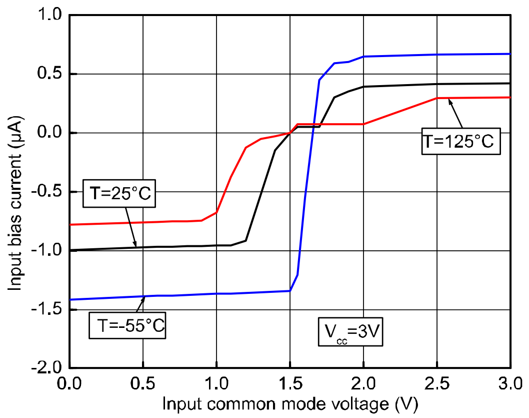


Figure 4: Input bias current vs Vicm at VCC = 4 V

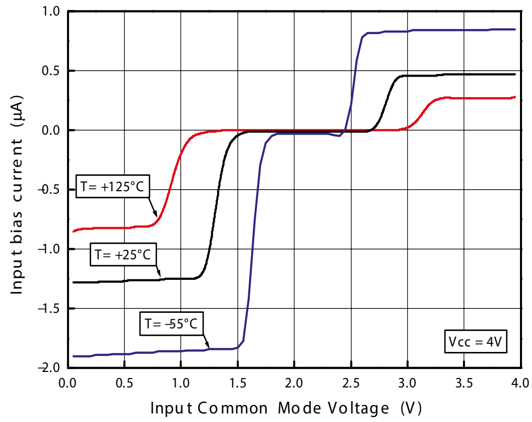


Figure 5: Input bias current vs. Vicm at VCC = 16 V

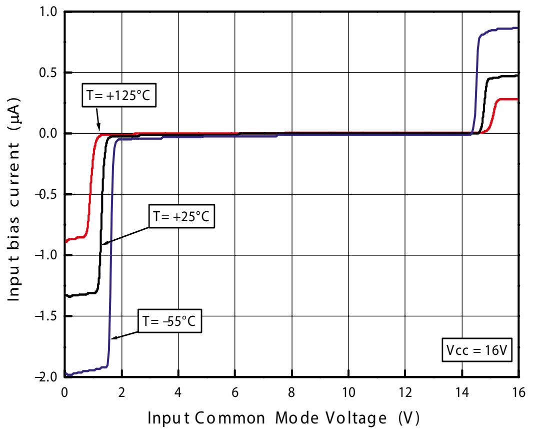


Figure 6: Gain bandwidth product vs. Vicm at VCC = 10 V

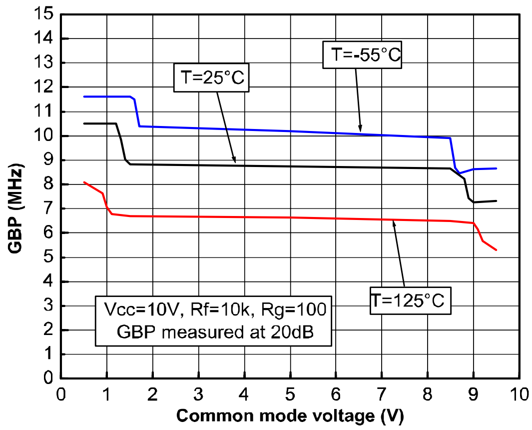


Figure 7: Supply current vs. Vicm in follower configuration at VCC = 3 V

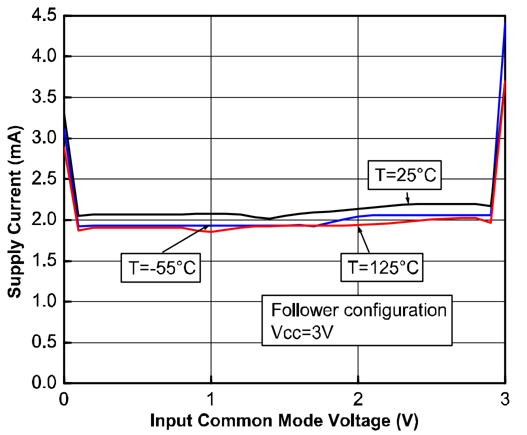


Figure 8: Supply current vs. Vicm in follower configuration at VCC = 16 V

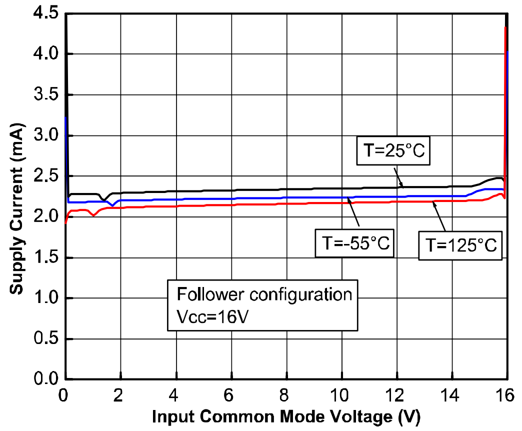


Figure 9: Supply current vs. supply voltage at Vicm = VCC/2

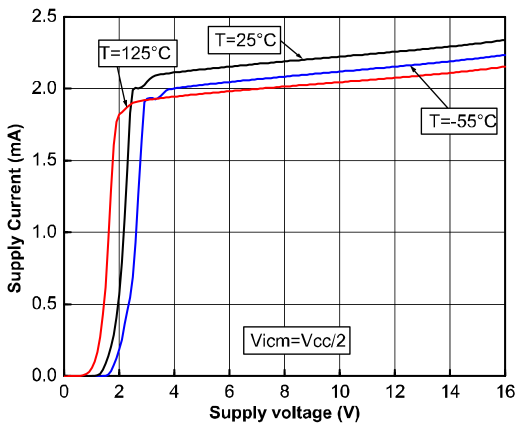


Figure 10: Output current vs. supply voltage at Vicm = VCC/2

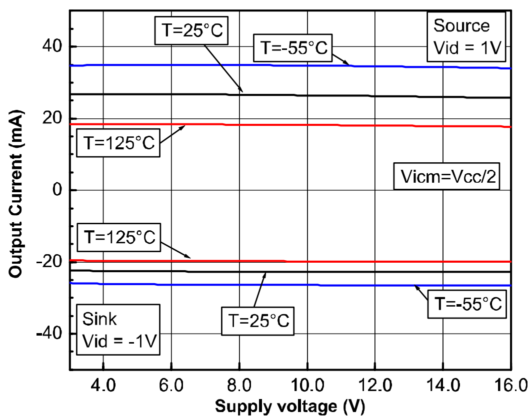


Figure 11: Output current vs. output voltage at VCC = 3 V

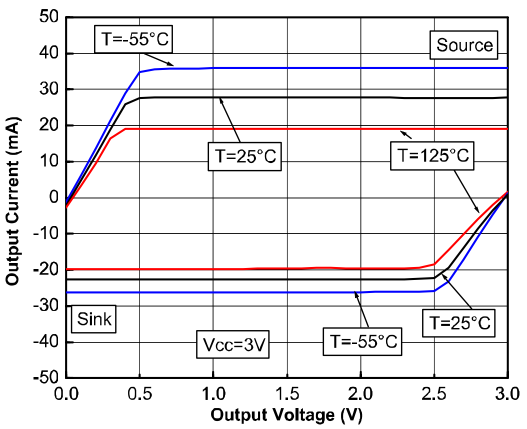


Figure 12: Output current vs. output voltage at VCC = 16 V

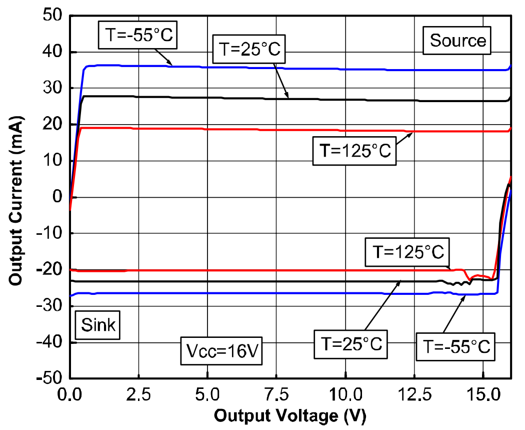


Figure 13: Differential input voltage vs. output voltage at VCC = 3 V

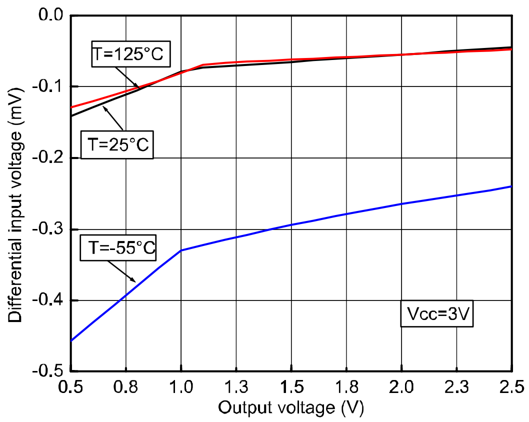


Figure 14: Differential input voltage vs. output voltage at VCC = 16 V

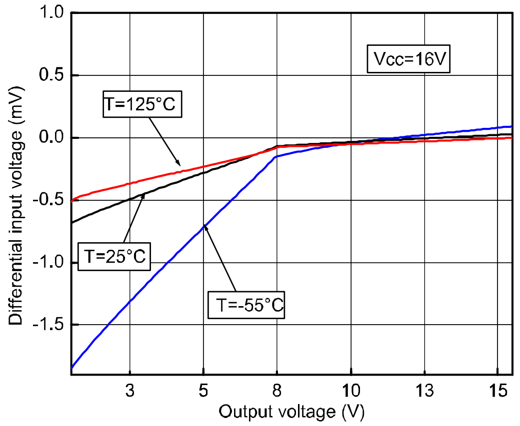


Figure 15: Noise vs. Vicm at VCC= 10 V

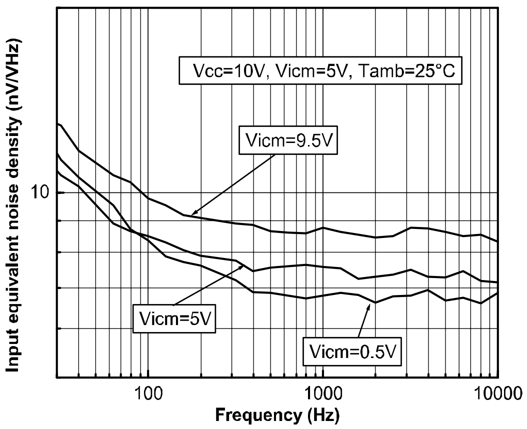


Figure 16: Noise vs. frequency at VCC= 3 V and VCC = 16 V

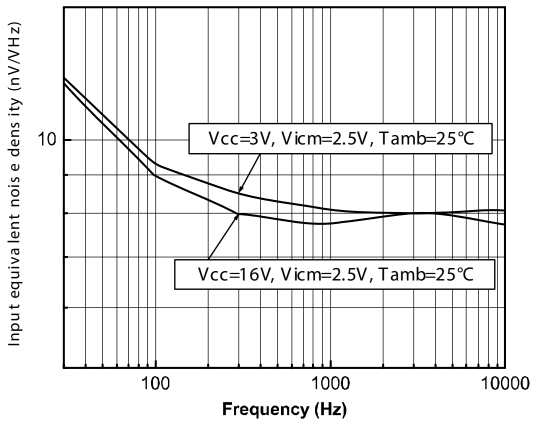


Figure 17: Voltage gain and phase vs. frequency at Vicm = 1.5 V and Vcc = 3 V

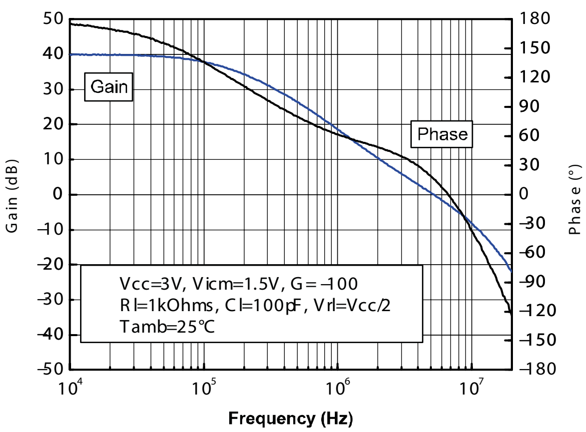


Figure 18: Voltage gain and phase vs. frequency at Vicm = 2.5 V and Vcc = 3 V

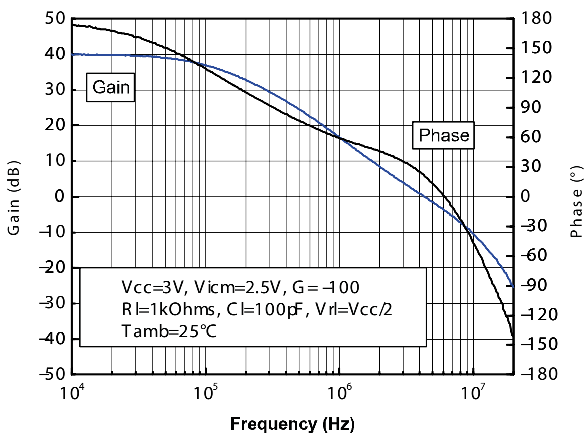


Figure 19: Voltage gain and phase vs. frequency at Vicm = 0.5 V and Vcc = 3 V

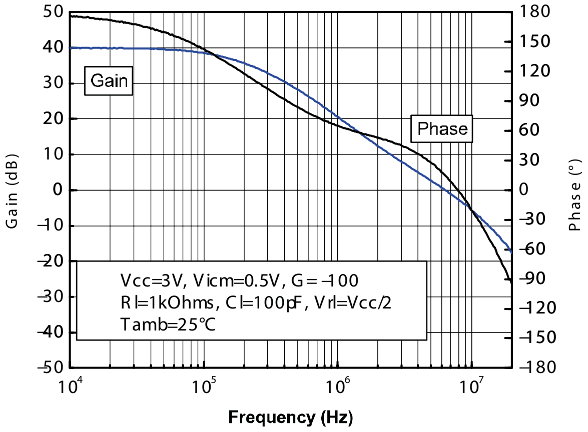


Figure 20: Voltage gain and phase vs. frequency at Vicm = 8 V and Vcc = 16 V

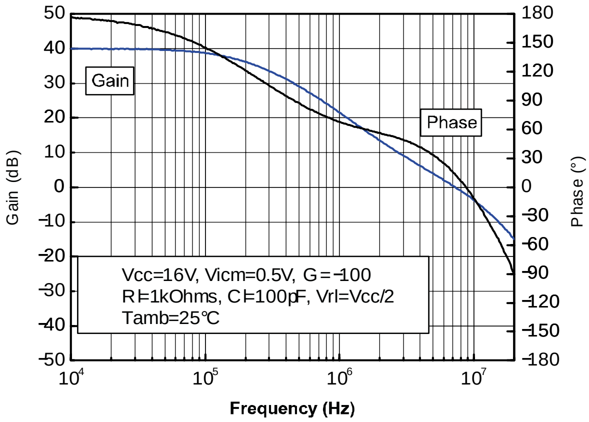


Figure 21: Voltage gain and phase vs. frequency at Vicm = 15.5 V and Vcc = 16 V

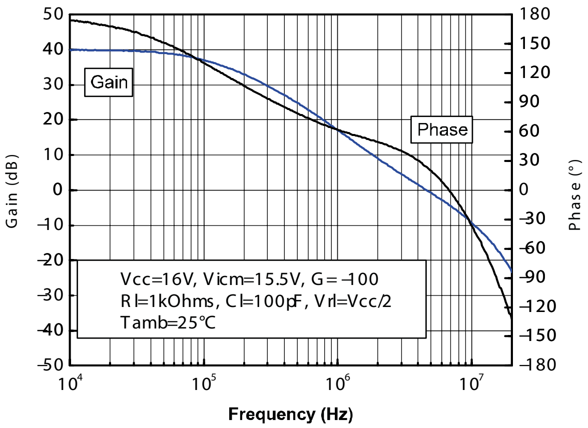


Figure 22: Voltage gain and phase vs. frequency at Vicm = 0.5 V and Vcc = 16 V

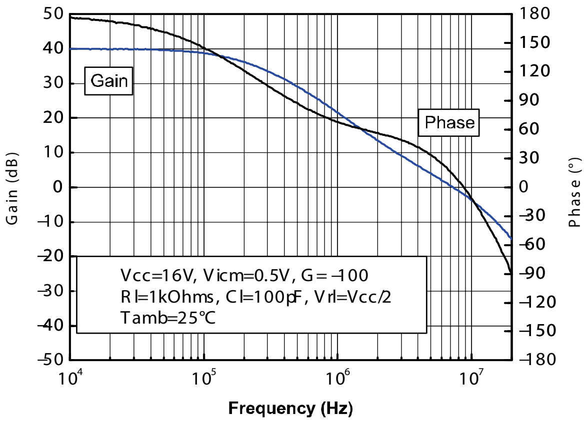


Figure 23: Inverting large signal pulse response at VCC = 3 V, 25°C

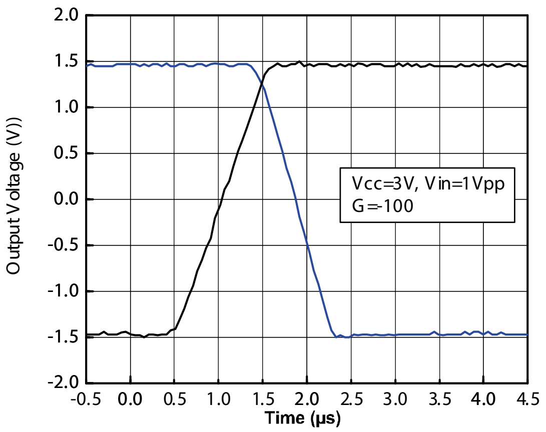
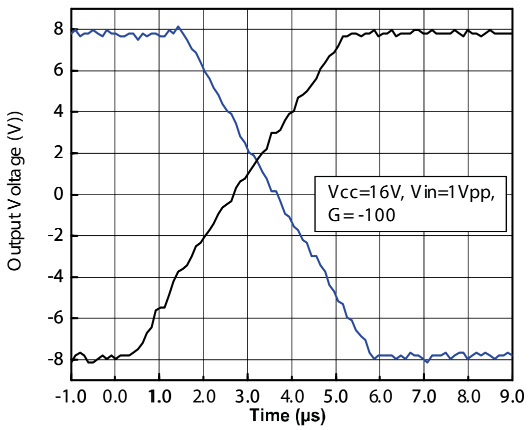


Figure 24: Inverting large signal pulse response at VCC = 16 V, 25°C



3 Radiations

3.1 Introduction

Table 6 summarizes the radiation performance of the RHF43B.

Table 6: Radiations

Type	Features		Value	Unit
TID	High-dose rate		300	krad
	Low-dose rate		300	
	ELDRS		300	
Heavy ions	SEL immunity (at 125 °C) up to:		110	MeV.cm²/mg
	SET characterized	Inverting	LET_{th} = 1	MeV.cm²/mg
			σ = 2.00E-03	cm²/device
		Non-inverting	LET_{th} = 0	MeV.cm²/mg
			σ = 1.00E-03	cm²/device
		Subtracting	LET_{th} = 0	MeV.cm²/mg
			σ = 2.00E-03	cm²/device

3.2 Total ionizing dose (TID)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MILSTD-883 test method 1019 specification.

The RHF43B is RHA QML-V qualified, and is tested and characterized in full compliance with the MIL-STD-883 specification. It using a mixed bipolar and CMOS technology and is tested both below 10 mrad/s (low dose rate) and between 50 and 300 rad/s (high dose rate).

- The ELDRS characterization is performed in qualification only on both biased and unbiased parts, on a sample of ten units from two different wafer lots.
- Each wafer lot is tested at high-dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

3.3 Heavy ions

The heavy ion trials are performed on qualification lots only. No additional test is performed.

4 Achieving good stability at low gain

At low frequencies, the RHF43B can be used in a low gain configuration as shown in *Figure 25*. At lower frequencies, the stability is not affected by the value of the gain, which can be set close to 1 V/V (0 dB), and is reduced to its simplest expression G1 = 1+Rfb/Rg. Therefore, an R-C cell is added in the gain network so that the gain is increased (up to 5) at higher frequencies (where the stability of the amplifier could be affected). At higher frequencies, the gain becomes G2 = 1+Rfb/(Rg//R).

Figure 25: Low gain configuration

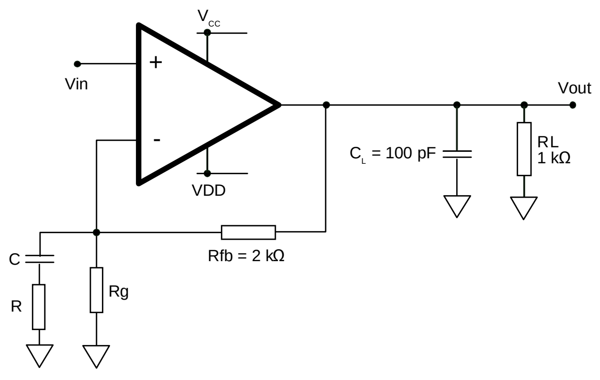
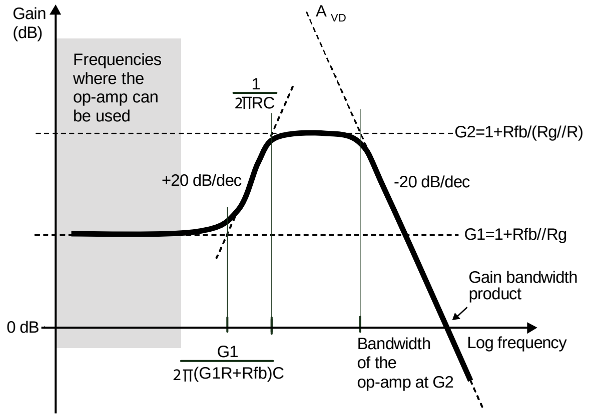


Figure 26: Closed-loop gain



Rg becomes a complex impedance. The closed-loop gain features a variation in frequency and can be expressed as *Equation 1*.

Equation 1

$$\text{Gain} = G1 \frac{1 + jC\omega \times \left(\frac{G1R + Rfb}{G1}\right)}{1 + jCR\omega}$$

Where a pole appears at 1/2πRC and a zero at G1/2π(G1R+Rfb)C. The frequency can be plotted as shown in *Figure 26*.

Table 7: External components versus low-frequency gain

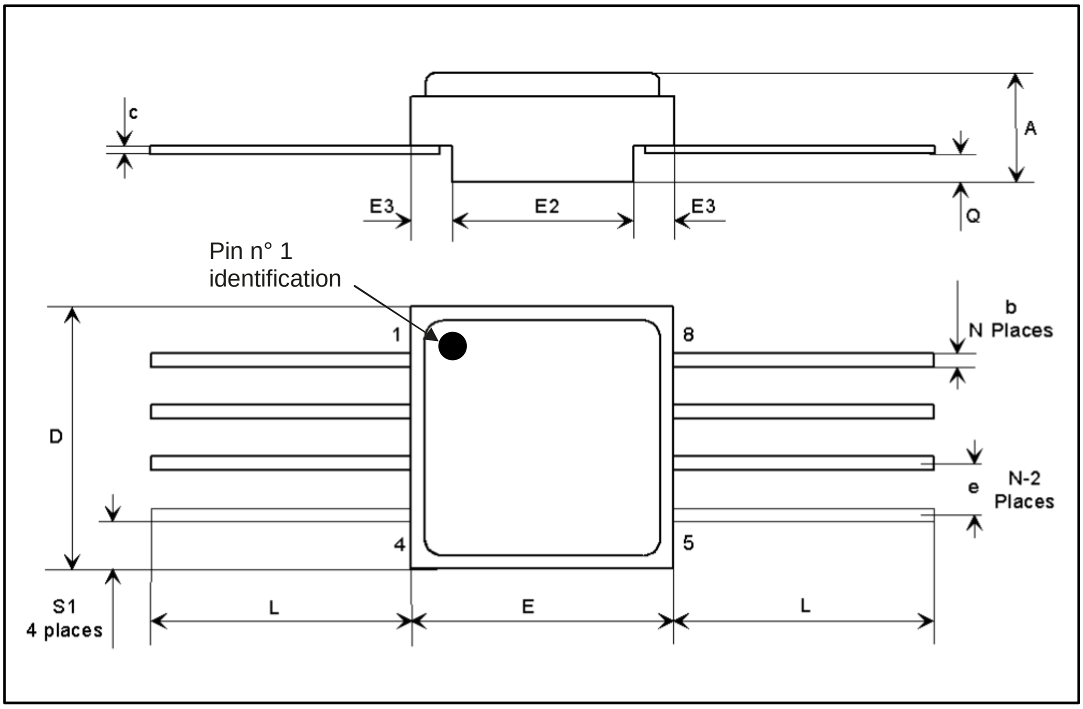
G1 (V/V)	R (Ω)	C (nF)	Rg (Ω)	Rfb (Ω)
1.1	510	1	20 k	2 k
2			2 k	
3			1 k	
4			750	2.4 k
5	Not connected	Not connected	820	3.3 k

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

5.1 Ceramic Flat-8 package information

Figure 27: Ceramic Flat-8 package outline



The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

Table 8: Ceramic Flat-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L	6.51		7.38	0.256		0.291
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

6 Ordering information

Table 9: Ordering information

Order code	SMD pin	EPPL [(1)]	Quality level	Package	Lead finish	Marking [(2)]	Packing
RHF43BK1	-	-	Engineering model	Flat-8	Gold	RHF43BK1	Strip pack
RHF43BK-01V	5962F0623701VXC	Yes	QML-V flight			5962F0623701VXC	

Notes:

(1)EPPL = ESA preferred part list

(2)Specific marking only. Complete marking includes the following:
- SMD pin (as indicated in above table)
- ST logo
- Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
- QML logo (Q or V)
- Country of origin (FR = France).

Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

7 Other information

7.1 Date code

The date code is structured as shown below:

- EM xyywwz
- QML-V yywwz
  where:
  - x (EM only) = 3 and the assembly location is Rennes, France
  - yy = last two digits of the year
  - ww = week digits
  - z = lot index in the week

7.2 Documentation

Table 10: Documentation provided for each type of product

Quality level	Documentation
Engineering model	—
QML-V flight	Certificate of conformance
	QCI (groups A, B, C, D, and E) [(1)]
	Screening electrical data
	Precap report
	PIND test [(2)]
	SEM inspection report [(3)]
	X-ray report

Notes:

(1) QCI = quality conformance inspection

(2) PIND = particle impact noise detection

(3) SEM = scanning electron microscope

8 Revision history

Table 11: Document revision history

Date	Revision	Changes
21-May-2007	1	First public release
10-Dec-2007	2	Changed name of pins on pinout diagram on cover page Modified supply current values over temperature range in electrical characteristics. Power dissipation removed from AMR table
29-Jan-2008	3	Added ELRS-free rad-hard design in description on cover page Modified description of heavy ion latch-up (SEL) immunity parameter in *Table 2*.
11-May-2009	4	Updated radiation immunity in *Features* and in *Table 2* Updated smb reference in *Features*
15-Oct-2009	5	Updated test conditions for Avd vs. Vicm in *Table 4* and *Table 5* Updated input current and voltage noise in *Table 4* Updated order codes in *Table 9*
30-Mar-2010	6	Added *Figure 4* and *Figure 5* Added information for ambient temperature in *Table 4* and *Table 5* Added *Section 4: "Achieving good stability at low gain"*
20-Aug-2010	7	Corrected "L" dimension in *Table 8*
27-Jul-2011	8	Added note underneath *Figure 27* and in the "Pin connections" diagram on the cover page.
08-Nov-2012	9	*Features*: added silhouette Added *Table 1: Device summary* *Table 2*: removed ±9 from “Supply voltage”; updated footnote1. Added *Figure 6* and *Figure 15* *Figure 17* through to *Figure 22*: modified titles *Table 9: Ordering information*: updated table and removed order code RHF43BK-01V.
06-Feb-2015	10	Replaced package name with “Flat-8S” instead of “Flat-8” Added marker to show the position of pin 1 on package silhouette, pinout and drawing. Updated *Features* Updated *Table 1: Device summary* Updated note concerning products in die form and QML-Q versions on the cover page. *Table 2: Absolute maximum ratings (AMR)*: transferred radiation information to *Table 6: Radiations*. *Table 8*: updated dimension "L" Added *Section 3: Radiations* Updated *Section 6: Ordering information* Added *Section 7: "Other information"*
24-Mar-2015	11	Replaced Flat-8S silhouette, pinout, and package with Flat-8 silhouette, pinout, and package.