

## P-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
- 100	0.134 at V <sub>GS</sub> = - 10 V	- 13.2 <sup>e</sup>	16.5 nC
	0.145 at V <sub>GS</sub> = - 4.5V	- 12.7 <sup>e</sup>	

### FEATURES

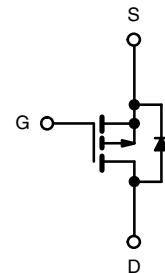
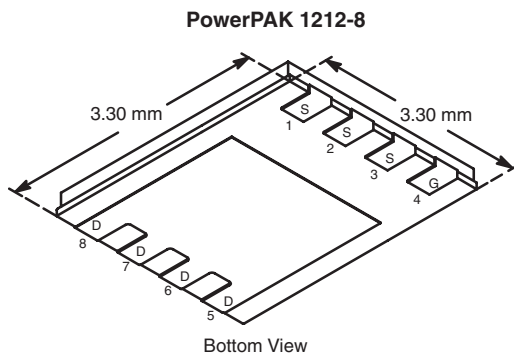
- Halogen-free Option Available
- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 1.07 mm Profile
- UIS and R<sub>G</sub> Tested



**RoHS**  
COMPLIANT

### APPLICATIONS

- Active Clamp in Intermediate DC/DC Power Supplies



P-Channel MOSFET

Ordering Information: Si7113DN-T1-E3 (Lead (Pb)-free)  
Si7113DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	- 100	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 13.2 <sup>e</sup>
		T <sub>C</sub> = 70 °C	- 10.6 <sup>e</sup>
		T <sub>A</sub> = 25 °C	- 3.5 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	- 2.8 <sup>a, b</sup>
Pulsed Drain Current	I <sub>DM</sub>	- 20	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	- 3.0 <sup>a, b</sup>
Avalanche Current	I <sub>AS</sub>	15	mJ
Single-Pulse Avalanche Energy	E <sub>AS</sub>	11.25	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	52
		T <sub>C</sub> = 70 °C	33
		T <sub>A</sub> = 25 °C	3.7 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	2.4 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>c, d</sup>		260	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Package limited.

**THERMAL RESISTANCE RATINGS**

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	26	33	°C/W
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	1.9	2.4	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.  
b. Maximum under Steady State conditions is 81 °C/W.

**SPECIFICATIONS**  $T_J = 25$  °C, unless otherwise noted

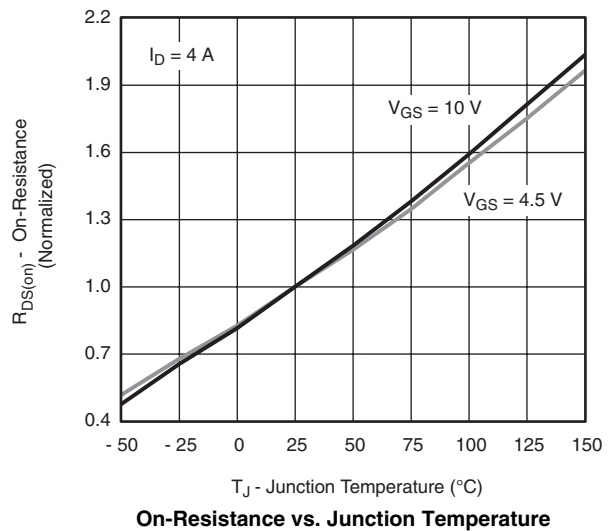
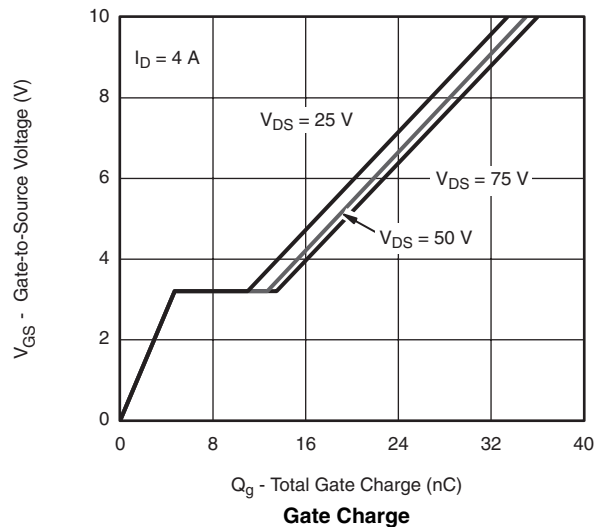
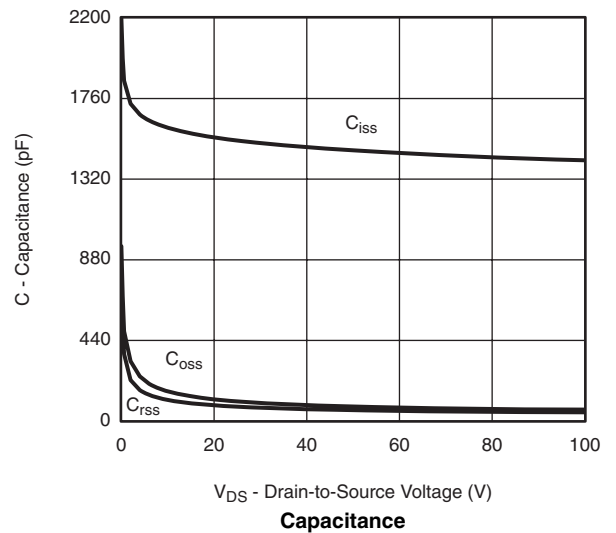
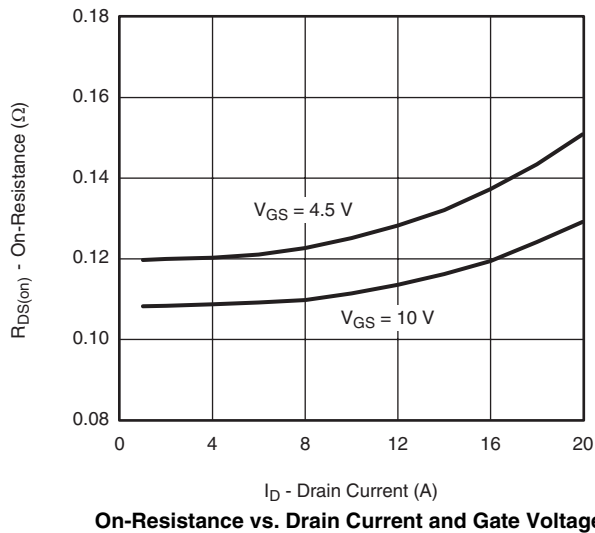
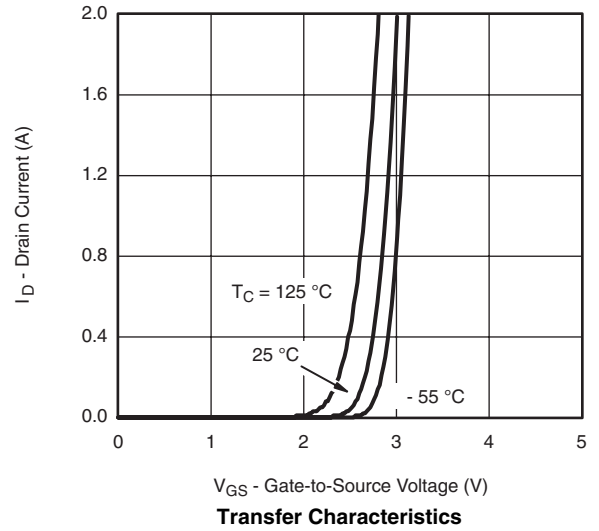
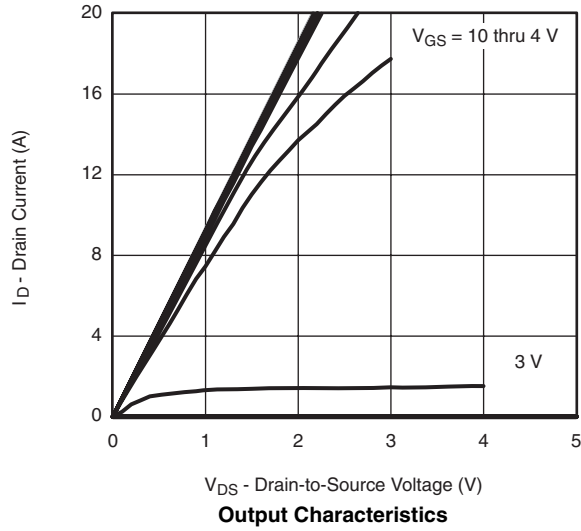
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = -250$ $\mu$ A	-100			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250$ $\mu$ A		-100		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-5.0		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250$ $\mu$ A	-1		-3	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100$ V, $V_{GS} = 0$ V			-1	$\mu$ A
		$V_{DS} = -100$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq -5$ V, $V_{GS} = -10$ V	-10			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -4$ A		0.108	0.134	$\Omega$
		$V_{GS} = -4.5$ V, $I_D = -3$ A		0.119	0.145	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15$ V, $I_D = 4$ A		25		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -50$ V, $V_{GS} = 0$ V, $f = 1$ MHz		1480		pF
Output Capacitance	$C_{oss}$			80		
Reverse Transfer Capacitance	$C_{rss}$			60		
Total Gate Charge	$Q_g$	$V_{DS} = -50$ V, $V_{GS} = -10$ V, $I_D = -4$ A		35	55	nC
			$V_{DS} = -50$ V, $V_{GS} = -4.5$ V, $I_D = -4$ A		16.5	
$Q_{gs}$		4.7				
$Q_{gd}$		8				
Gate Resistance	$R_g$	$f = 1$ MHz		5.3	8	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50$ V, $R_L = 12.5$ $\Omega$ $I_D \cong -4$ A, $V_{GEN} = -4.5$ V, $R_g = 1$ $\Omega$		30	45	ns
Rise Time	$t_r$			110	165	
Turn-Off Delay Time	$t_{d(off)}$			51	80	
Fall Time	$t_f$			40	60	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50$ V, $R_L = 12.5$ $\Omega$ $I_D \cong -4$ A, $V_{GEN} = -10$ V, $R_g = 1$ $\Omega$		11	18	
Rise Time	$t_r$			13	20	
Turn-Off Delay Time	$t_{d(off)}$			42	65	
Fall Time	$t_f$			10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C			-13.2	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				-20	
Body Diode Voltage	$V_{SD}$	$I_S = -3$ A		-0.8	-1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -4$ A, $di/dt = 100$ A/ $\mu$ s, $T_J = 25$ °C		46	70	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			97	150	nC
Reverse Recovery Fall Time	$t_a$			36		ns
Reverse Recovery Rise Time	$t_b$			10		

Notes:

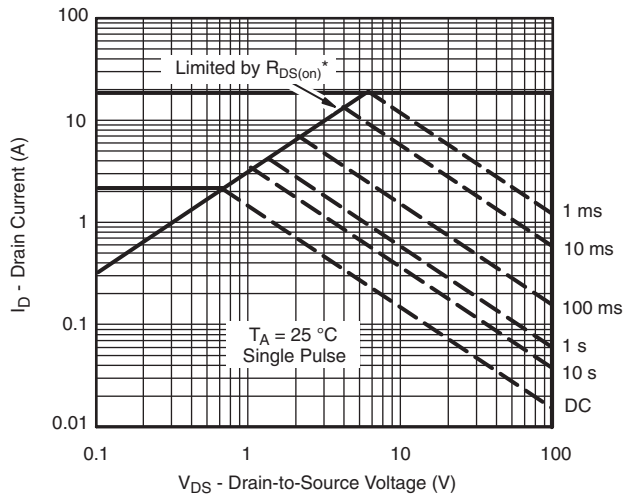
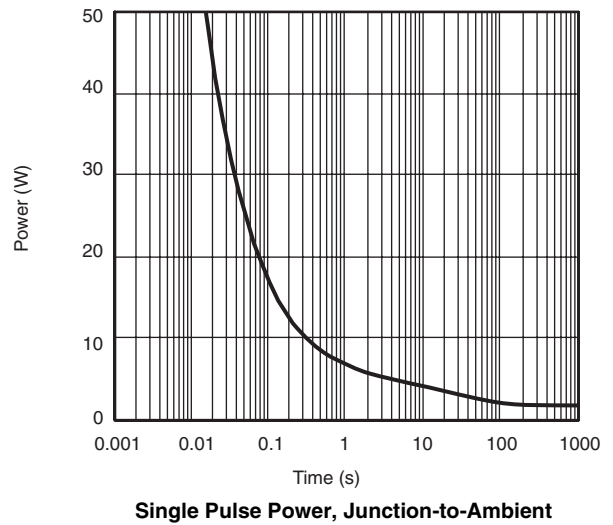
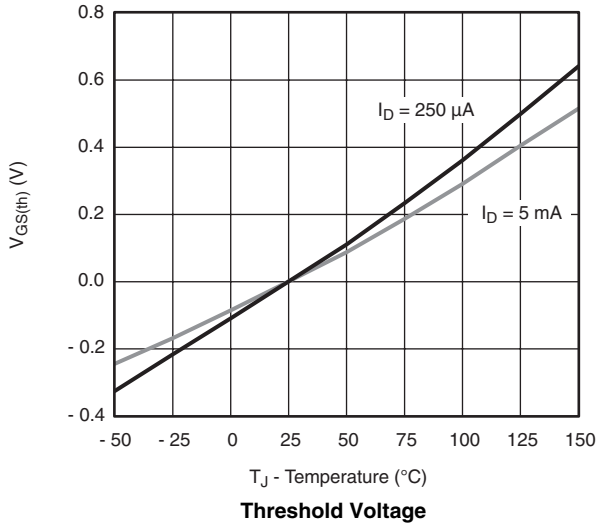
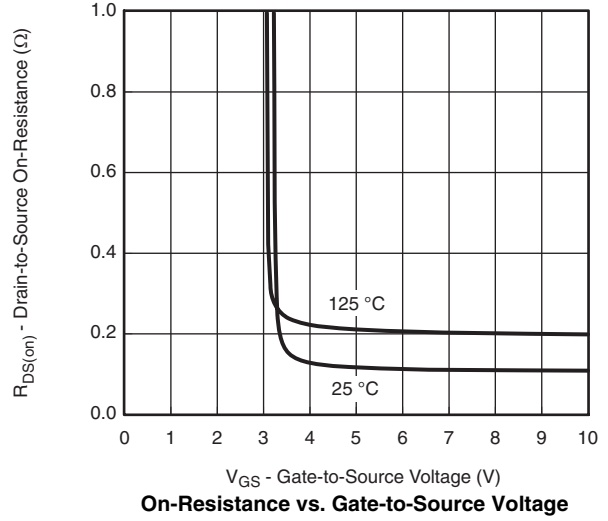
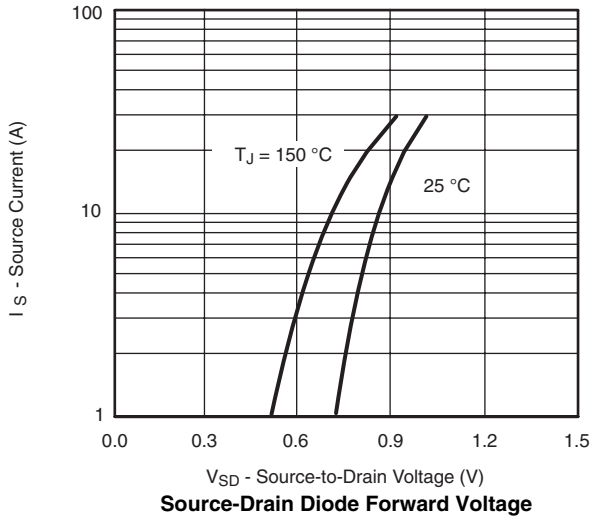
- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

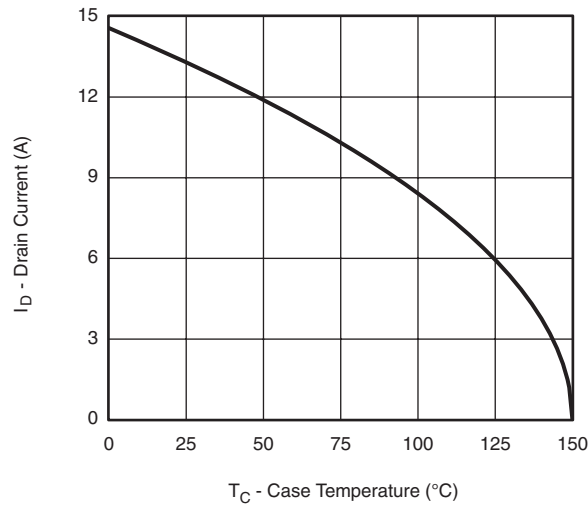


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

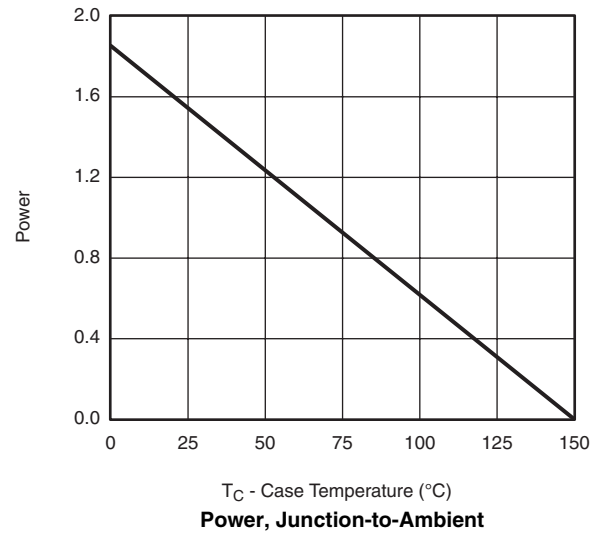
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Current Derating\***



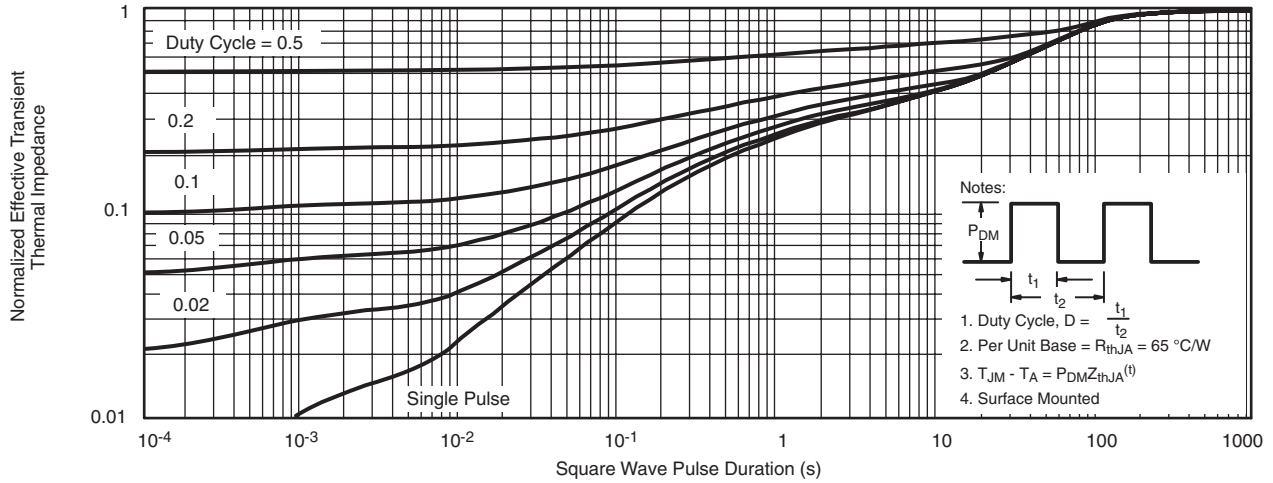
**Power, Junction-to-Case**



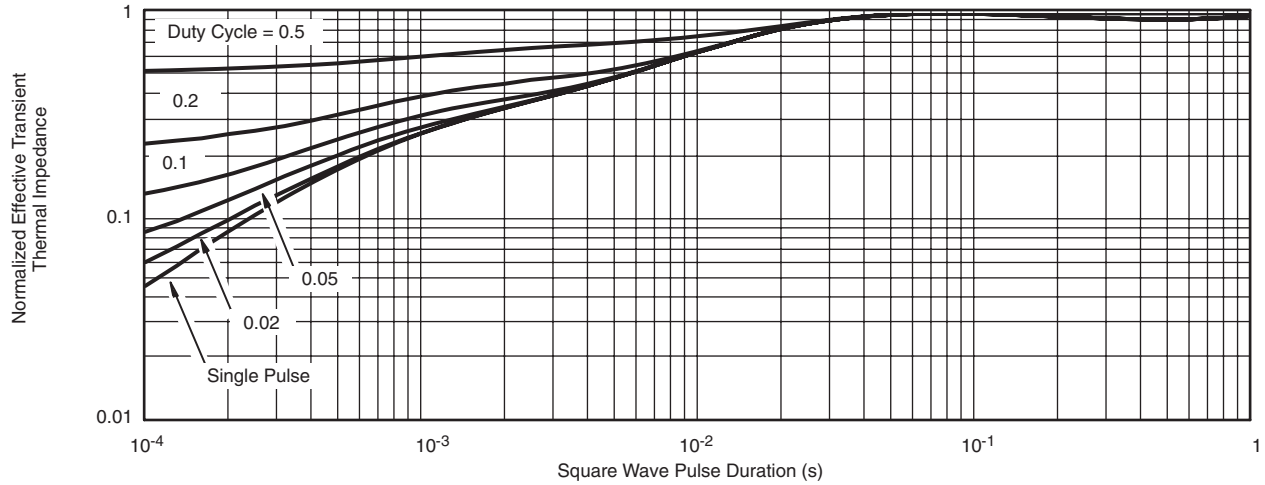
**Power, Junction-to-Ambient**

\* The power dissipation PD is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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