N-Channel 60-V (D-S) Fast Switching MOSFET

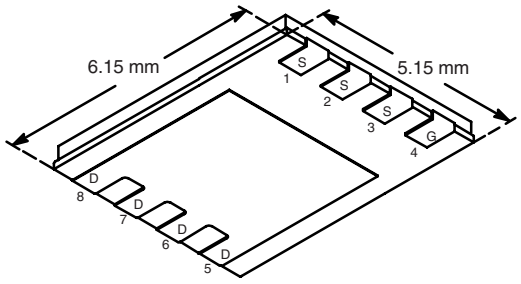
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
60	0.022 at V_{GS} = 10 V	10.3
	0.031 at V_{GS} = 4.5 V	8.7

FEATURES

- **Halogen-free According to IEC 61249-2-21 Available**
- TrenchFET® Power MOSFETs
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- PWM Optimized for Fast Switching
- 100 % R_g Tested

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

PowerPAK SO-8

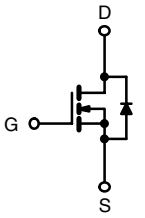


Bottom View

Ordering Information: Si7850DP-T1-E3 (Lead (Pb)-free)
Si7850DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- Primary Side Switch for 24 V DC/DC Applications
- Secondary Synchronous Rectifier



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	60		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	10.3	6.2	A
	T_A = 85 °C		7.5	4.5	
Continuous Source Current		I_S	3.7	1.5	
Pulsed Drain Current		I_{DM}	40		
Avalanche Current[b]		I_{AS}	15		
Single Avalanche Energy[b]		E_{AS}	11		mJ
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	4.5	1.8	W
	T_A = 85 °C		2.3	0.9	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	22	28	°C/W
	Steady State		58	70	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.6	3.3	

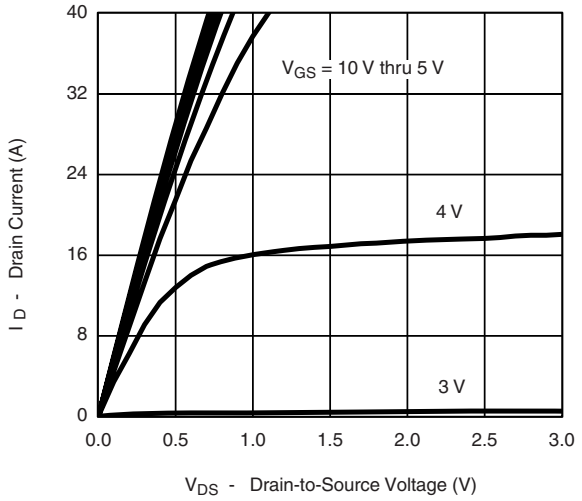
Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. Guaranteed by design, not subject to production testing.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1		3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 55 °C			20	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10.3 A		0.018	0.022	Ω
		V_{GS} = 4.5 V, I_D = 8.7 A		0.025	0.031	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 10.3 A		26		S
Diode Forward Voltage[a]	V_{SD}	I_S = 3.8 A, V_{GS} = 0 V		0.85	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 10.3 A		18	27	nC
Gate-Source Charge	Q_{gs}			3.4		
Gate-Drain Charge	Q_{gd}			5.3		
Gate Resistance	R_g		0.5	1.4	2.2	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			12	24	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 3.8 A, dI/dt = 100 A/µs		50	80	

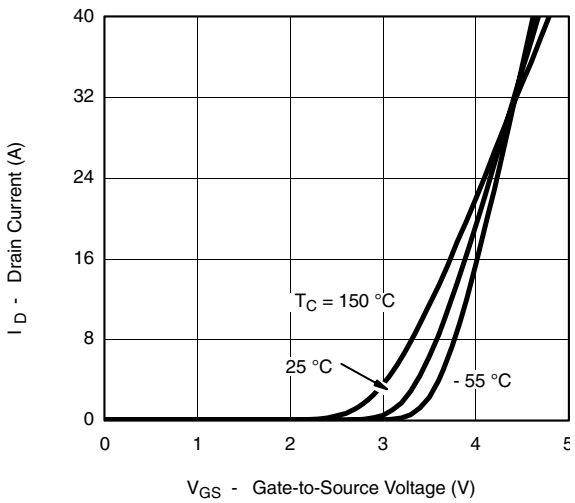
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

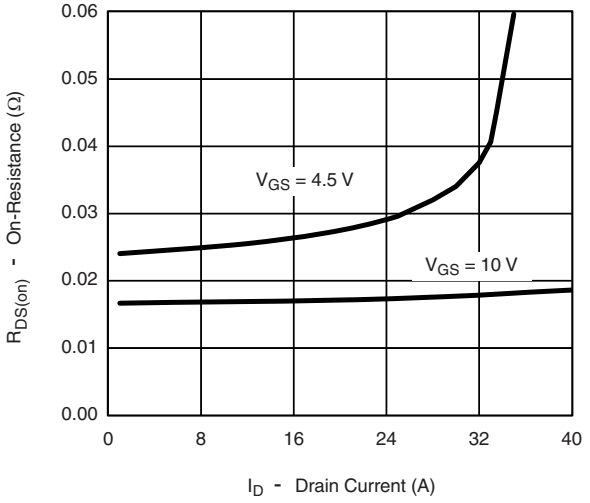


Output Characteristics

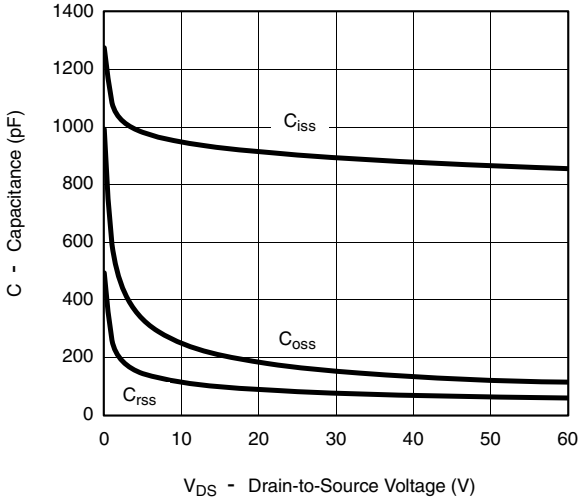


Transfer Characteristics

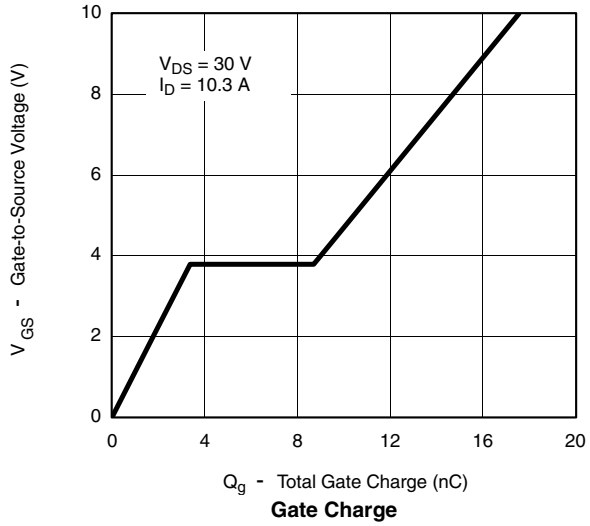
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



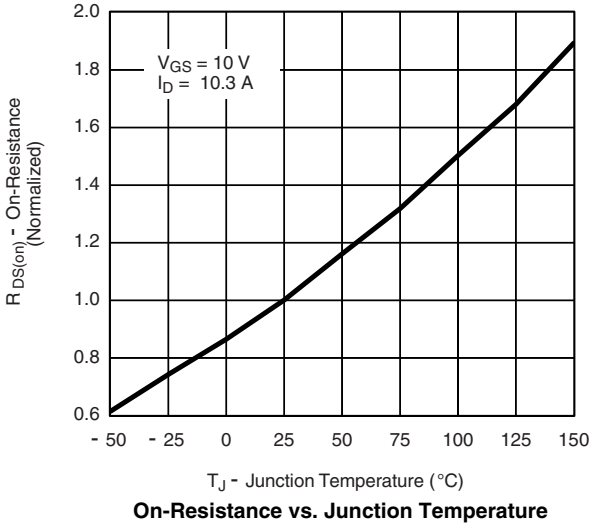
On-Resistance vs. Drain Current



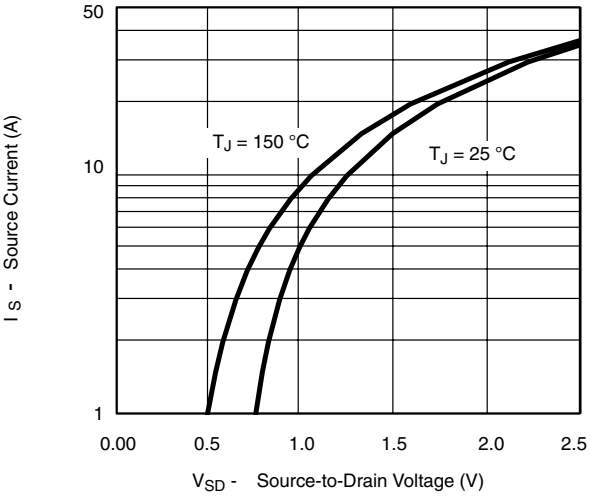
Capacitance



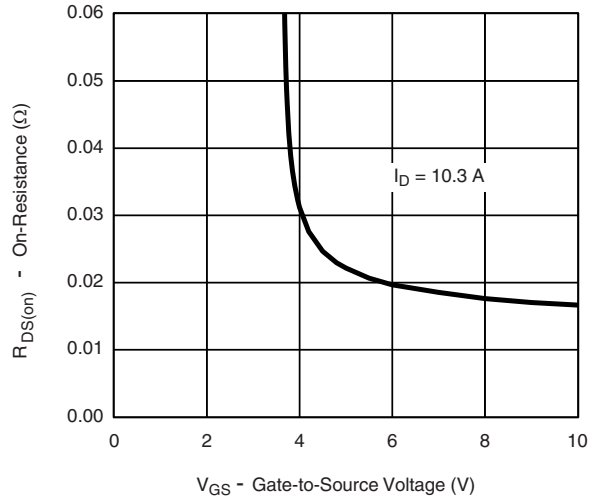
Gate Charge



On-Resistance vs. Junction Temperature

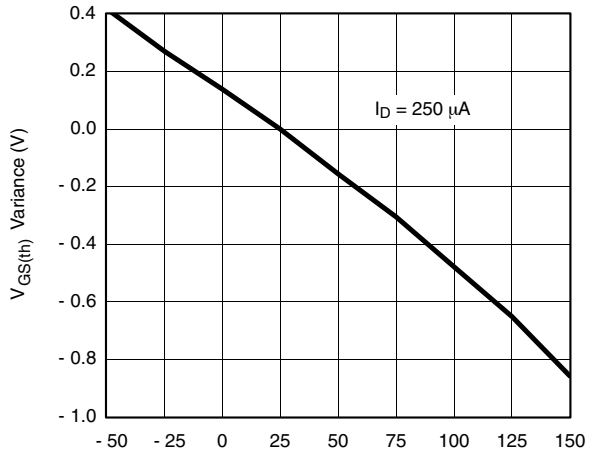


Source-Drain Diode Forward Voltage

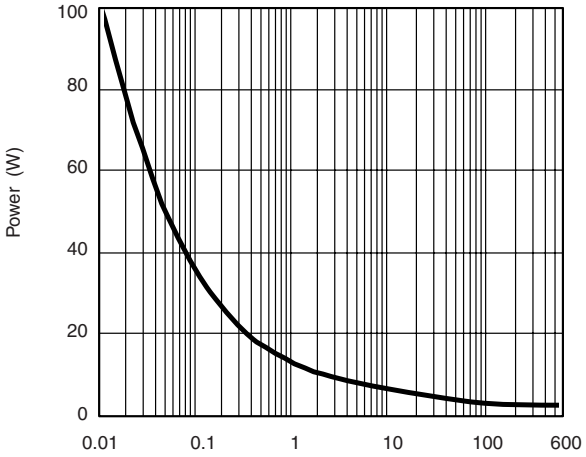


On-Resistance vs. Gate-to-Source Voltage

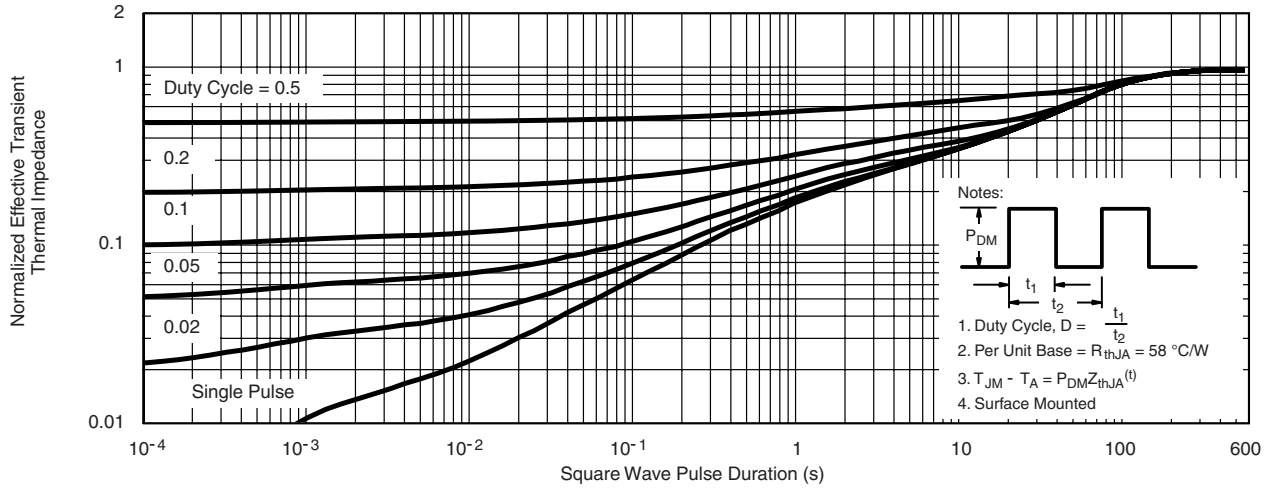
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



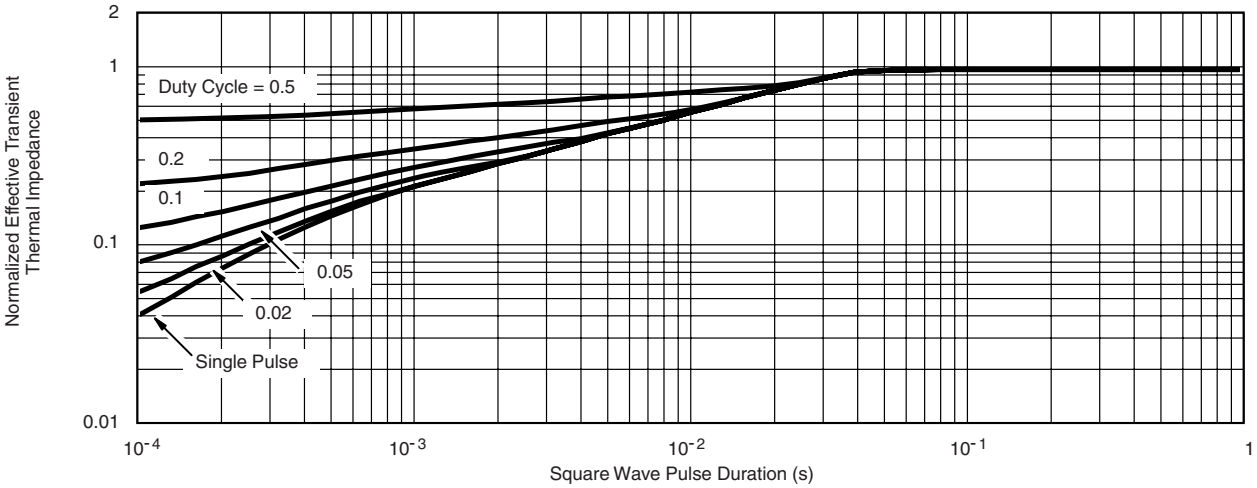
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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