262144 x 16 BIT VRAM
MULTIPORT VIDEO RAM

AVAILABLE AS MILITARY SPECIFICATIONS
- Military Processing Flow(SM Level)
- -55C to 125C temperature

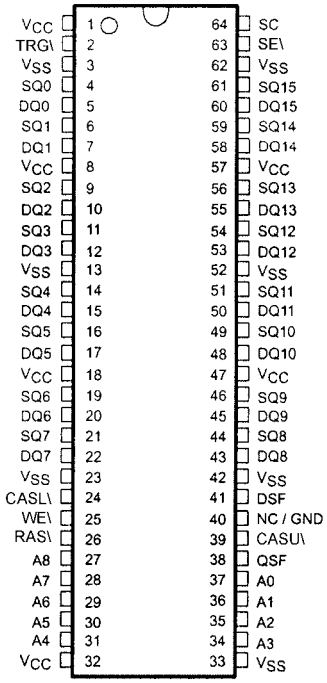
FEATURES
- Organization:
  - DRAM: 262 144 by 16 Bits
  - SAM: 512 by 16 Bits
- Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports
- Bidirectional Data-Transfer Function From the DRAM to the Serial-Data Register, and from Serial Data Register to DRAM
- (8 x 8) x 2 Block Write feature for fast area fill
- Write-Per-Bit Feature for Selective Write to Each RAM I/O; Two Write-Per-Bit Modes to Simplify System Design
- Byte-Write Control (CASL, CASU) Provides Flexibility
- Extended Data Output for Faster System Cycle Time
- Enhanced Page-Mode Operation for Faster Access
- CAS-Before-RAS (CBR) and Hidden-Refresh Modes
- Long Refresh Period: Every 8 ms (Maximum)
- Up to 50-MHz Uninterrupted Serial-Data Streams
- 512 Selectable Serial-Register Starting Locations
- SE-Controlled Register-Status QSF
- Split-Register-Transfer Read for Simplified Real-Time Register Load
- Programmable Split-Register Stop Point
- 3-State Serial Outputs Allow Easy Multiplexing of Video-Data Streams
- Pin-out Compatible upgrade from SM55161
- Compatible With JEDEC Standards

OPTIONS / MARKING

- Timing
  - 70ns access -70
  - 75ns access -75
  - 80ns access -80
- Package
  - 68 pin PGA GB
  - 64 pin Flatpack HKC
- Operating Temperature Ranges
  - Military (-55°C to +125°C) M suffix
  - Industrial (-40°C to +85°C) I suffix

PIN ASSIGNMENT
(Top View)

64-Pin Ceramic Flatpack (HKC)



PIN DESCRIPTIONS

PIN	DESCRIPTION
A0-A8	Address inputs
CASL\, CASU\	Column-Address Strobe/Byte Selects
DQ0-DQ15	DRAM Data I/O, Write Mask Data Special Function Select
DSF	Special-Function Select
NC/GND	No Connect/Ground (NOTE: Not connected internally to V_{SS})
QSF	Special-Function Output
RAS\	Row-Address Strobe
SC	Serial Clock
SE\	Serial Enable
SQ0-SQ15	Serial-Data Output
TRG\	Output Enable, Transfer Select
V_{CC}	5V Supply (TYP)
V_{SS}	Ground
WE\	DRAM Write-Enable Select

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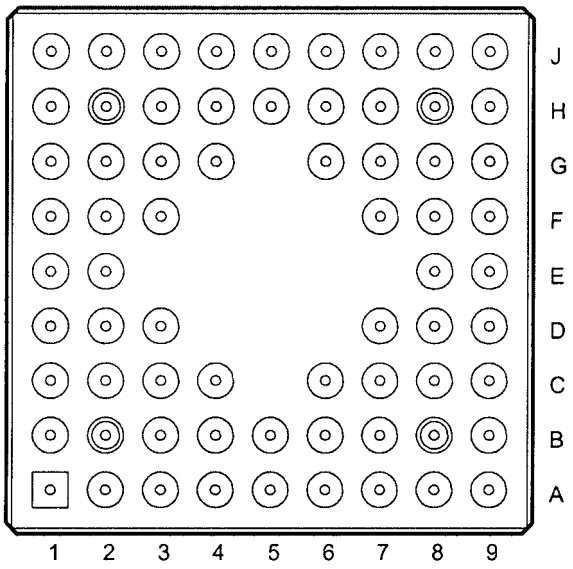
PERFORMANCE RANGES

		-70		-75		-80		
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Access Time Row Enable	$t_{a(R)}$		70		75		80	ns
Access Time Serial Data	$t_{a(SQ)}$		20		23		25	ns
DRAM Cycle Time	$t_{c(W)}$	130		140		150		ns
DRAM Page Mode	$t_{c(P)}$	45		48		50		ns
Serial Cycle Time	$t_{c(SC)}$	22		24		30		ns
Operating Current, Serial Port Stand-by	I_{CC1}		165		165		210	mA
Operating Current, Serial Port Active	I_{CC1A}		210		210		195	mA

GB PACKAGE (Bottom View) & PIN ASSIGNMENTS



PIN No.	NAME	PIN No.	NAME
J1	DQ1	E8	V_{SS1}
J2	SQ3	E9	A4
J3	DQ3	D1	SE\
J4	DQ4	D2	V_{SS1}
J5	DQ5	D3	V_{DD1}
J6	DQ6	D7	V_{SS1}
J7	SQ7	D8	A3
J8	CASL\	D9	A2
J9	A8	C1	SQ15
H1	DQ0	C2	V_{SS1}
H2	SQ2	C3	V_{DD2}
H3	DQ2	C4	V_{SS2}
H4	SQ4	C6	V_{DD2}
H5	SQ5	C7	V_{SS2}
H6	SQ6	C8	CASU\
H7	DQ7	C9	A1
H8	WE\	B1	DQ15
H9	A7	B2	DQ14
G1	SQ0	B3	DQ13
G2	SQ1	B4	DQ12
G3	V_{DD2}	B5	DQ11
G4	V_{SS2}	B6	DQ10
G6	V_{DD2}	B7	SQ8
G7	V_{SS2}	B8	DSF
G8	RAS\	B9	A0
G9	A6	A1	SQ14
F1	TRG	A2	SQ13
F2	V_{SS1}	A3	SQ12
F3	V_{DD1}	A4	SQ11
F7	V_{DD1}	A5	SQ10
F8	V_{DD1}	A6	SQ9
F9	A5	A7	DQ9
E1	SC	A8	DQ8
E2	V_{DD1}	A9	QSF

GENERAL DESCRIPTION

The SMJ55161A, a multiport-video random-access memory (RAM), is a high-speed, dual-port memory device. It consists of a dynamic RAM (DRAM) module organized as 262 144 words of 16 bits each interfaced to a serial-data register (serial-access memory [SAM]) organized as 512 words of 16 bits each. The SMJ55161A supports three basic types of operation: random access to and from the DRAM, serial access to/from the serial register, and transfer of data from any row in the DRAM to the serial register and vice versa. Except during transfer operations, the SMJ55161A can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The SMJ55161A is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel-draw rates are achieved by the device's $(8 \times 8) \times 2$ block-write feature. The block-write mode allows 16 bits of data (present in an on-chip color-data register) to be written to any combination of eight adjacent column-address locations. As many as 128 bits of data can be written to memory during each CAS\ cycle time. Also, on the DRAM port and SAM port, a write mask or a write-per-bit feature allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register that, once loaded, can be used on subsequent write cycles without reloading. The SMJ55161A also offers byte control which can be applied in read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. The SMJ55161A also offers extended-data-output (EDO) mode. The EDO mode is effective in both the page-mode and standard DRAM cycles.

The SMJ55161A offers a split-register-transfer read (DRAM-to-SAM) feature for the serial register (SAM port) that enables real-time-register-load implementation for continuous serial-data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads done during CRT-retrace periods), the full-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 50 MHz. During the split-register-transfer read operations, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active.

All inputs, outputs, and clock signals on the SMJ55161 are compatible with Series 54/74 TTL. All address lines and data-in lines are latched on-chip to simplify system design. All data-out lines are unlatched to allow greater system flexibility.

The SMJ55161A is offered in a 68-pin ceramic pin-grid-array package (GB suffix) and a 64-pin ceramic flatpack (HKC suffix).

The SMJ55161A is supported by a broad line of graphic processors and control devices from Texas Instruments. See Table 2 and Table 4 for additional information.

Additional features of the 55161A include MASKED FLASH WRITE which allows for data in color register to be written into all the memory locations of a selected row.

FUNCTIONAL BLOCK DIAGRAM

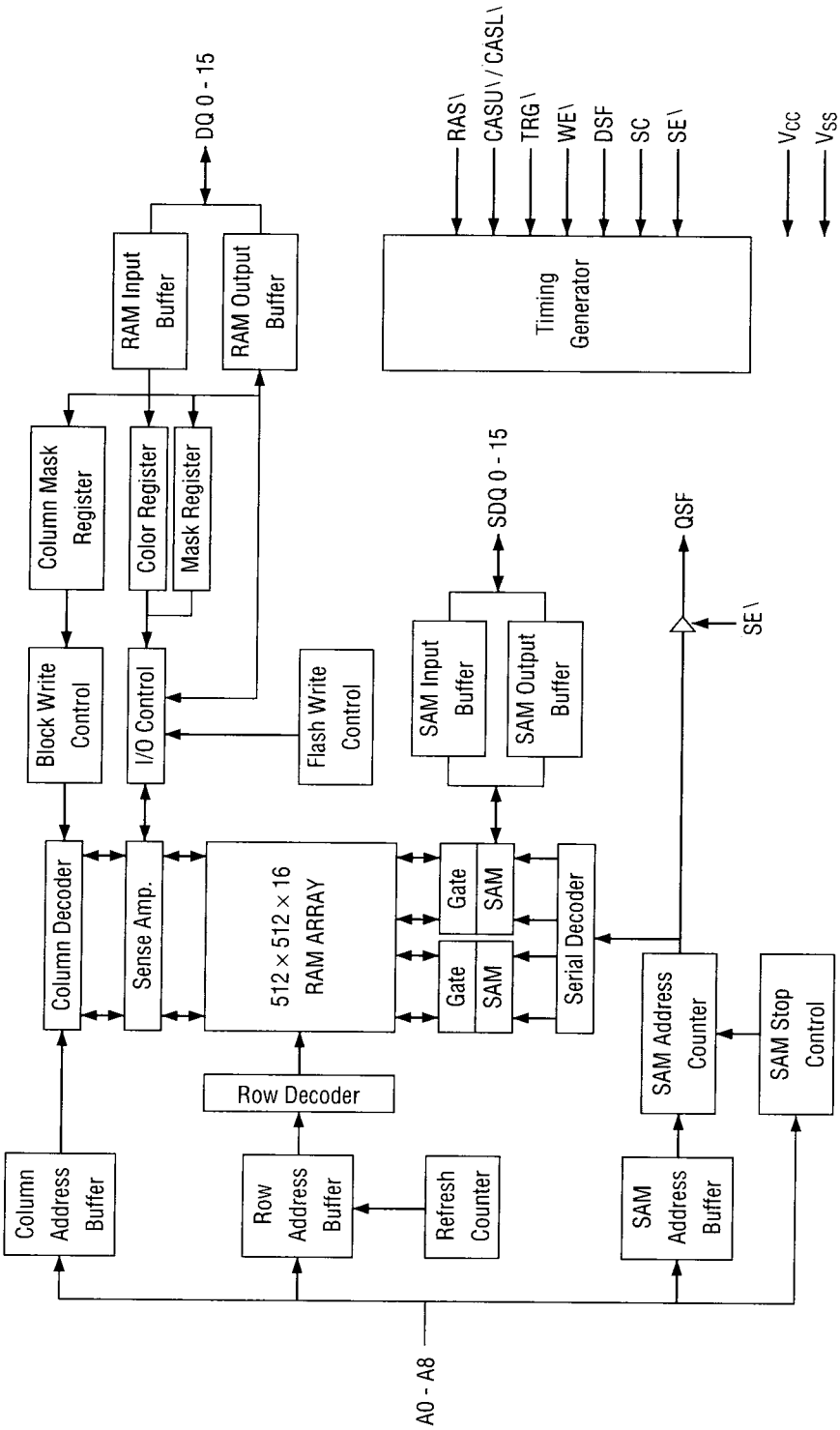


TABLE 1: DRAM & SAM FUNCTIONS

FUNCTION	RAS\ FALL				CASx\ FALL	ADDRESS		DQ0-DQ15[1]		MNE CODE
	CASx\[2]	TRG\	WE\	DSF	DSF	RAS\	CASX\[3]	RAS\	CASL\ CASU\ WE\	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	---
CBR refresh (no reset) and stop-point set[4]	L	X	L	H	X	Stop point[5]	X	X	X	CBRS
CBR refresh (option reset)[6]	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)[7]	L	X	H	H	X	X	X	X	X	CBRN
Full-register-transfer read	H	L	H	L	X	Row Address	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Address	Tap Point	X	X	SRT
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Address	Column Address	Write Mask	Valid Data	RWM
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Address	Block Address A3-A8	Write Mask	Column Mask	BWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Address	Column Address	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Address	Block Address A3-A8	X	Column Mask	BWM
DRAM write (nonmasked)	H	H	H	L	L	Row Address	Column Address	X	Valid Data	RW
DRAM block write (nonmasked)	H	H	H	L	H	Row Address	Block Address A3-A8	X	Column Mask	BW
Load write-mask register[8]	H	H	H	H	L	Refresh Address	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Address	X	X	Color Data	LCR
Masked Write Transfer[9]	H	L	L	L	X	Row Address	Tap Point	Write Mask	X	MWT
Masked Split Write Transfer[9]	H	L	L	H	X	Row Address	Tap Point	Write Mask	X	MSWT
Masked Flash Write Transfer[9]	H	H	L	H	X	Row Address	X	Write Mask	---	FWM

LEGEND:

Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled
X = Don't Care

NOTES:

1. DQ0–DQ15 are latched on either the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later.
2. Logic L is selected when either or both CASL\ and CASU\ are low.
3. The column address and block address are latched on the first falling edge of CASx\.
4. CBRS cycle should be performed immediately after the power-up initialization cycle.
5. A0–A3, A8: don't care; A4–A7: stop-point code
6. CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
7. CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
8. Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.
9. MWT, MSWT, FWM function shown are for nonpersistent mask writes. These functions also support persistent mask write.

TABLE 2: PIN DESCRIPTIONS VS. OPERATIONAL MODE

PIN	DRAM	TRANSFER	SAM
A0-A8	Row, column address	Row address, Tap point	
CASL\, CASU\	Column-address strobe, DQ output enable	Tap-address strobe	
DQ	DRAM data I/O, write mask		
DSF	Block-write enable Write-mask-register load enable Color-register load enable CBR (option reset)	Split-register-transfer enable	
RAS\	Row-address strobe	Row-address strobe	
SE\			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial-data output
TRG\	DQ output enable	Transfer enable	
WE\	Write enable, write-pre-bit enable		
QSF	Special-function output		Serial-register status
NC/GND	Either make no external connection or tie to system GND (V_{SS})		
V_{CC} [1]	5V supply		
V_{SS} [1]	Ground		

NOTES: 1. For proper device operation, all VCC pins must be connected to a 5-V supply, and all VSS pins must be tied to ground.

address (A0–A8)

Eighteen address bits are required to decode each one of the 262 144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of RAS\. Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the first falling edge of CASx\. All addresses must be stable on or before the falling edge of RAS\ and the first falling edge of CASx\.

During the full-register-transfer read operation, the states of A0–A8 are latched on the falling edge of RAS\ to select one of the 512 rows where the transfer occurs. At the first falling edge of CASx\, the column-address bits A0–A8 are latched. The most significant column-address bit (A8) selects which half of the row is transferred to the SAM. The appropriate 8-bit column address (A0–A8) selects one of 512 tap points (starting positions) for the serial-data output.

During the split-register-transfer read operation, an internal counter selects which half of the register is used. If the high half of the SAM is currently in use, the low half of the SAM is loaded with the low half of the DRAM half row and vice versa. Column address (A8) selects the DRAM half row. The remaining eight address bits (A0–A7) are used to select one of 256 possible starting locations within the SAM.

row-address strobe (RAS\)

RAS\ is similar to a chip enable so that all DRAM cycles and transfer cycles are initiated by the falling edge of RAS\. RAS\ is a control input that latches the states of the row address, WE\, TRG\, CASL\, CASU\, and DSF onto the chip to invoke DRAM and transfer-read/write functions of the SMJ55161A.

column-address strobe (CASL, CASU)

CASL\ and CASU\ are control inputs that latch the states of the column address and DSF to control DRAM and transfer functions of the SMJ55161A. CASx\ also acts as output enable for the DRAM output pins DQ0–DQ15. In DRAM operation, CASL\ enables data to be written to or read from the lower byte (DQ0–DQ7), and CASU\ enables data to be written to or from the upper byte (DQ8–DQ15). In transfer operations, address bits A0–A8 are latched at the first falling edge of CASx\ as the start position (tap) for the serial-data output (SQ0–SQ15).

output enable/transfer select (TRG\)

TRG\ selects either DRAM or transfer operation as RAS\ falls. For DRAM operation, TRG\ must be held high as RAS\ falls. During DRAM operation, TRG functions as an output enable for the DRAM output pins DQ0–DQ15. For transfer operation, TRG\ must be brought low before RAS\ falls.

write-mask select, write enable (WE)

In DRAM operation, WE\ enables data to be written to the DRAM. WE\ is also used to select the DRAM write-per-bit mode. Holding WE\ low on the falling edge of RAS\ invokes the write-per-bit operation. The SMJ55161A supports both the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

special-function select (DSF)

The DSF input is latched on the falling edge of RAS\ or the first falling edge of CASx\, similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- CBR refresh with reset (CBR)
- CBR refresh with no reset (CBRN)
- CBR refresh with no reset and stop-point set (CBRS)
- Block write
- Loading write-mask register for the persistent write-per-bit mode (LMR)
- Loading color register for the block-write mode
- Split-register-transfer read

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ-output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 54 TTL load. Data out is the same polarity as data in. During a normal access cycle, the outputs remain in the high-impedance state until TRG\ is brought low. Data appears at the outputs until TRG\ returns high, CASx\ returns high following RAS\ returning high, or RAS\ returns high following CASx\ returning high. The write mask is latched into the device through the random DQ pins by the falling edge of RAS\ and is used on all write-per-bit cycles. In a transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

serial-data outputs (SQ0 –SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 54 TTL load. The serial outputs are in the high-impedance (floating) state as long as the serial-enable pin, SE\, is high. The serial outputs are enabled when SE\ is brought low.

serial clock (SC)

Serial data is accessed out of the data register during the rising edge of SC. The SMJ55161A is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC-clock operating frequency.

serial enable (SE)

During serial-access operations, SE\ is used as an enable/disable for the SQ outputs. SE\ low enables the serial-data output while SE\ high disables the serial-data output. SE\ is also used as an enable/disable for output pin QSF.

IMPORTANT: While SE\ is held high, the serial clock is not disabled. External SC pulses increment the internal serial-address counter regardless of the state of SE\. This ungated serial-clock scheme minimizes access time of serial output from SE\ low because the serial-clock input buffer and the serial-address counter are not disabled by SE\.

special-function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial-address pointer is accessing the lower (least significant) 256 bits of the serial register (SAM). When QSF is high, the pointer is accessing the higher (most significant) 256 bits of the SAM.

During full-register-transfer operations, QSF can change state upon completing the cycle. This state is determined by the tap point loaded during the transfer cycle. QSF is enabled by SE\; therefore, if SE\ is high, the QSF output is in the high-impedance state.

no connect / ground (NC/GND)

NC/GND must be tied to system ground or left floating for proper device operation.

TABLE 3: DRAM FUNCTIONS

FUNCTION	RAS\ FALL				CASx\ FALL	ADDRESS		DQ0-DQ15[1]		MNE CODE
	CASx\[2]	TRG\	WE\	DSF	DSF	RAS\	CASX\[3]	RAS\	CASL\ CASU\ WE\	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	---
CBR refresh (no reset) and stop-point set[4]	L	X	L	H	X	Stop point[5]	X	X	X	CBRS
CBR refresh (option reset)[6]	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)[7]	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Address	Column Address	Write Mask	Valid Data	RWM
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Address	Block Address A3-A8	Write Mask	Column Mask	BWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Address	Column Address	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Address	Block Address A3-A8	X	Column Mask	BWM
DRAM write (nonmasked)	H	H	H	L	L	Row Address	Column Address	X	Valid Data	RW
DRAM block write (nonmasked)	H	H	H	L	H	Row Address	Block Address A3-A8	X	Column Mask	BW
Load write-mask register[8]	H	H	H	H	L	Refresh Address	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Address	X	X	Color Data	LCR

LEGEND:

Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled
X = Don't Care

NOTES:

1. DQ0–DQ15 are latched on either the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later.
2. Logic L is selected when either or both CASL\ and CASU\ are low.
3. The column address and block address are latched on the first falling edge of CASx\.
4. CBRS cycle should be performed immediately after the powerup initialization cycle.
5. A0–A3, A8: don't care; A4–A7: stop-point code
6. CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.
7. CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.
8. Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.
9. MWT, MSWT, FWM function shown are for nonpersistent mask writes. These functions also support persistent mask write.

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row-address setup, row-address hold, and address multiplex. The maximum RAS\ low time and CAS\ page cycle time used determine the number of columns that can be accessed.

Unlike conventional page-mode operations, the enhanced page mode allows the SMJ55161A to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when CASx\ transitions low. A valid column address can be presented immediately after the row-address hold time has been satisfied, usually well in advance of the falling edge of CASx\. In this case, data is obtained after $t_{a(C)}$ MAX (access time from CASx\ low) if $t_{a(CA)}$ MAX (access time from column address) has been satisfied.

REFRESH

CAS-before-RAS (CBR) refresh

CBR refreshes are accomplished by bringing either or both CASL\ and CASU\ low earlier than RAS\. The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN and CBRS refreshes (no reset) do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period, $t_{rf(MA)}$. The output buffers remain in the high-impedance state during the CBR refresh cycles regardless of the state of TRG\.

hidden refresh

A hidden refresh is accomplished by holding both CASL\ and CASU\ low in the DRAM read cycle and cycling RAS\. The output data of the DRAM read cycle remains valid while the refresh is carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

RAS-only refresh

A RAS\-only refresh is accomplished by cycling RAS\ at every row address. Unless CASx\ and TRG\ are low, the output buffers remain in the high-impedance state to conserve power. Externally-generated addresses must be supplied during RAS\-only refresh. Strobing each of the 512 row addresses with RAS\ causes all bits in each row to be refreshed.

extended data output

The SMJ55161A features EDO during DRAM accesses. While RAS\ and TRG\ are low, the DRAM output remains valid. The output remains valid even when CASx\ returns high until WE\ is low, TRG\ is high, or both CASx\ and RAS\ are high (see Figure 1 and Figure 2). The EDO mode functions during all read cycles including DRAM read, page-mode read, and read-modify-write cycles (see Figure 3).

FIGURE 1: DRAM Read Cycle With RAS\-Controlled Output

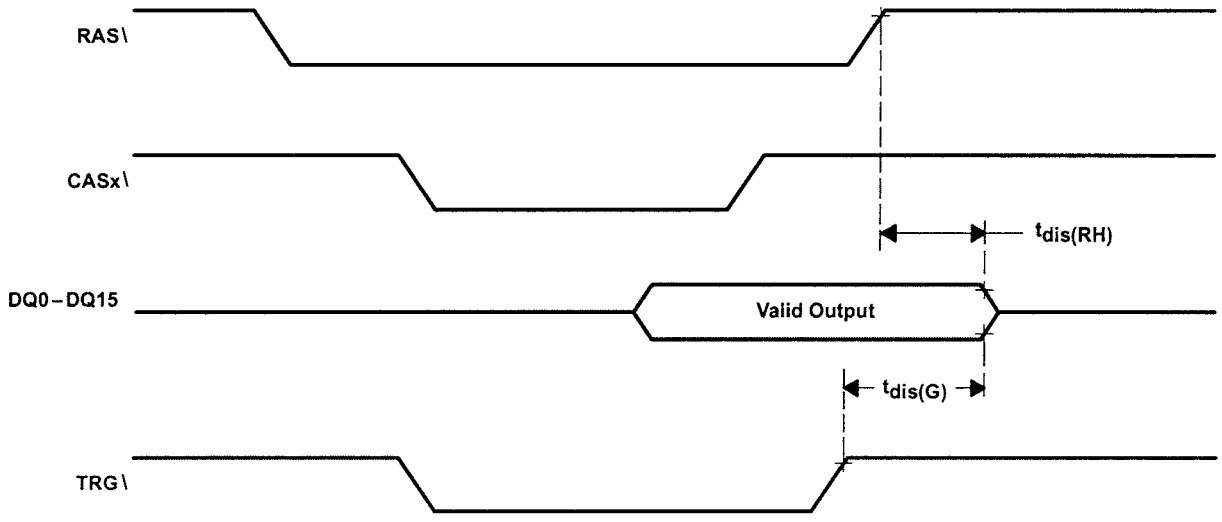


FIGURE 2: DRAM Read Cycle With CASx\-Controlled Output

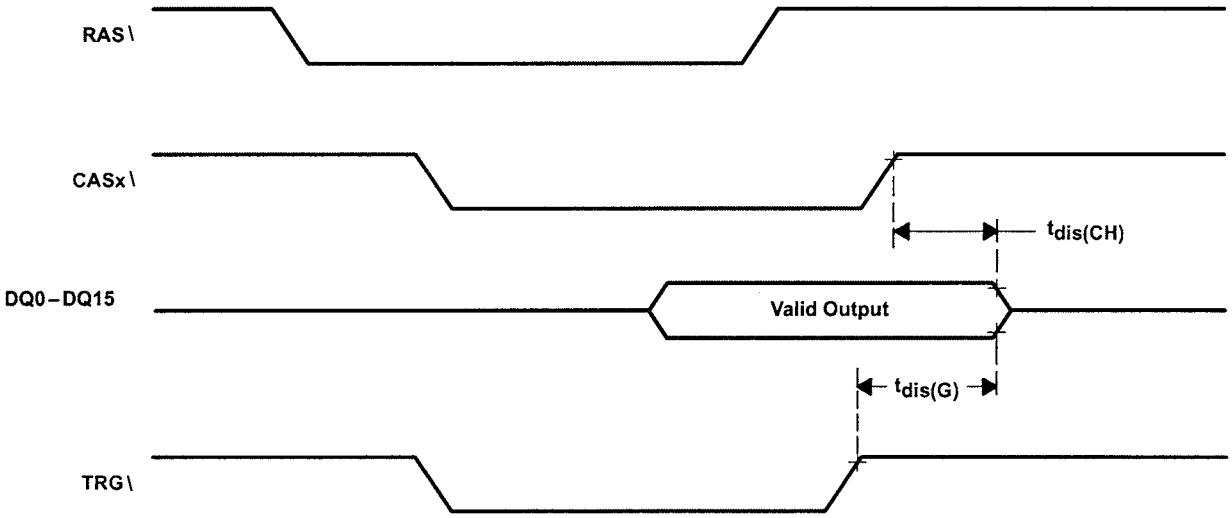
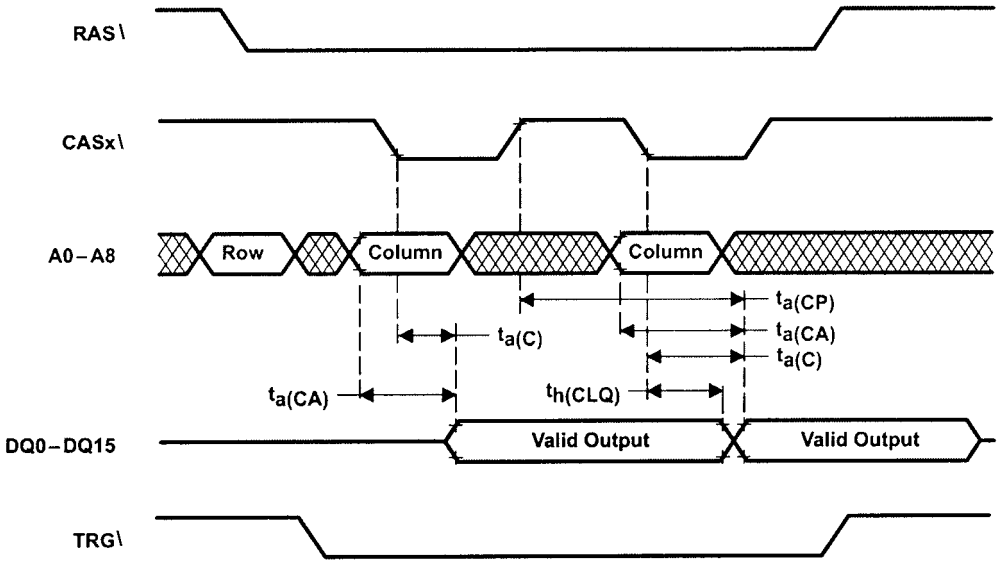


FIGURE 3: DRAM Page-Read Cycle with Extended Output



byte operation

Byte operation can be applied in DRAM-read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. In byte operation, the column address (A0–A8) is latched at the first falling edge of CASx\. In read cycles, CASL\ enables the lower byte (DQ0–DQ7) and CASU\ enables the upper byte (DQ8–DQ15) (see Figure 4).

In byte-write operation, CASL enables data to be written to the lower byte (DQ0–DQ7), and CASU\ enables data to be written to the upper byte (DQ8–DQ15). In an early write cycle, WE is brought low prior to both CASx\ signals, and data setup and hold times for DQ0 –DQ15 are referenced to the first falling edge of CASx\ (see Figure 5).

For late-write or read-modify-write cycles, WE\ is brought low after either or both CASL\ and CASU\ fall. The data is strobed in with data setup and hold times for DQ0 –DQ15 referenced to WE\ (see Figure 6).

FIGURE 4: Example of a Byte-Read Cycle

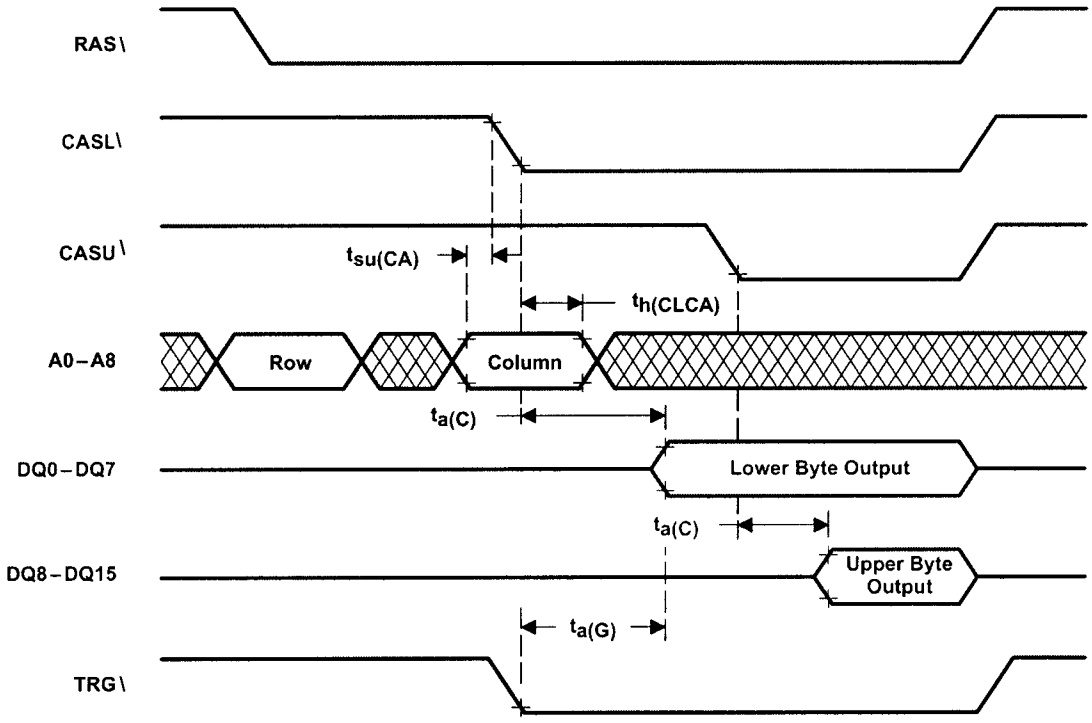


FIGURE 5: Example of an Early-Write Cycle

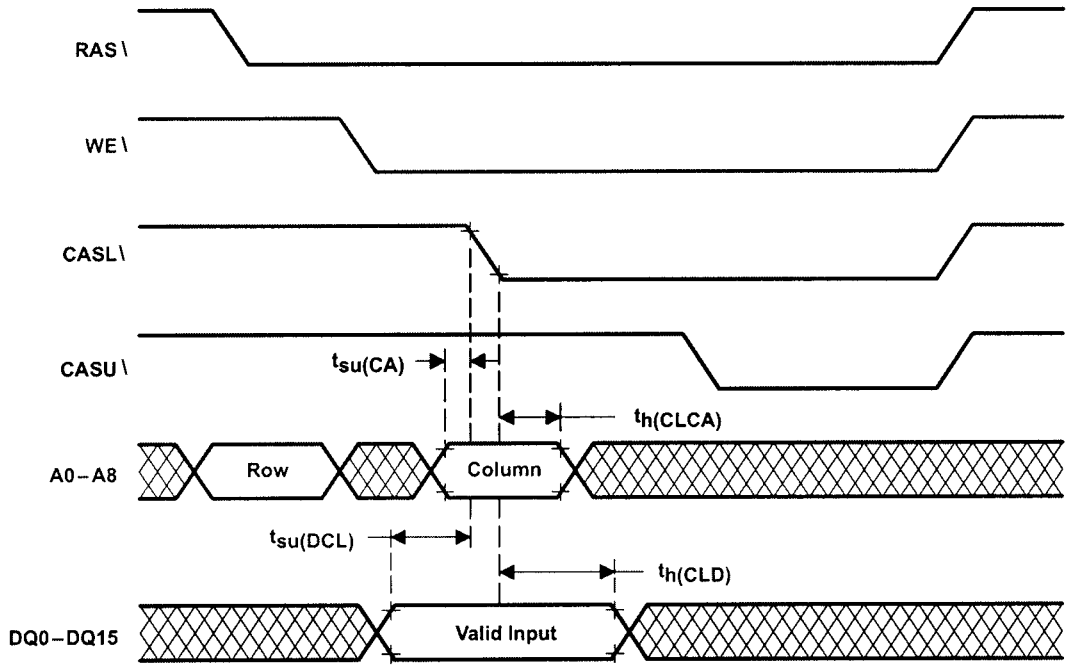
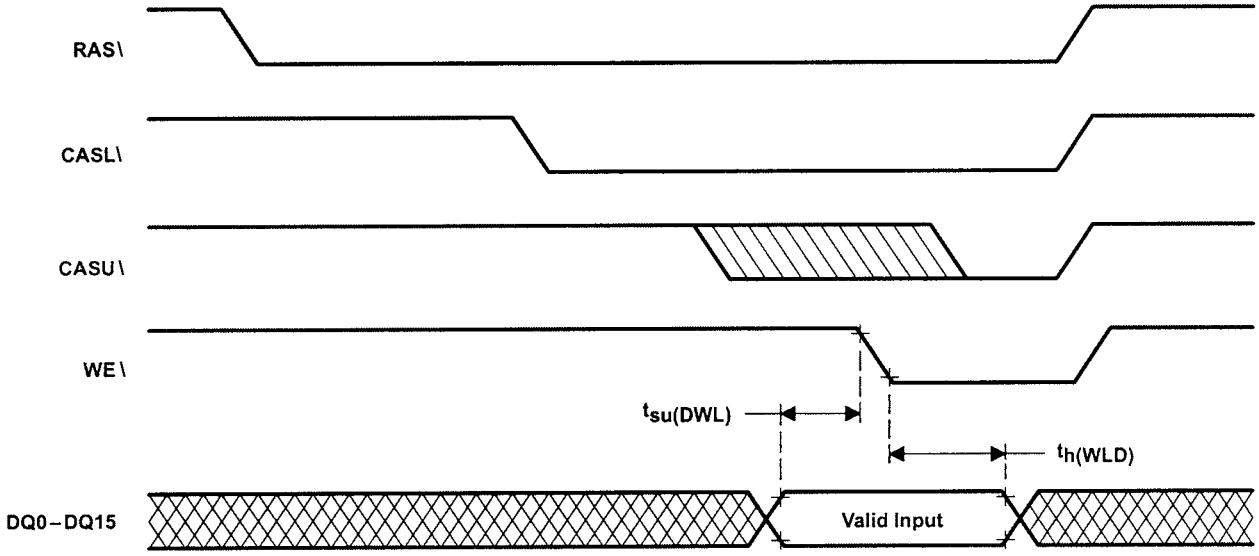


FIGURE 6: Example of a Late-Write Cycle



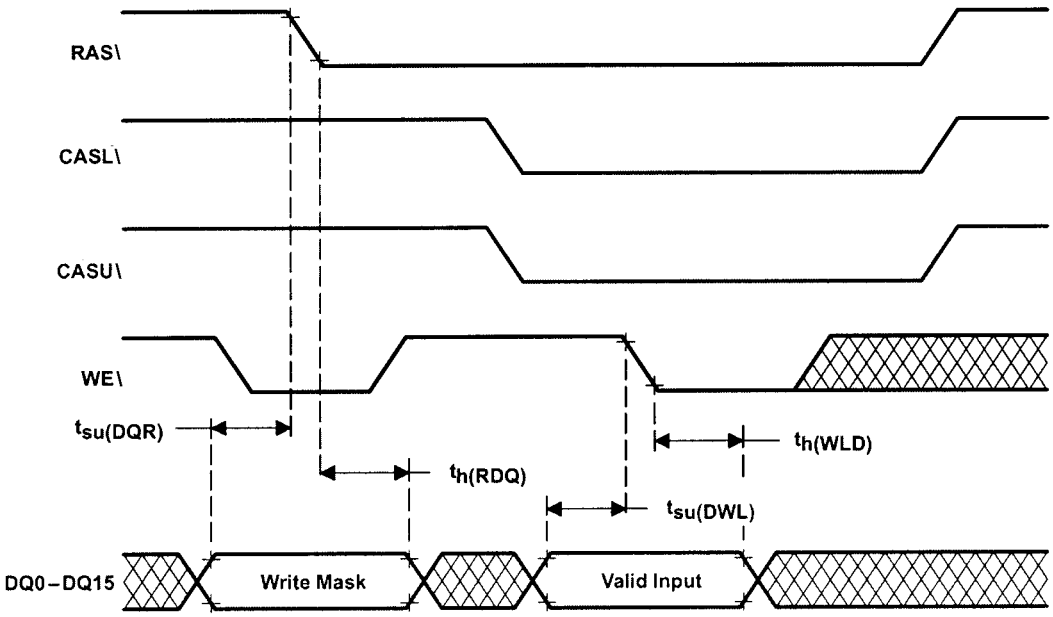
write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when WE\ is held low on the falling edge of RAS\. If WE\ is held high on the falling edge of RAS\, the write operation is performed without any masking. The SMJ55161A offers two write-per-bit modes: nonpersistent write-per-bit and persistent write-per-bit.

nonpersistent write-per-bit

When WE\ is low on the falling edge of RAS\, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device through the DQ pins and latched on the falling edge of RAS\. The write-per-bit mask selects which of the 16 I/Os are to be written and which are not. After RAS\ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later. CASL\ enables the lower byte (DQ0–DQ7) to be written through the mask and CASU\ enables the upper byte (DQ8–DQ15) to be written through the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of RAS\, data is not written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of RAS\, data is written to that I/O (see Figure 7).

FIGURE 7: Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

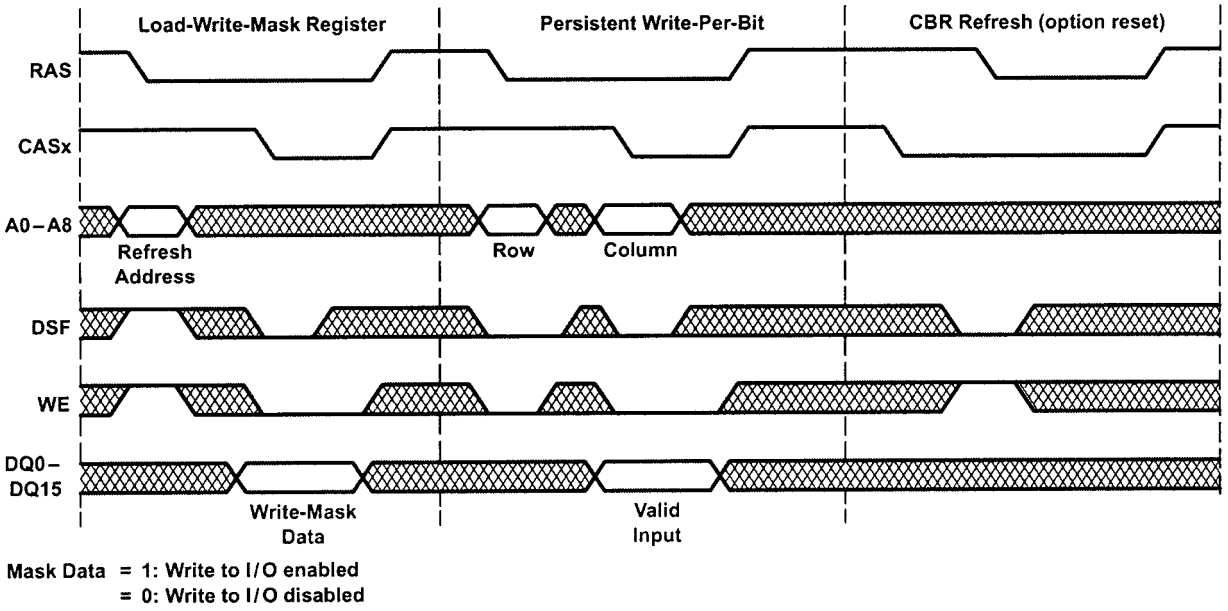


persistent write-per-bit

The persistent write-per-bit mode is initiated by performing a load-write-mask-register (LMR) cycle. In the persistent write-per-bit mode, the write-per-bit mask is overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The LMR cycle is performed using DRAM write-cycle timing with DSF held high on the falling edge of RAS\ and held low on the first falling edge of CASx\. A binary code is input to the write-mask register via the random I/O pins and latched on either the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later. Byte write control can be applied to the write mask during the LMR cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of RAS\ is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a CBR refresh (option-reset) cycle (see Figure 8).

FIGURE 8: Example of a Persistent Write-Per-Bit Operation



block write

The block-write feature allows up to 128 bits of data to be written simultaneously to one row of the memory array. This function is implemented as eight columns by eight DQs and repeated in two halves. In this manner, each of the two 2M-bit halves can have up to eight consecutive columns written at a time with up to eight DQs per column (see Figure 9).

Each 2M-bit half has a 8-bit column mask to mask off and prevent any or all of the eight columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write-masking options. The DQ data is provided by 8 bits from the on-chip color register. Bits 0–7 from the 16-bit write-mask register, bits 0 –7 from the 16-bit column-mask register, and bits 0 –7 from the 16-bit color-data register configure the block write for the first half, while bits 8 - 15 of the corresponding register control the other half in a similar fashion (see Figure 10).

FIGURE 9: Block-Write Operation

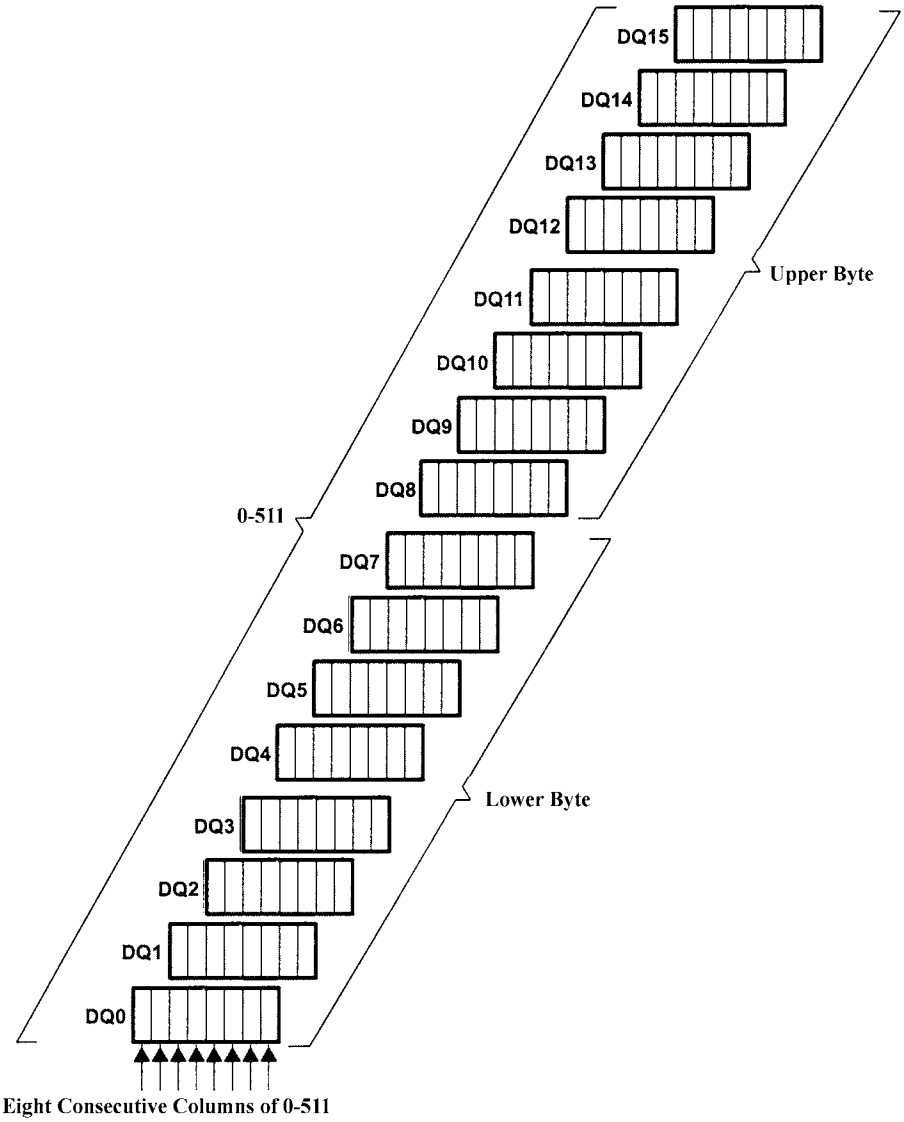
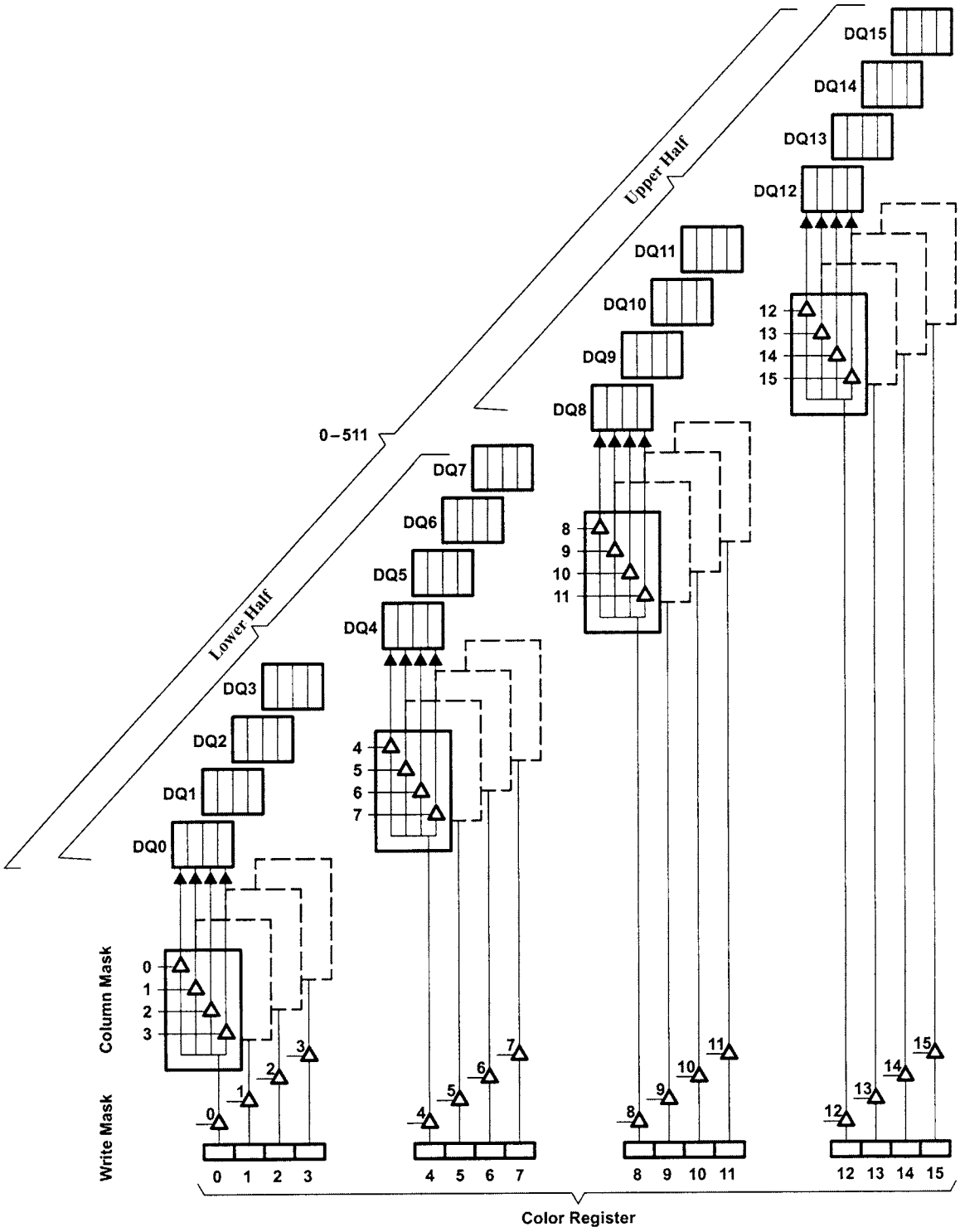


FIGURE 10: Block-Write With Masks



block write (continued)

A set of eight columns makes a block, resulting in 64 blocks along one row. Block 0 comprises columns 0 –7, block 1 comprises columns 7 –15, block 2 comprises columns 16 –23, etc., as shown in Figure 11.

During block-write cycles, only the six most significant column addresses (A3–A8) are latched on the first falling edge of CASx to decode one of the 64 blocks. Address bits A0–A2 are ignored. Each 2M-bit half has the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the first falling edge of CASx\. As in a DRAM write operation, CASL\ and CASU\ enable the corresponding lower and upper DRAM DQ bytes to be written. The column-mask data is input via the DQs and is latched on either the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability, allowing additional performance options.

Example of block write:
Block-write column address = 110000000
(A0–A8 from left to right)

	bit 0			bit 15
Color-data register =	1011	1011	1100	0111
Write-mask register =	1110	1111	1111	1011
Column-mask register =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column-address bits A0 and A2 are ignored. Block 0 (columns 0 –7) is selected for each 2M-bit half. The first half has DQ0–DQ2 written with bits 0–2 from the color-data register (101) to first four columns of block 0. DQ3 is not written and retains its previous data due to write-mask-register-bit 3 being 0. DQ4–DQ7 has all four columns masked off due to column-mask bits 4–7 being 0 so that no data is written.

The second half (DQ8–DQ11) has its four DQs written with bits 8 –11 from the color-data register (1100) to columns 1–3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to column-mask-register-bit 8 being 0.

DQ12–DQ15 has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for DQ12-DQ15 is all 0s, the upper half (DQ12-DQ15) contains the data pattern shown in Figure 12 after the block-write operation shown in the previous example.

FIGURE 12: Example of Upper DQ12-DQ15 After A Block-Write Operation With Previous Data Of 0

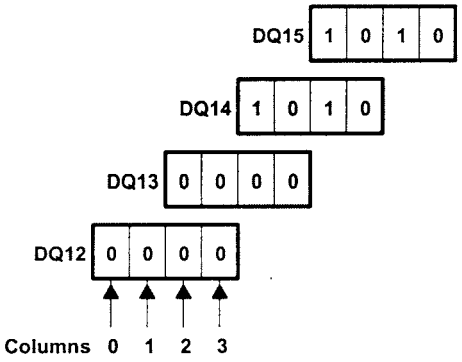
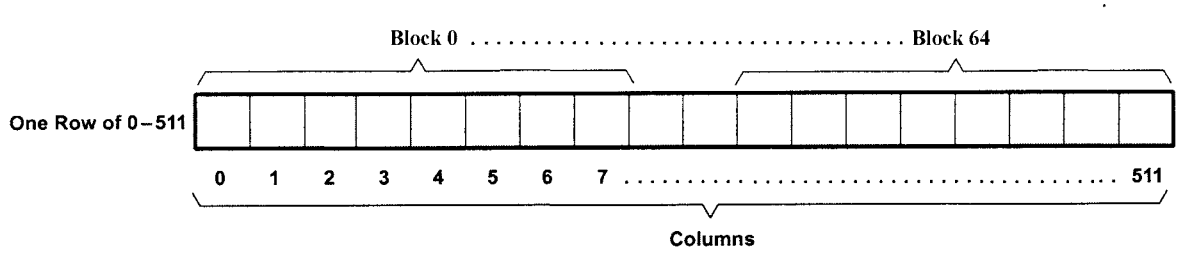


FIGURE 11: Block Columns Organization



load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of RAS\, CASL\, and CASU\. The color register is loaded from pins DQ0 –DQ15, which are latched on either the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later. If only one CASx\ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figure 13 and Figure 14).

FIGURE 13: Example of Block Writes

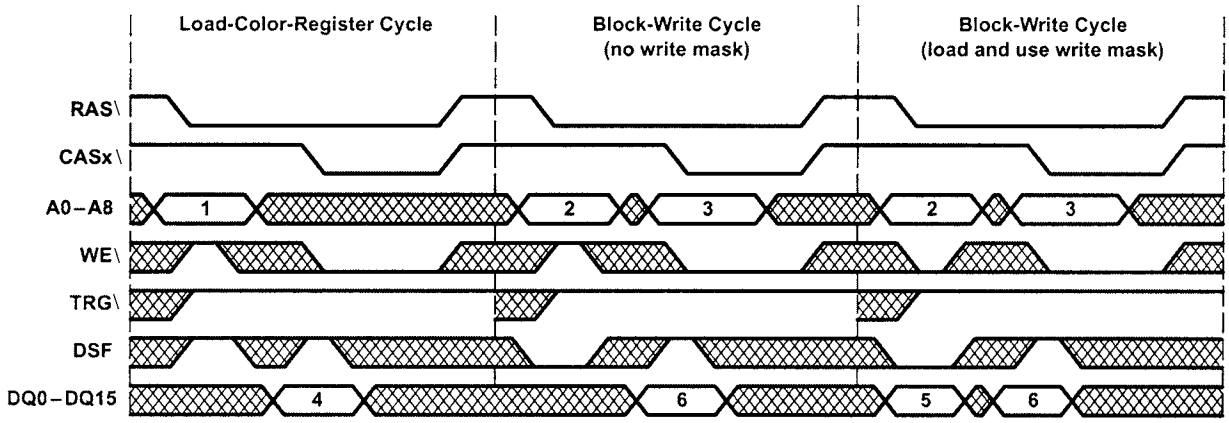
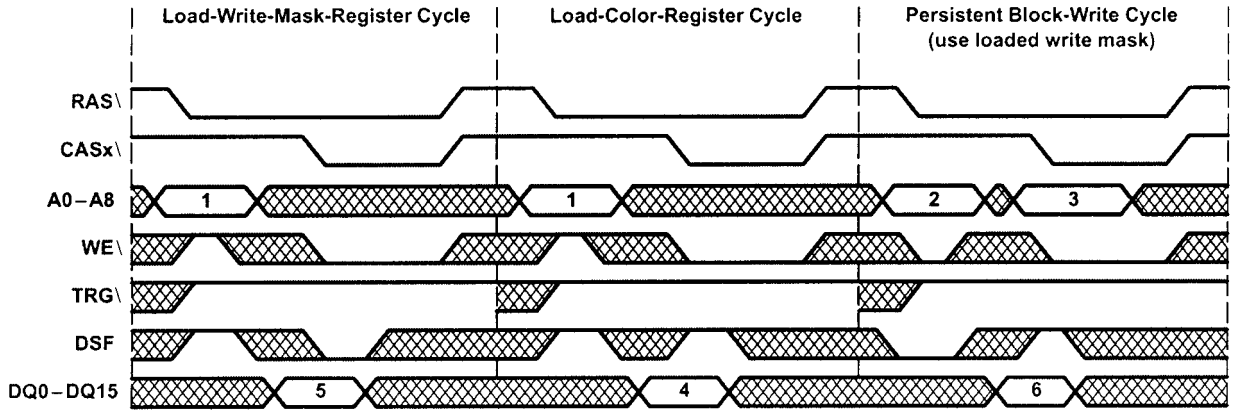


FIGURE 14: Example Of A Persistent Block Write



Legend:

1. Refresh address
2. Row address
3. Block address (A3–A8) is latched on the first falling edge of CASx\.
4. Color-register data
5. Write-mask data: DQ0–DQ15 are latched on the falling edge of RAS\.
6. Column-mask data: DQi–DQi+7 (i = 0, 8) are latched on either the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later.

= don't care

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one row (512 columns) in the DRAM array is selected to be transferred to the 512-bit serial-data register. The transfer operation is invoked by TRG\ being brought low and WE\ being held high on the falling edge of RAS\. The state of DSF, which is latched on the falling edge of RAS\, determines whether the full-register-transfer read operation or the split-register-transfer read operation is performed (see Table 4).

full-register-transfer read

A full-register-transfer read operation loads data from a selected half of a row in the DRAM into the SAM. TRG\ is brought low and latched at the falling edge of RAS\. Nine row-address bits (A0–A8) are also latched at the falling edge of RAS\ to select one of the 512 rows available for the transfer. The nine column-address bits (A0– A8) are latched at the first falling edge of CASx\. Address bits A0–A8 select one of the SAM's 512 available tap points from which the serial data is read out.

A full-register-transfer read can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the TRG\ trailing edge in the full-register-transfer read cycle (see Figure 15).

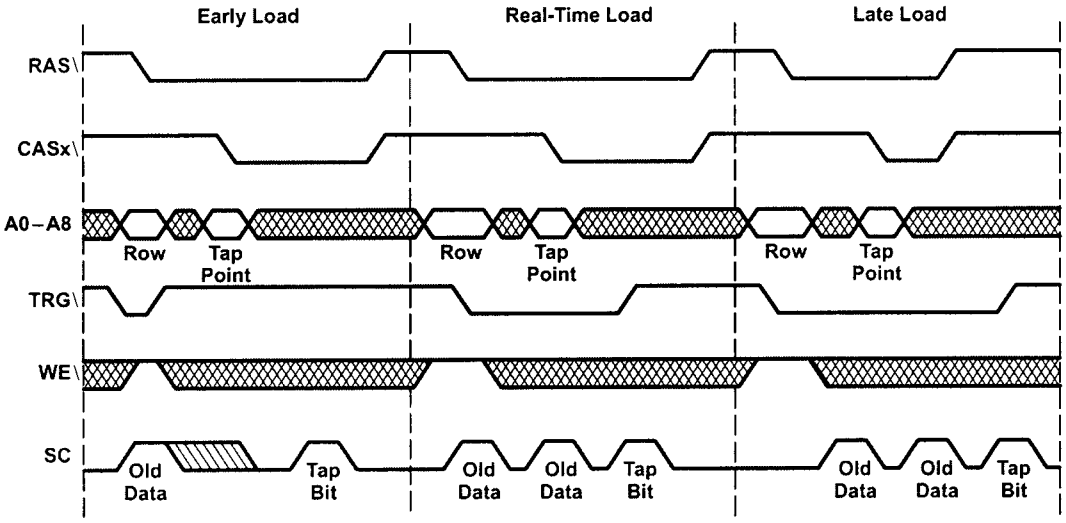
TABLE 4: SAM Fuction Table

FUNCTION	RAS\ FALL				CASx\ FALL	ADDRESS		DQ0-DQ15		MNE CODE
	CASx\[1]	TRG\	WE\	DSF	DSF	RAS\	CASX\	RAS\	CASx\ WE\	
Full-register-transfer Read	H	L	H	L	X	Row Address	Tap Point	X	X	RT
Split-register-transfer Read	H	L	H	H	X	Row Address	Tap Point	X	X	SRT

LEGEND:
X = Don't Care

NOTES:
1. Logic L is selected when either CASL\ or CASU\ are low.

FIGURE 15: Example of Full-Register-Transfer Read Operations



split-register-transfer read

The SMJ55161A features two types of bidirectional data transfer capability between DRAM and SAM.
1) Conventional (non split) transfer: 512 words by 16 bits of data can be loaded from DRAM to SAM (Read transfer), or from SAM to DRAM (write transfer).
2) Split transfer: 256 words by 16 bits of data can be loaded from the lower/upper half of the DRAM to the lower/uppper half of the SAM (Split read transfer), or from the lower/upper half to SAM to the lower/upper half of DRAM (Split write transfer).

The conventional transfer and split transfer modes are controlled by the DSF input signal. Data transfer is invoked by holding the TRG\ signal "low" at the falling edge of RAS\.

The SMJ55161A supports 4 types of transfer operations: Read transfer, Split read transfer, Write transfer and Split write transfer as shown in the truth table. The type of transfer operation is determined by the state of CAS\, WE\, and DSF latched at the falling edge of RAS\. During conventional transfer operations, the SAM port is switched from input to output mode (Read transfer), or output to input mode (Write transfer). It remains unchanged during split transfer operation (Split read transfer or Split write transfer).

Both DRAM and SAM are divided by the most significant row address (AX8), as shown in Figure 16. Therefore, no data transfer between AX8=0 side DRAM and AX8=1 side DRAM can be provided through the SAM. Care must be taken if the split read transfer on AX8=1 side (or AX8=0 side) is provided after the read transfer or the split read transfer, is provided on AX8=0 side (or AX8=1 side).

QSF indicates which half of the register is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 256 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 256 bits of the SAM. QSF changes state upon completing a full-register-transfer-read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

FIGURE 16: DRAM and SAM Configuration

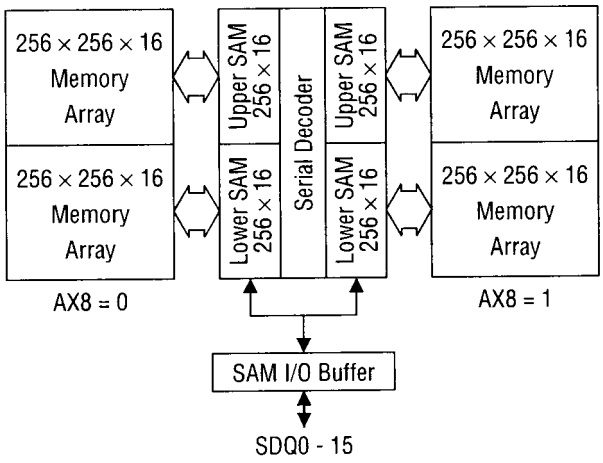


FIGURE 17: Example Of A Split-Register-Transfer Read After A Full-Register-Transfer Read

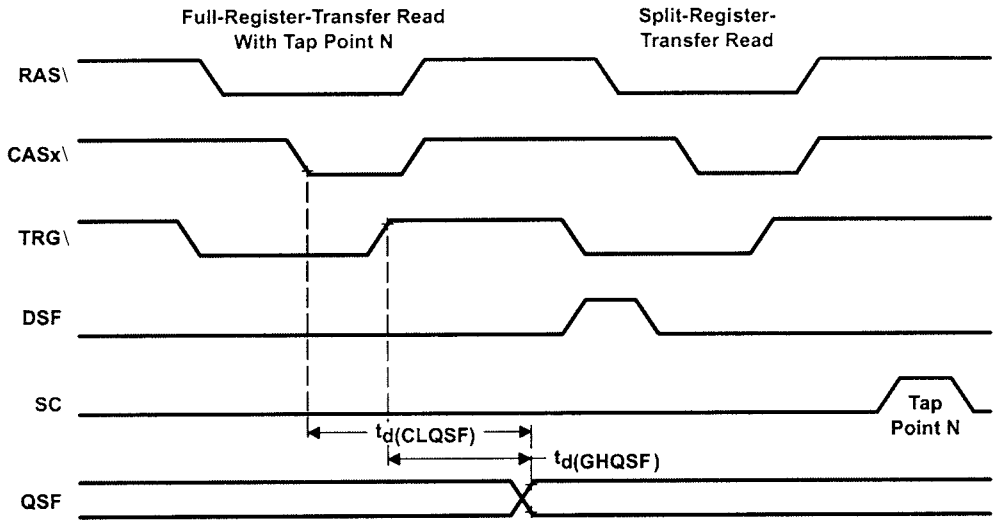
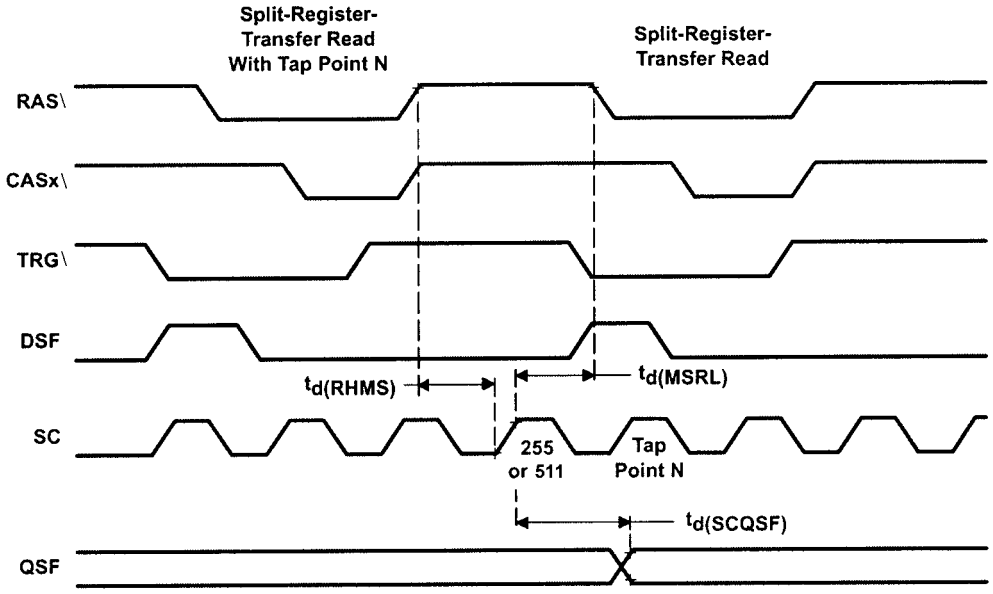


FIGURE 18: Example Of Successive Split-Register-Transfer-Read Operations



serial-read operation

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 255), and then wrapping around to the least significant bit (bit 0), as shown in Figure 19.

For split-register-transfer-read operation, serial data can be read out from the active half of the SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle. The serial pointer then proceeds sequentially to the most significant bit of the half, bit 255 or bit 511. If there is a split-register-transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register transfer (see Figure 20).

If there is no split-register-transfer read to the inactive half during this period, the serial pointer points next to bit 256 or bit 0, respectively (see Figure 21).

split-register programmable stop point

The SMJ55161A offers a programmable stop-point mode for split-register-transfer read operations. This mode can be used to improve two-dimensional drawing performance in a nonscanline data format.

For a split-register-transfer-read operation, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose length is programmed via row addresses A4–A7 in a CBR set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 22).

Figure 19: Serial-Pointer Direction for Serial Read

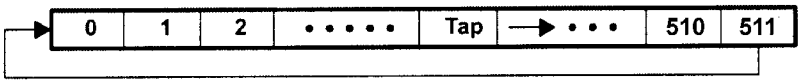


Figure 20: Serial Pointer for Split-Register Read - Case I

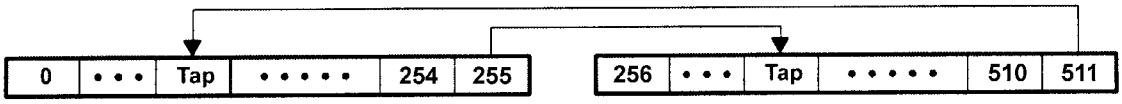


Figure 21: Serial Pointer for Split-Register Read - Case II

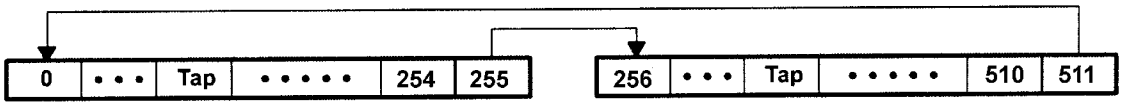
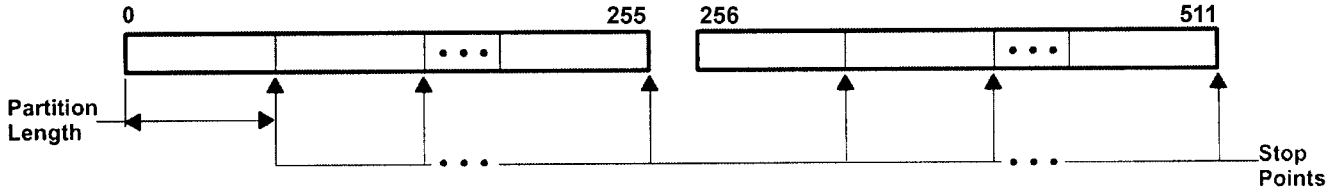


Figure 22: Example of the SAM with Partitions



split-register programmable stop point (continued)

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is enabled by holding CASx\ and WE\ low and DSF high on the falling edge of RAS\. The falling edge of RAS\ also latches row addresses A4–A7 which are used to define the SAM's partition length. The other row-address inputs are don't cares. Stop-point mode should be initiated after the initialization cycles are performed (see Table 5).

In stop-point mode, the tap point loaded during the split-register-transfer read cycle determines the SAM partition in which the serial output begins and at which stop point the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM (see Figure 23).

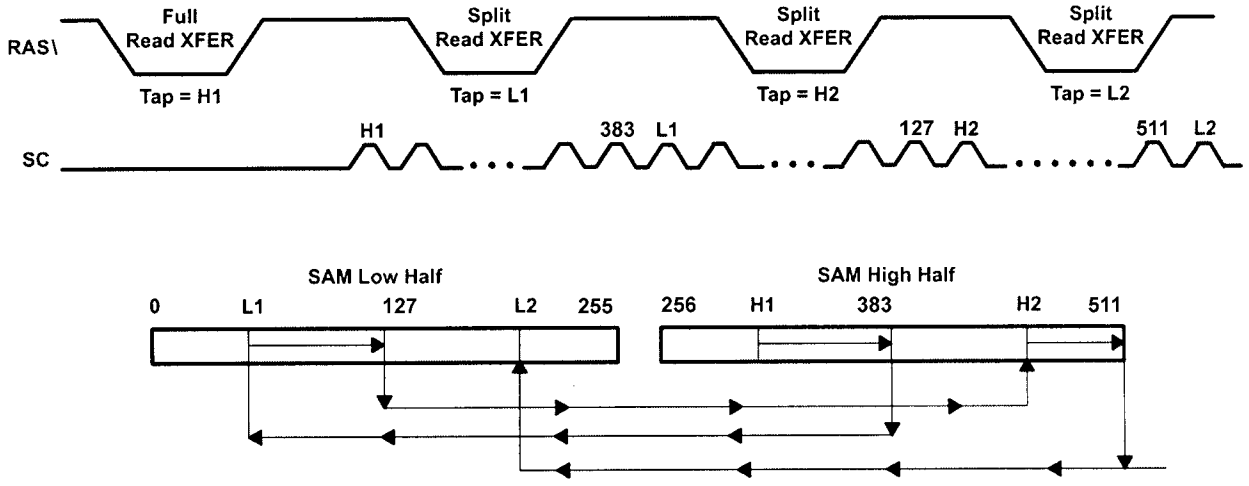
The stop-point mode of the previous revision 55161 is designed to be compatible with both 256-bit SAM and 512-bit SAM devices like the 55161A.

IMPORTANT: For proper device operation, a stop-point-mode (CBRS) cycle should be initiated immediately after the power-up initialization cycles are performed.

TABLE 5: Programming Code for Stop-Point Mode

MAX PARTITION LENGTH	ADDRESS AT RAS\ IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0 - A3		
16	X	L	L	L	L	X	16	31, 63, 95, 127, 159, 191, 223, 255, 287, 319, 351, 383, 415, 447, 479, 511
32	X	L	L	L	H	X	8	63, 127, 191, 255, 319, 383, 447, 511
64	X	L	L	H	H	X	4	127, 255, 383, 511
128	X	L	H	H	H	X	2	255, 511
256	X	H	H	H	H	X	1	255

FIGURE 23: Example of Split-Register Operation With Programmable Stop Points



power up

To achieve proper device operation, an initial pause of 200 ms is required after power up followed by a minimum of eight RAS\ cycles or eight CBR cycles to initialize the DRAM port. A full-register-transfer-read cycle and two SC cycles are required to initialize the SAM port.

After initialization, the internal state of the SMJ55161A is as shown in Table 6.

TABLE 6: Internal State of SMJ55161A

STATE	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write Mode	Nonpersistent Mode
Write-mask Register	Undefined
Color Register	Undefined
Serial-Register Tap Point	Defined by the transfer cycle during initialization
SAM Port	Output Mode

ABSOLUTE MAXIMUM RATINGS*

Supply voltage range, V_{CC}**.....-1V to +7 V
Voltage range on any pin.....-1V to +7 V
Short-circuit output current.....50mA
Power dissipation.....1.1W
Operating free-air temperature range, T_A.....-55°C to 125°C
Storage temperature range, T_{stg}.....-65°C to 150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**All voltage values are with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS

CONDITION	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5	5.5	V
Supply Voltage	V_{SS}		0		V
High-level input voltage	V_{IH}	2.4		V_{CC} +0.5	V
Low-level input voltage[1]	V_{IL}	-0.5		0.8	V
Operating free-air temperature	T_A	-55		125	°C

NOTES:

1. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE (UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	CONDITIONS	SAM PORT	-70		-75		-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
High-level output voltage	V_{OH}	V_{OH} = -1 mA		2.4		2.4		2.4		V
Low-level output voltage	V_{OL}	V_{OL} = 2 mA			0.4		0.4		0.4	V
Input current (leakage)	I_I	V_{CC} = 5.5V, V_I = 0V to 5.8V, All other pins at 0V to V_{CC}			±10		±10		±10	µA
Output current (leakage)[3]	I_O	V_{CC} = 5.5V, V_O = 0V to V_{CC}			±10		±10		±10	µA
Operating current[2]	I_{CC1}	See note 4	Standby		140		130		120	mA
Operating current[2]	I_{CC1A}	$t_{c(SC)}$ = MIN	Active		180		170		160	mA
Standby current	I_{CC2}	All clocks = V_{CC}	Standby		12		12		12	mA
Standby current	I_{CC2A}	tc(SC) = MIN	Active		60		55		50	mA
RAS\-only refresh current	I_{CC3}	See note 4	Standby		130		120		115	mA
RAS\-only refresh current	I_{CC3A}	tc(SC) = MIN[5]	Active		175		165		155	mA
Page-mode current[2]	I_{CC4}	tc(P) = MIN[5]	Standby		140		130		120	mA
Page-mode current2	I_{CC4A}	tc(SC) = MIN[5]	Active		190		180		170	mA
CBR current	I_{CC5}	See note 4	Standby		110		100		95	mA
CBR current	I_{CC5A}	tc(SC) = MIN[5]	Active		150		140		130	mA
Data-transfer current	I_{CC6}	See note 4	Standby		120		120		110	mA
Data-transfer current	I_{CC6A}	tc(SC) = MIN	Active		170		160		150	mA

NOTES:

1. For conditions shown as MAX/MIN, use the appropriate value specified in the timing requirements.
2. Measured with outputs open.
3. SE\ is disabled for SQ output leakage tests.
4. Measured with one address change while RAS\ = V_{IL}; $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN.
5. Measured with one address change while CASx\ = V_{IH}.

CAPACITANCE OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input capacitance, address inputs	$C_{i(A)}$		5	10	pF
Input capacitance, address-strobe inputs	$C_{i(RC)}$		8	10	pF
Input capacitance, write-enable input	$C_{i(W)}$		7	10	pF
Input capacitance, serial clock	$C_{i(SC)}$		6	10	pF
Input capacitance, serial enable	$C_{i(SE)}$		7	10	pF
Input capacitance, special function	$C_{i(DSF)}$		7	10	pF
Input capacitance, transfer-register input	$C_{i(TRG)}$		7	10	pF
Output capacitance, SQ and DQ	$C_{O(O)}$		12	15	pF
Output capacitance, QSF	$C_{O(QSF)}$		10	12	pF

NOTES: *V_{CC} = 5V ±0.5V, and the bias on pins under test is 0V.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE[1]

PARAMETER	SYMBOL	CONDITIONS[2]	-70		-75		-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Access time from CASx\	$t_{a(C)}$	$t_{d(RLCL)}$ = MAX		17		20		20	ns
Access time from column address	$t_{a(CA)}$			35		38		40	ns
Access time from CASx\ high	$t_{a(CP)}$			40		43		45	ns
Access time from RAS\	$t_{a(R)}$			70		75		80	ns
Access time of DQ from TRG\ low	$t_{a(G)}$			17		20		20	ns
Access time of SQ from SC high	$t_{a(SQ)}$	C_L = 30 pF		20		23		25	ns
Access time of SQ from SE\ low	$t_{a(SE)}$	C_L = 30 pF		17		18		20	ns
Disable time, random output from CASx\ high[3]	$t_{dis(CH)}$	C_L = 50 pF	0	17	0	20	0	20	ns
Disable time, random output from RAS\ high[3]	$t_{dis(RH)}$	C_L = 50 pF	0	17	0	20	0	20	ns
Disable time, random output from TRG\ high[3]	$t_{dis(G)}$	C_L = 50 pF	0	17	0	20	0	20	ns
Disable time, random output from WE\ low	$t_{dis(WL)}$	C_L = 50 pF	0	17	0	25	0	25	ns
Disable time, serial output from SE\ high	$t_{dis(SE)}$	C_L = 30 pF	0	15	0	18	0	20	ns

NOTES:

1. Switching times for RAM-port output are measured with a load equivalent to one TTL load and 50pF. Data-out reference level: V_{OH}/V_{OL} = 2V/0.8V. Switching times for SAM-port output are measured with a load equivalent to one TTL load and 30pF. Serial-data out reference level: V_{OH}/V_{OL} = 2V/0.8V.
2. For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
3. $t_{dis(CH)}$, $t_{dis(RH)}$, $t_{dis(G)}$, $t_{dis(WL)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE[1]

PARAMETER	SYMBOL	-70		-75		-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle time, read	$t_{c(rd)}$	124		140		150		ns
Cycle time, write	$t_{c(W)}$	124		140		150		ns
Cycle time, read-modify-write	$t_{c(rdW)}$	170		188		200		ns
Cycle time, page-mode read, write	$t_{c(P)}$	35		48		50		ns
Cycle time, page-mode read-modify-write	$t_{c(RDWP)}$	74		88		90		ns
Cycle time, transfer read	$t_{c(TRD)}$	130		140		150		ns
Cycle time, serial clock[2]	$t_{c(SC)}$	20		24		30		ns
Pulse duration, CASx\ high	$t_{w(CH)}$	10		10		10		ns
Pulse duration, CASx\ low[3]	$t_{w(CL)}$	15	10,000	20	10,000	20	10,000	ns
Pulse duration, RAS\ high	$t_{w(RH)}$	50		55		60		ns
Pulse duration, RAS\ low[4]	$t_{w(RL)}$	70	10,000	75	10,000	80	10,000	ns
Pulse duration, WE\ low	$t_{w(WL)}$	10		13		15		ns
Pulse duration, TRG\ low	$t_{w(TRG)}$	17		20		20		ns
Pulse duration, SC high	$t_{w(SCH)}$	7		9		10		ns
Pulse duration, SC low	$t_{w(SCL)}$	7		9		10		ns
Pulse duration, TRG\ high	$t_{w(GH)}$	20		20		20		ns
Pulse duration, RAS\ low (page mode)	$t_{w(RL)P}$	70	100,000	75	100,000	80	100,000	ns
Setup time, column address before CASx\ low	$t_{su(CA)}$	0		0		0		ns
Setup time, DSF before CASx\ low	$t_{su(SFC)}$	0		0		0		ns
Setup time, row address before RAS\ low	$t_{su(RA)}$	0		0		0		ns
Setup time, WE\ before RAS\ low	$t_{su(WMR)}$	0		0		0		ns
Setup time, DQ before RAS\ low	$t_{su(DQR)}$	0		0		0		ns
Setup time, TRG\ high before RAS\ low	$t_{su(TRG)}$	0		0		0		ns
Setup time, DSF low before RAS\ low	$t_{su(SFR)}$	0		0		0		ns
Setup time, data valid before CASx\ low	$t_{su(DCL)}$	0		0		0		ns
Setup time, data valid before WE\ low	$t_{su(DWL)}$	0		0		0		ns
Setup time, read command, WE\ high before CASx\ low	$t_{su(rd)}$	0		0		0		ns
Setup time, early-write command, WE\ low before CASx\ low	$t_{su(WCL)}$	0		0		0		ns
Setup time, WE\ low before CASx\ high, write	$t_{su(WCH)}$	15		18		20		ns
Setup time, WE\ low before RAS\ high, write	$t_{su(WRH)}$	17		20		20		ns
Hold time, column address after CASx\ low	$t_{h(CLCA)}$	10		13		15		ns
Hold time, DSF after CASx\ low	$t_{h(SFC)}$	12		15		15		ns
Hold time, row address after RAS\ low	$t_{h(RA)}$	10		10		10		ns
Hold time, TRG\ after RAS\ low	$t_{h(TRG)}$	12		15		15		ns
Hold time, write mask after RAS\ low	$t_{h(RWM)}$	12		15		15		ns
Hold time, DQ after RAS\ low (write-mask operation)	$t_{h(RDQ)}$	12		15		15		ns

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE (continued)[1]

PARAMETER	SYMBOL	-70		-75		-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Hold time, DSF after RAS\ low	$t_{h(SFR)}$	10		10		10		ns
Hold time, column address valid after RAS\ low[5]	$t_{h(RLCA)}$	30		33		35		ns
Hold time, data valid after CASx\ low	$t_{h(CLD)}$	12		15		15		ns
Hold time, data valid after RAS\ low[5]	$t_{h(RLD)}$	30		35		35		ns
Hold time, data valid after WE\ low	$t_{h(WLD)}$	12		15		15		ns
Hold time, read, WE\ high after CASx\ high[6]	$t_{h(CHrd)}$	0		0		0		ns
Hold time, read, WE\ high after RAS\ high[6]	$t_{h(RHrd)}$	0		0		0		ns
Hold time, write, WE\ low after CASx\low	$t_{h(CLW)}$	12		15		15		ns
Hold time, write, WE\ low after RAS\ low[5]	$t_{h(RLW)}$	30		35		35		ns
Hold time, TRG\ high after WE\ low[7]	$t_{h(WLG)}$	10		10		10		ns
Hold time, SQ valid after SC high	$t_{h(SHSQ)}$	2		2		2		ns
Hold time, DSF after RAS\ low	$t_{h(RSF)}$	30		35		35		ns
Hold time, output valid after CASx\ low	$t_{h(CLQ)}$	0		0		0		ns
Delay time, RAS\ low to CASx\ high	$t_{d(RLCH)}$	70		75		80		ns
See Note 8	$t_{d(RLCH)}$	10		13		15		
Delay time, CASx\ high to RAS\ low	$t_{d(CHRL)}$	7		5		5		ns
Delay time, CASx\ low to RAS\ high	$t_{d(CLRH)}$	17		20		20		ns
Delay time, CASx\ low to WE\ low[9,10]	$t_{d(CLWL)}$	40		48		50		ns
Delay time, RAS\ low to CASx\ low[11]	$t_{d(RLCL)}$	15	50	20	50	20	60	ns
Delay time, column address valid to RAS\ high	$t_{d(CARH)}$	35		38		40		ns
Delay time, column address valid to CASx\ high	$t_{d(CACH)}$	35		38		40		ns
Delay time, RAS\ low to WE\ low[9]	$t_{d(RLWL)}$	90		100		105		ns
Delay time, column address valid to WE\ low[9]	$t_{d(CAWL)}$	55		63		65		ns
Delay time, CASx\ low to RAS\ low[8]	$t_{d(CLRL)}$	5		5		5		ns
Delay time, RAS\ high to CASx\ low[8]	$t_{d(RHCL)}$	0		0		0		ns
Delay time, CASx\ low to TRG\ high for DRAM read cycles	$t_{d(CLGH)}$	20		20		20		ns
Delay time, TRG\ high before data applied at DQ	$t_{d(GHD)}$	15		15		15		ns
Delay time, RAS\ low to TRG\ high[12]	$t_{d(RLTH)}$	55		58				ns
Delay time, RAS\ low to first SC high after TRG\ high[13]	$t_{d(RLSH)}$	70		75				ns
Delay time, RAS\ low to column address valid	$t_{d(RLCA)}$	12	35	15	35	15	40	ns
Delay time, TRG\ low to RAS\ high	$t_{d(GLRH)}$	15		20		20		ns
Delay time, CASx\ low to first SC high after TRG\ high[13]	$t_{d(CLSH)}$	20		23		25		ns
Delay time, SC high to TRG\ high[12, 13]	$t_{d(SCTR)}$	5		5		5		ns
Delay time, TRG\ high to RAS\ high[12]	$t_{d(THRH)}$	-10		-10		-10		ns
Delay time, TRG\ high to RAS\ low[14]	$t_{d(THRL)}$	50		55		60		ns
Delay time, TRG\ high to SC high[12]	$t_{d(THSC)}$	15		18		20		ns

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE (continued)[1]

PARAMETER	SYMBOL	-70		-75		-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Delay time, RAS\ high to last (most significant) rising edge of SC before boundary switch during split-register-transfer read cycles	$t_{d(RHMS)}$	20		20		20		ns
Delay time, CASx\ low to TRG\ high in read-time-transfer read cycles	$t_{d(CLTH)}$	17		15		15		ns
Delay time, column address to first SC in early-load-transfer read cycles	$t_{d(CASH)}$	25		28		30		ns
Delay time, column address to TRG\ high in real-time-transfer read cycles	$t_{d(CAGH)}$	20		20		20		ns
Delay time, data to CASx\ low	$t_{d(DCL)}$	0		0		0		ns
Delay time, data to TRG\ low	$t_{d(DGL)}$	0		0		0		ns
Delay time, last (most significant) rising edge of SC to RAS\ low before boundary switch during split-register-transfer read cycles	$t_{d(MSRL)}$	20		20		20		ns
Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register-transfer read cycles[15]	$t_{d(SCQSF)}$		25		28		30	ns
Delay time, CASx\ low to QSF switching in transfer-read cycles[15]	$t_{d(CLQSF)}$		30		33		35	ns
Delay time, TRG\ high to QSF switching in transfer-read cycles[15]	$t_{d(GHQSF)}$		25		28		30	ns
Delay time, RAS\ lwo to QSF switching in transfer-read cycles[15]	$t_{d(RLQSF)}$		70		73		75	ns
Refresh time interval, memory	$t_{rf(MA)}$		8		8		8	ms
Transition time	t_t	3	25	3	25	3	25	ns

NOTE:

1. Timing measurements are referenced to V_{IL} MAX and V_{IH} MIN.
2. Cycle time assumes tt = 3 ns.
3. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the transition times, this can require additional CASx\ low time [$t_{w(CL)}$].
4. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the transition times, this can require additional RAS\ low time [$t_{w(RL)}$].
5. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ MIN as a reference.
6. Either $t_{h(RHrd)}$ or $t_{d(CHrd)}$ must be satisfied for a read cycle.
7. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
8. CBR refresh operation only.
9. Read-modify-write operation only.
10. TRG\ must disable the output buffers prior to applying data to the DQ pins.
11. The maximum value is specified only to assure RAS\ access time.
12. Real-time-load transfer read or late-load-transfer read cycle only.
13. Early-load-transfer read cycle only.
14. Full-register-(read) transfer cycles only.
15. Switching times for QSF output are measured with a load equivalent to one TTL load and 30 pF, and the output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

SAM TO DRAM WRITE TRANSFER & SERIAL IN TIMINGS

PARAMETER	SYMBOL	-70	-75	-80	UNITS
Last SC to RAS\ set-up time (serial input)	t_{SRS}	25	25	25	ns
RAS\ to serial input delay time	t_{SDD}	35	40	45	ns
Serial input set-up time	t_{SDS}	0	0	0	ns
Serial input hold time	t_{SDH}	0	0	0	ns
Serial input to SE\ delay time	t_{SZE}	0	0	0	ns
Serial input to first SC delay time	t_{SZS}	0	0	0	ns
Serial write enable to set-up time	t_{SWS}	0	0	0	ns
Serial write enable to hold time	t_{SWH}	10	12	12	ns
Serial write disable to set-up time	t_{SWiS}	0	0	0	ns
Serial write disable to hold time	t_{SWiH}	10	12	12	ns

FIGURE 24: READ-CYCLE TIMING WITH CASx\-CONTROLLED OUTPUT

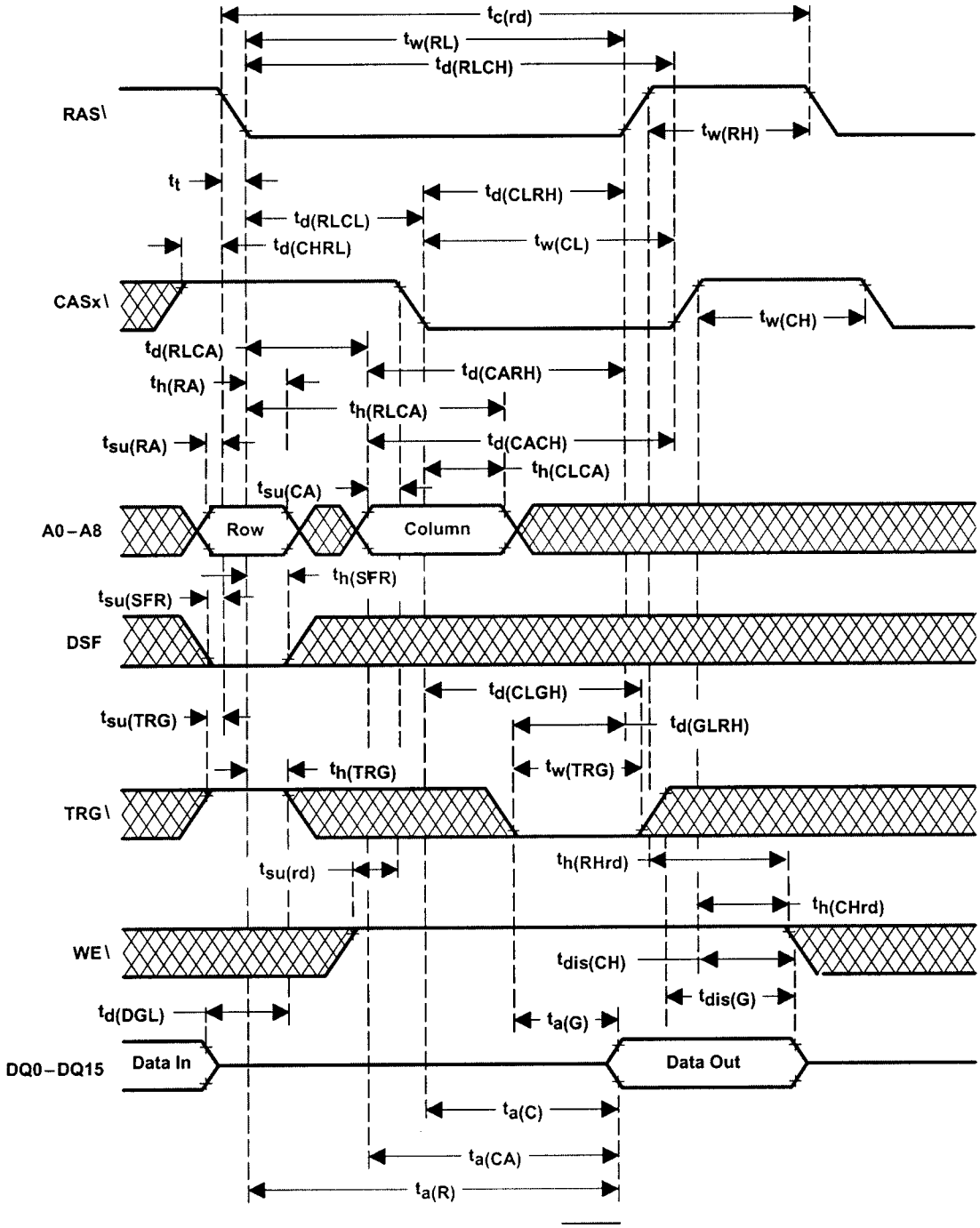


FIGURE 25: READ-CYCLE TIMING WITH RAS\-CONTROLLED OUTPUT

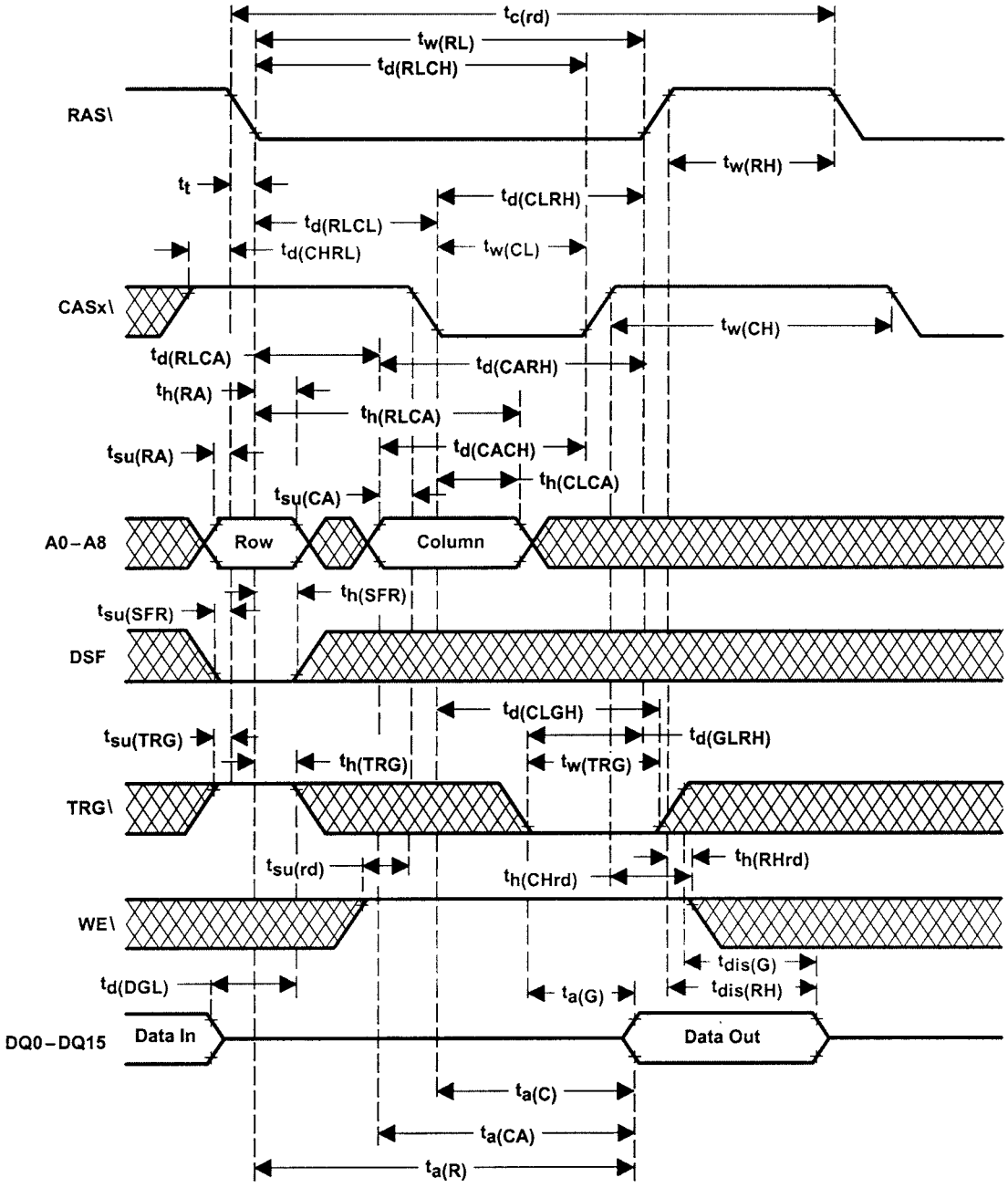


FIGURE 26: EARLY-WRITE-CYCLE TIMING

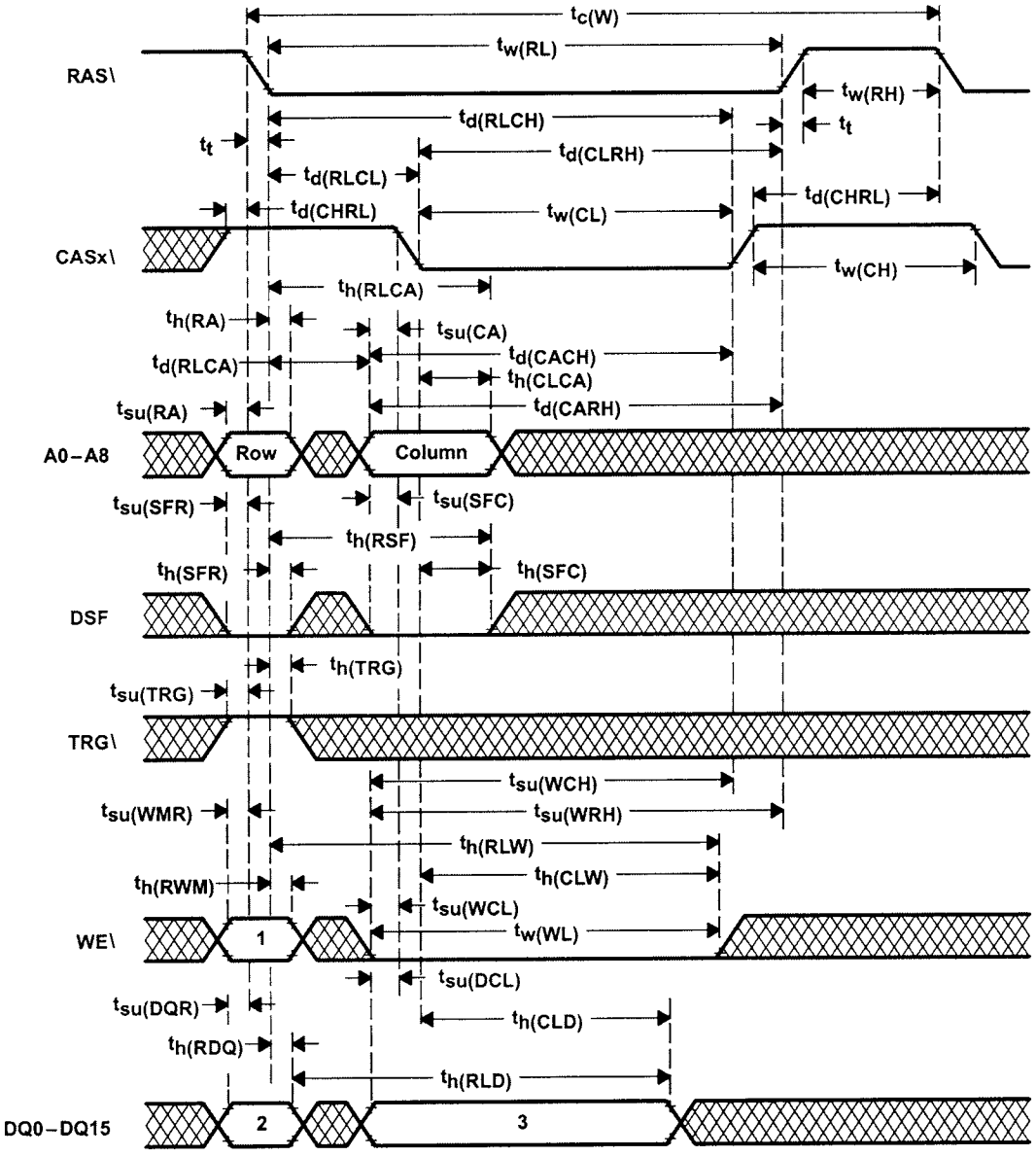


TABLE 7: EARLY-WRITE-CYCLE STATE TABLE

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't Care	Valid Data
Write operation with nonpersistent write-per-bit	L	Write Mask	Valid Data
Write operation with persistent write-per-bit	L	Don't Care	Valid Data

FIGURE 27: LATE-WRITE-CYCLE TIMING (OUTPUT-ENABLE-CONTROLLED WRITE)

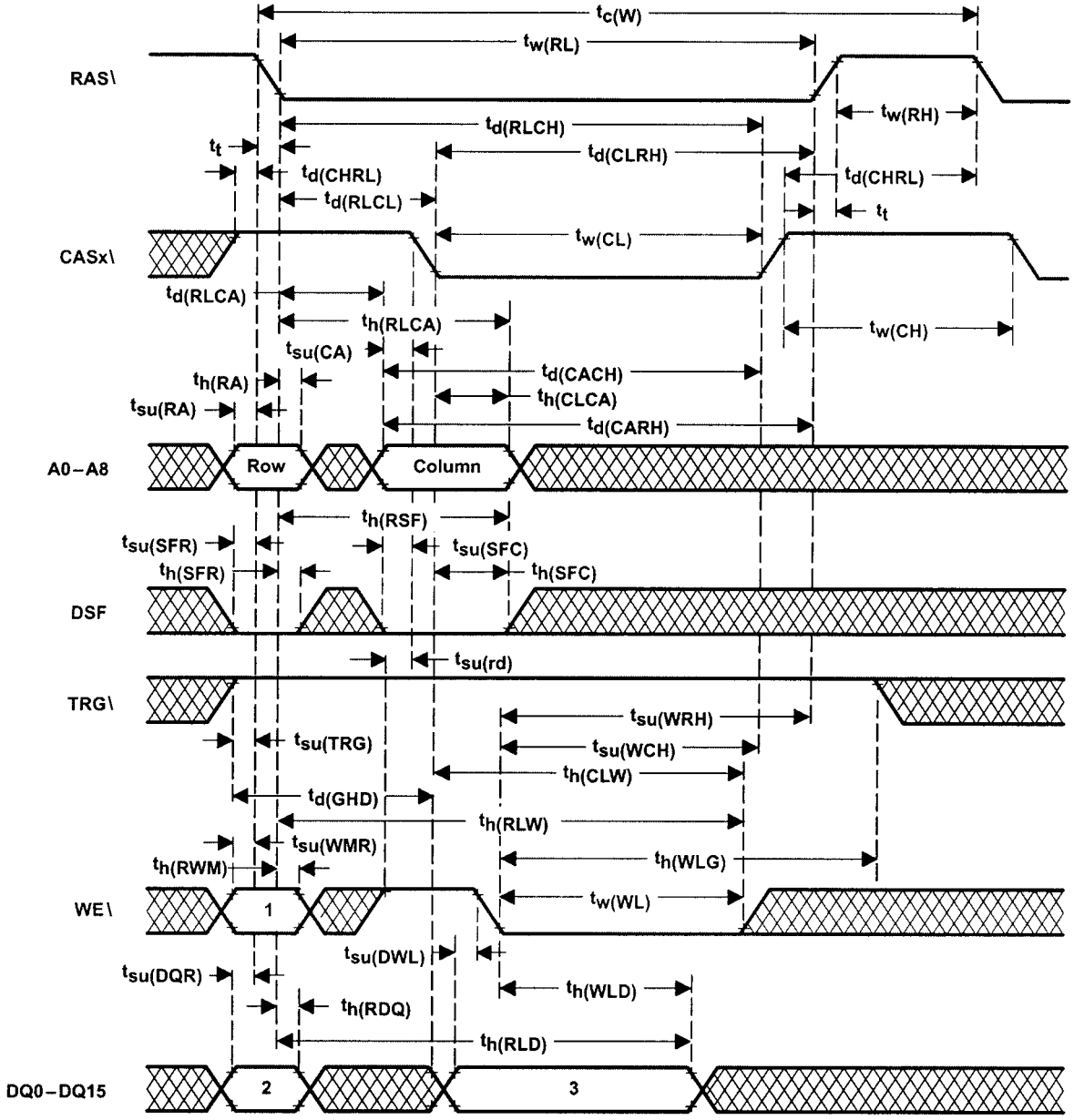
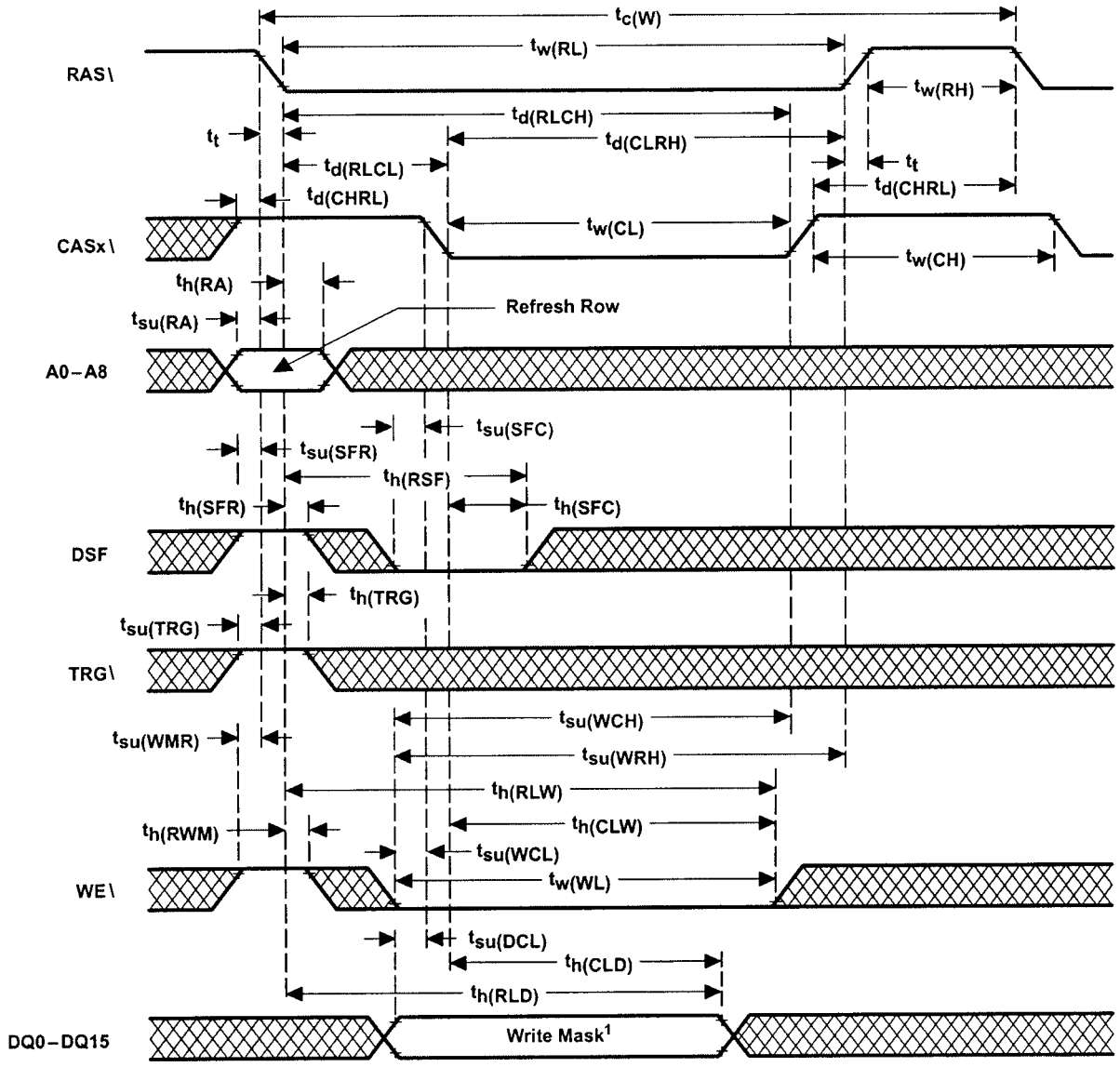


TABLE 8: LATE-WRITE-CYCLE STATE TABLE

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't Care	Valid Data
Write operation with nonpersistent write-per-bit	L	Write Mask	Valid Data
Write operation with persistent write-per-bit	L	Don't Care	Valid Data

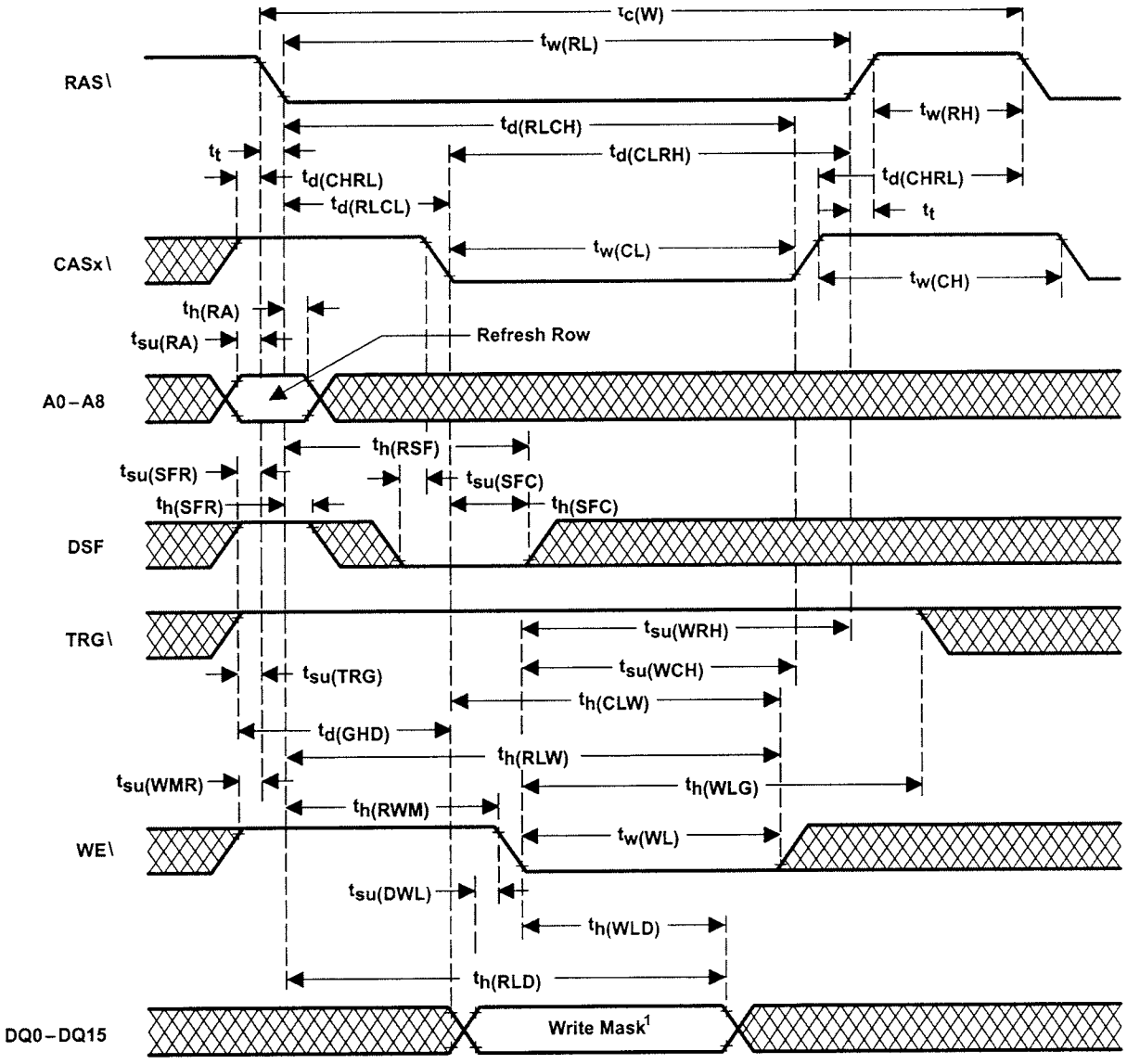
FIGURE 28: LOAD-WRITE-MASK-REGISTER-CYCLE TIMING (EARLY-WRITE LOAD)



NOTES:

1. Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

FIGURE 29: LOAD-WRITE-MASK-REGISTER-CYCLE TIMING (LATE-WRITE LOAD)



NOTES:

1. Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

FIGURE 30: READ-WRITE/READ-MODIFY-WRITE-CYCLE TIMING

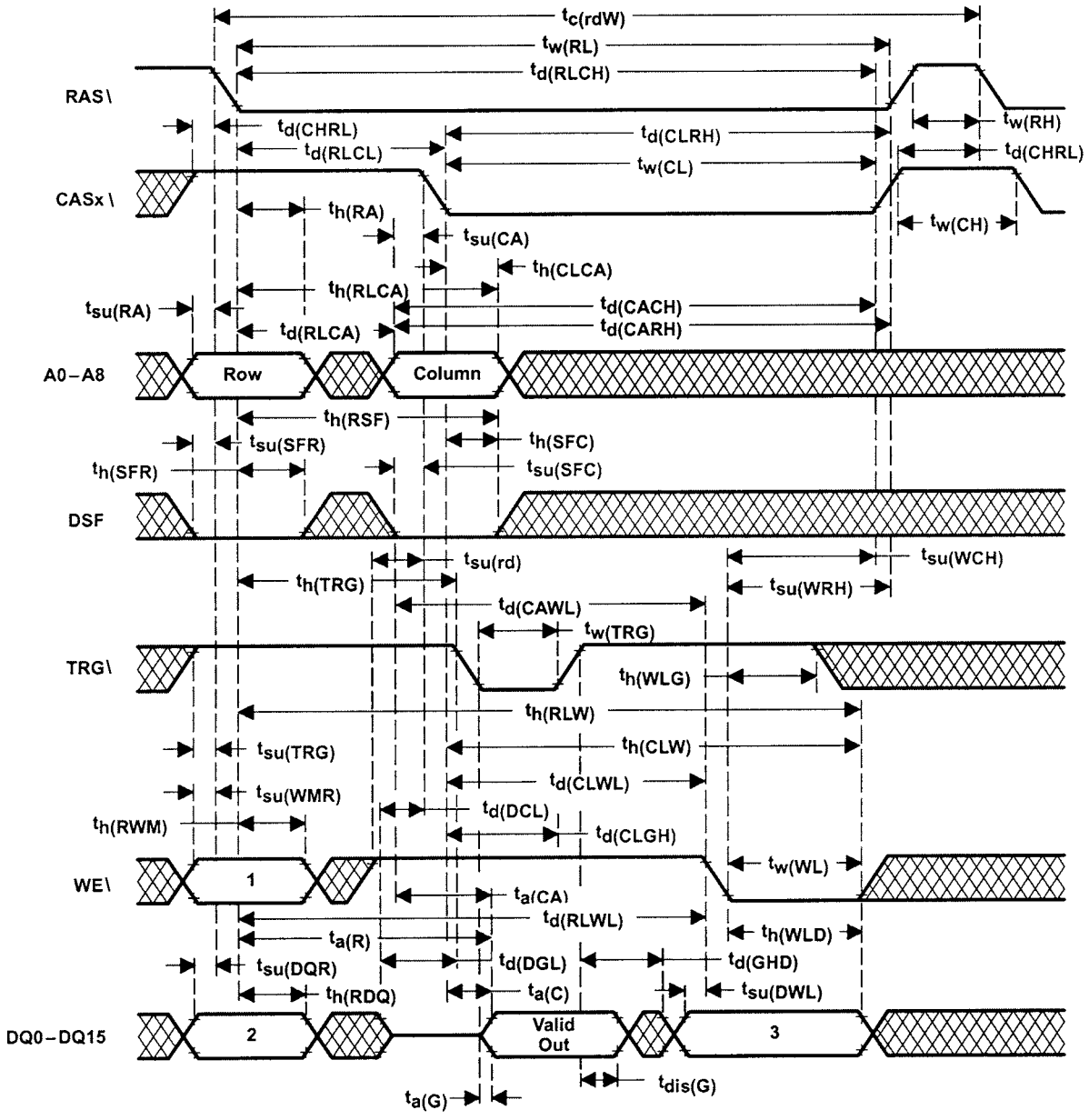
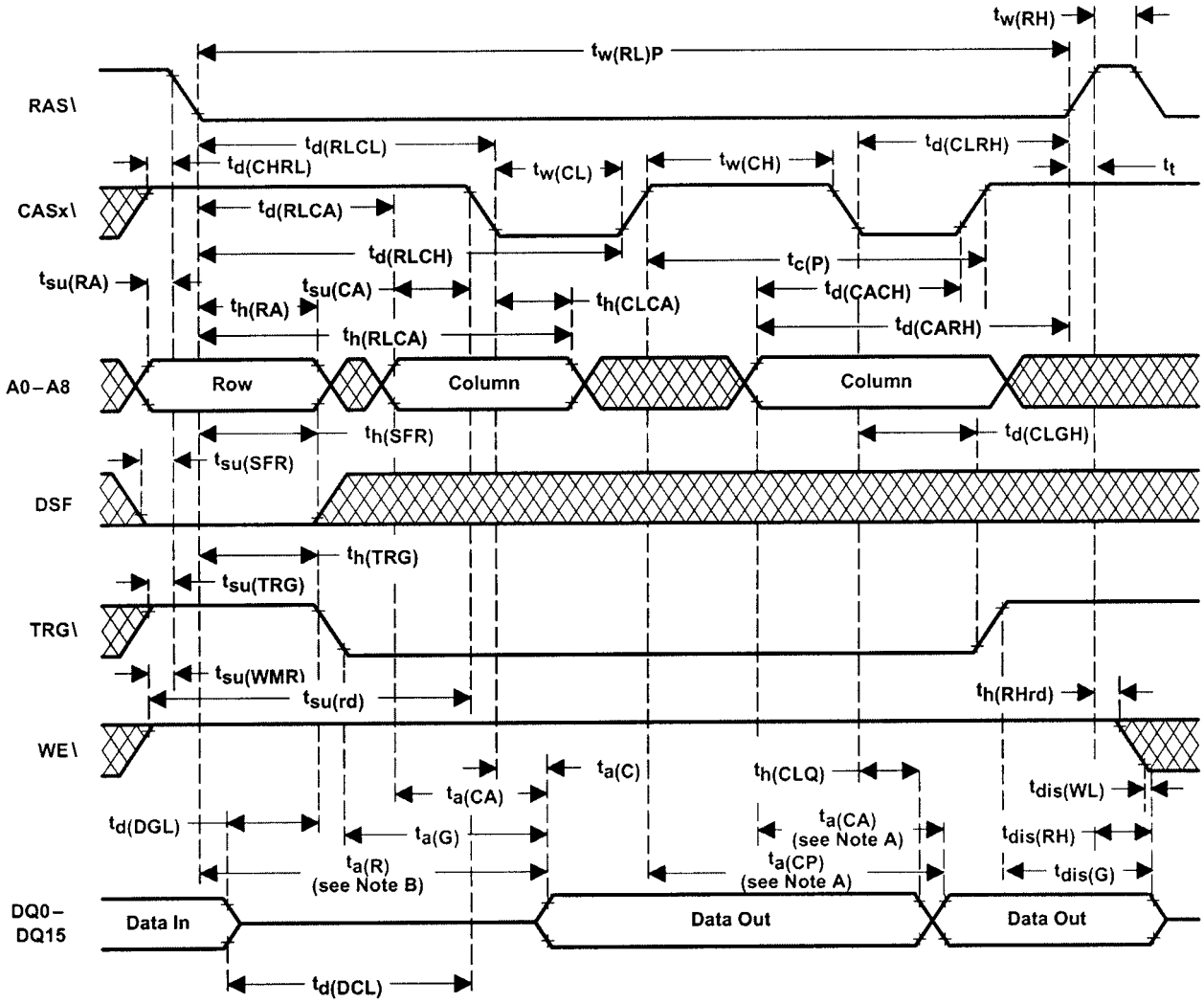


TABLE 9: READ-WRITE/READ-MODIFY-WRITE-CYCLE STATE TABLE

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't Care	Valid Data
Write operation with nonpersistent write-per-bit	L	Write Mask	Valid Data
Write operation with persistent write-per-bit	L	Don't Care	Valid Data

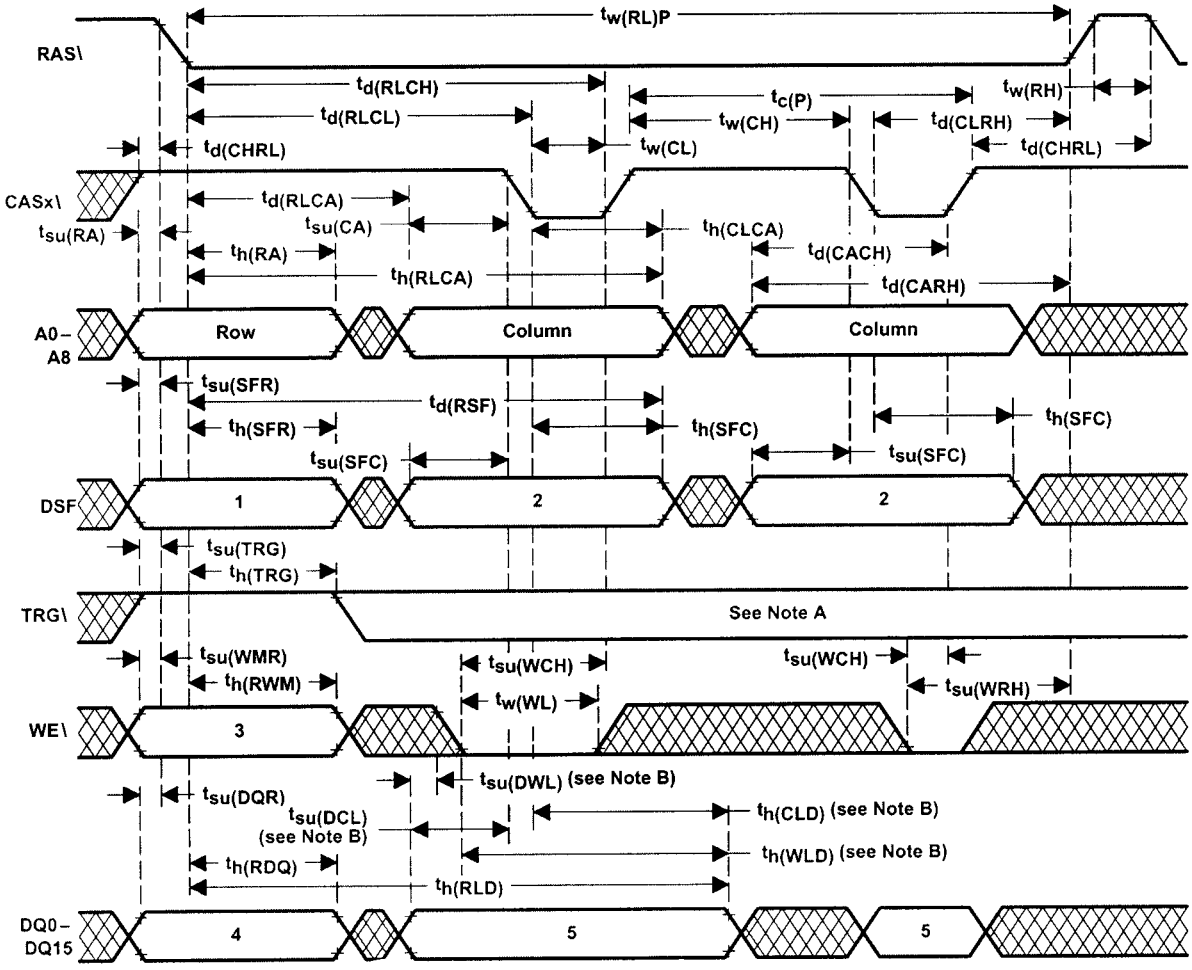
FIGURE 31: ENHANCED-PAGE-MODE READ-CYCLE TIMING



NOTES:

A. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of RAS\ and CASx\ to select the desired write mode (normal, block write, etc.).

FIGURE 32: ENHANCED-PAGE-MODE WRITE-CYCLE TIMING



NOTES:

A. Referenced to the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later

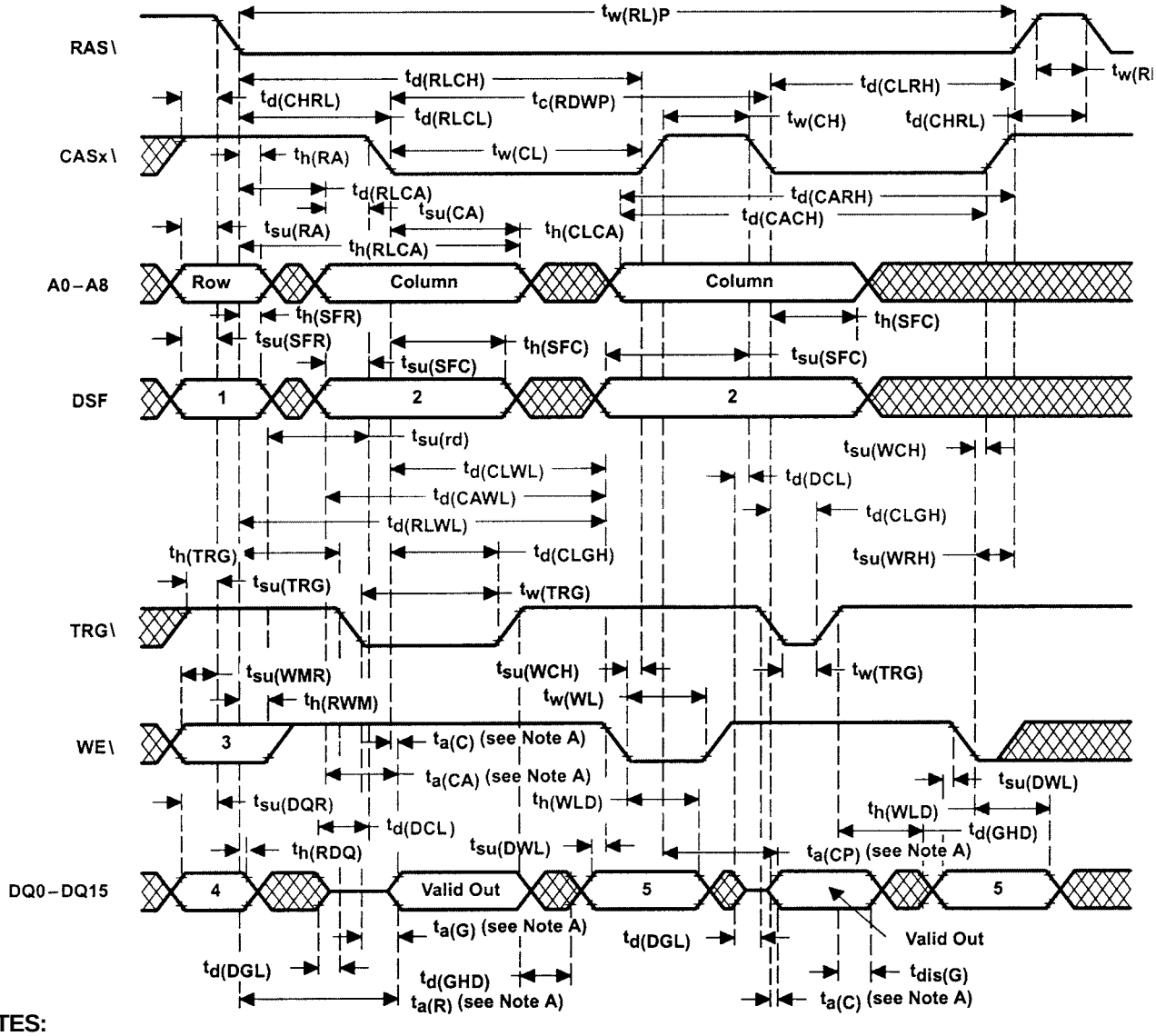
B. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To ensure page-mode cycle time, TRG\ must remain high throughout the entire page-mode operation if the late write feature is used. If the early write-cycle timing is used, the state of TRG\ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of RAS\..

TABLE 10: ENHANCED-PAGE-MODE WRITE-CYCLE STATE TABLE

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't Care	Valid Data
Write operation with nonpersistent write-per-bit	L	L	L	Write Mask	Valid Data
Write operation with persistent write-per-bit	L	L	L	Don't Care	Valid Data
Load-write mask on either the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later.[1]	H	L	H	Don't Care	Write Mask

NOTES: 1. Load-write-mask-register cycle puts the device in the persistent write-per-bit mode. Column address at the falling edge of CASx\ is a don't care during this cycle.

FIGURE 33: ENHANCED-PAGE-MODE READ-MODIFY-WRITE-CYCLE TIMING



NOTES:

A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

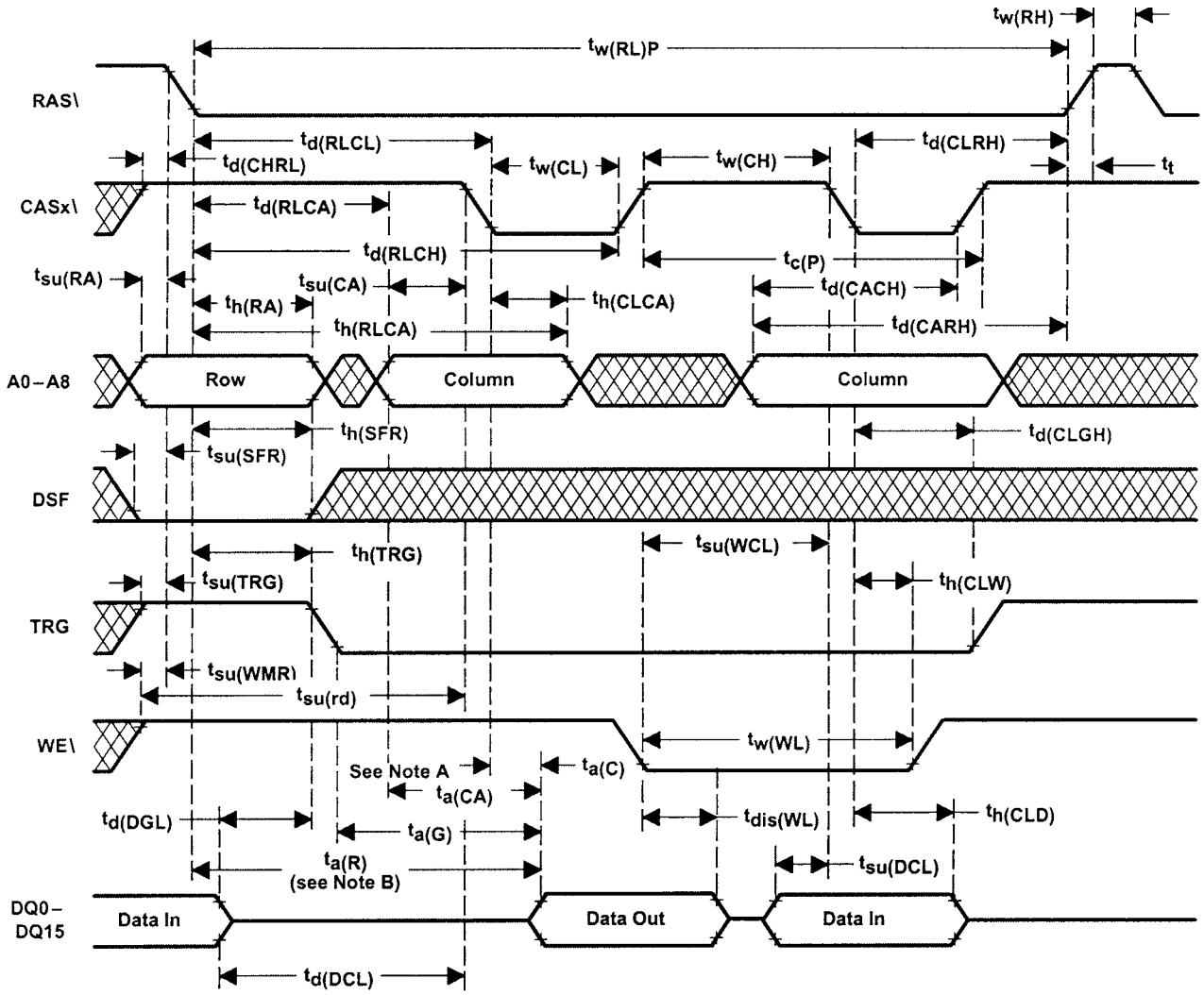
B. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

TABLE 11: ENHANCED-PAGE-MODE READ-MODIFY-WRITE-CYCLE STATE TABLE

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't Care	Valid Data
Write operation with nonpersistent write-per-bit	L	L	L	Write Mask	Valid Data
Write operation with persistent write-per-bit	L	L	L	Don't Care	Valid Data
Load-write mask on either the first falling edge of CASx\ or the falling edge of WE\, whichever occurs later.[1]	H	L	H	Don't Care	Write Mask

NOTES: 1. Load-write-mask-register cycle puts the device in the persistent write-per-bit mode. Column address at the falling edge of CASx\ is a don't care during this cycle.

FIGURE 34: ENHANCED-PAGE-MODE READ-/WRITE-CYCLE TIMING



NOTES:

A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

B. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of RAS\ and CASx\ to select the desired write mode (normal, block write, etc.).

FIGURE 35: LOAD-COLOR-REGISTER-CYCLE TIMING (EARLY-WRITE LOAD)

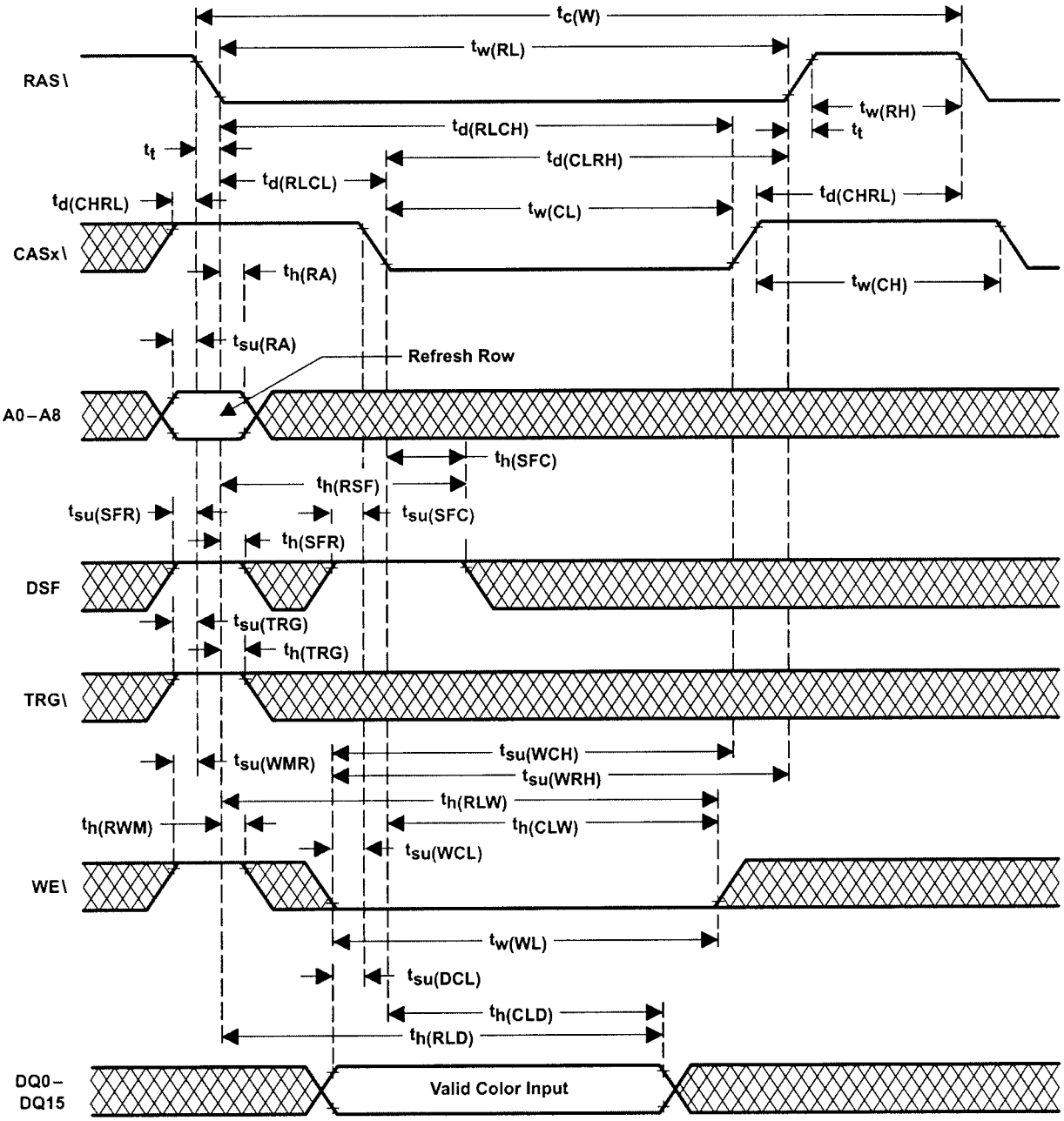


FIGURE 36: LOAD-COLOR-REGISTER-CYCLE TIMING (LATE-WRITE LOAD)

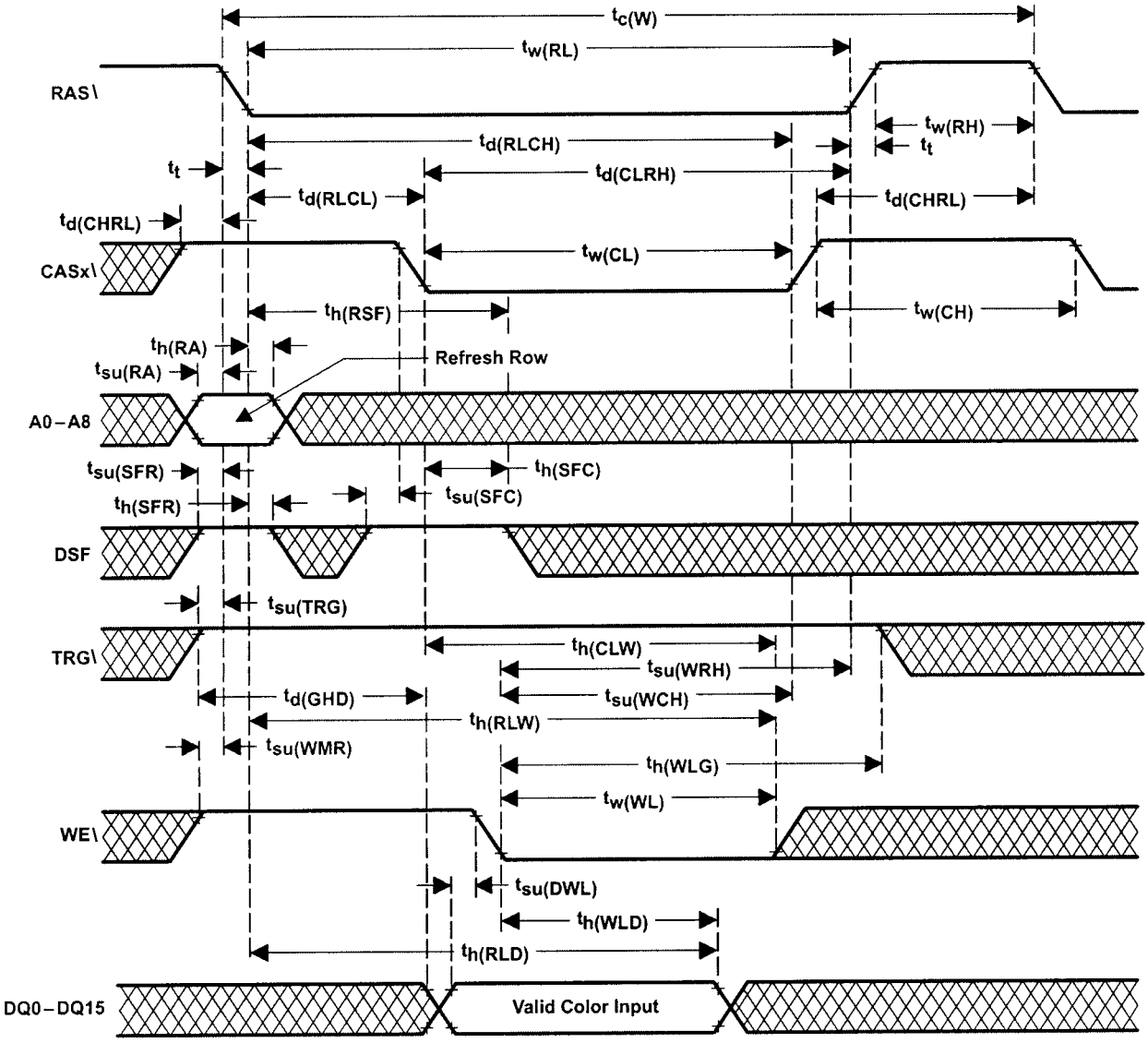


FIGURE 37: BLOCK-WRITE-CYCLE TIMING (EARLY WRITE)

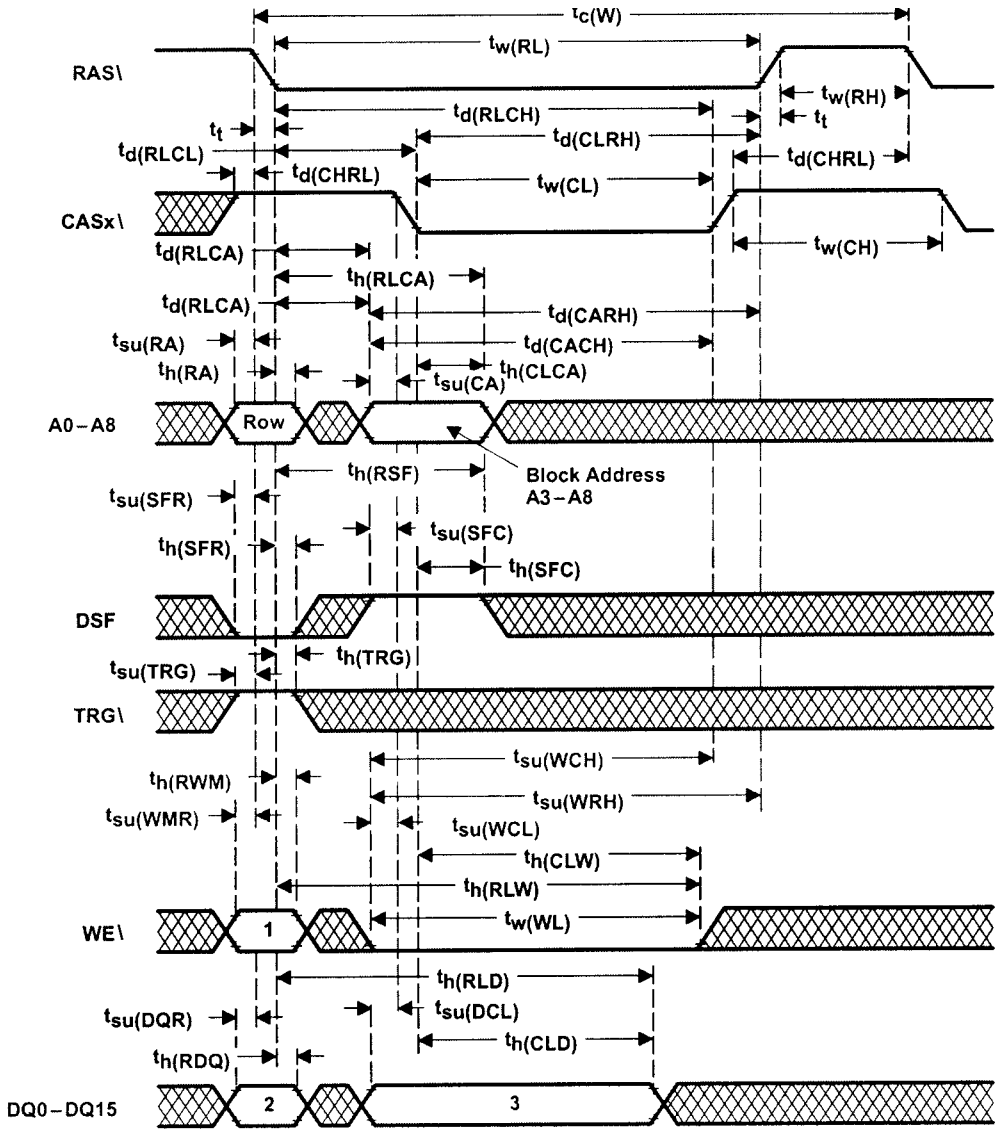


TABLE 12: BLOCK-WRITE-CYCLE STATE TABLE

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't Care	Valid Data
Block-write operation with nonpersistent write-per-bit	L	Write Mask	Valid Data
Block-write operation with persistent write-per-bit	L	Don't Care	Valid Data

Write-mask data 0: I/O write disable
1: I/O write enable DQ
Column-mask data DQi – DQi + 7 0: column-write disable
(i = 0,8) 1: column-write enable

COLUMN MASK DATA

	DQ0-15	COLUMN MASK DATA	
Lower Byte	DQ0	Column 0 (A0 = 0, A1 = 0, A2 = 0)	Low: Mask High: No Mask
	DQ1	Column 1 (A0 = 1, A1 = 0, A2 = 0)	
	DQ2	Column 2 (A0 = 0, A1 = 1, A2 = 0)	
	DQ3	Column 3 (A0 = 1, A1 = 1, A2 = 0)	
	DQ4	Column 4 (A0 = 0, A1 = 0, A2 = 1)	
	DQ5	Column 5 (A0 = 1, A1 = 0, A2 = 1)	
	DQ6	Column 6 (A0 = 0, A1 = 1, A2 = 1)	
	DQ7	Column 7 (A0 = 1, A1 = 1, A2 = 1)	
Upper Byte	DQ8	Column 0 (A0 = 0, A1 = 0, A2 = 0)	Low: Mask High: No Mask
	DQ9	Column 1 (A0 = 1, A1 = 0, A2 = 0)	
	DQ10	Column 2 (A0 = 0, A1 = 1, A2 = 0)	
	DQ11	Column 3 (A0 = 1, A1 = 1, A2 = 0)	
	DQ12	Column 4 (A0 = 0, A1 = 0, A2 = 1)	
	DQ13	Column 5 (A0 = 1, A1 = 0, A2 = 1)	
	DQ14	Column 6 (A0 = 0, A1 = 1, A2 = 1)	
	DQ15	Column 7 (A0 = 1, A1 = 1, A2 = 1)	

FIGURE 38: BLOCK-WRITE-CYCLE TIMING (LATE WRITE)

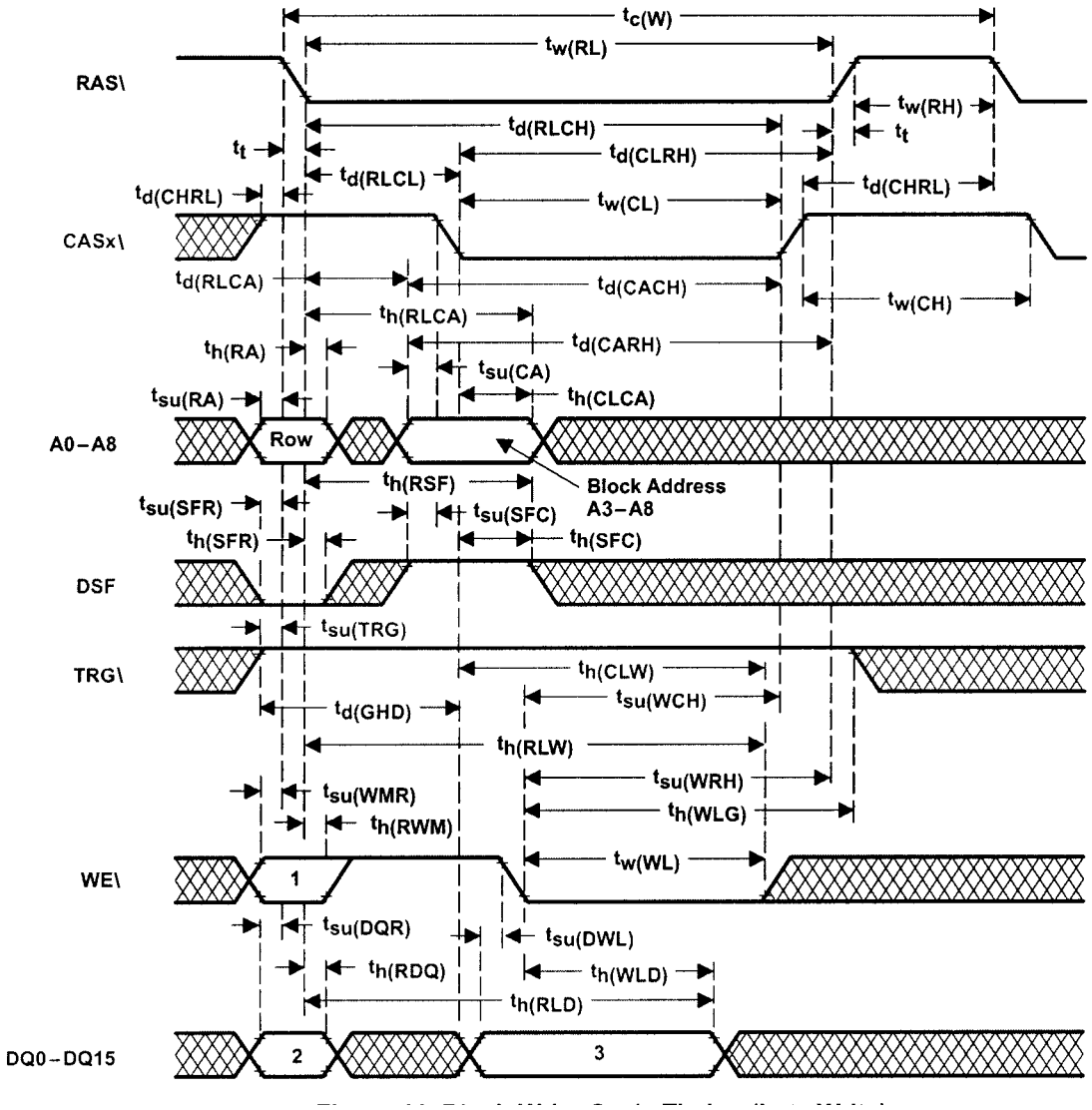


TABLE 13: BLOCK-WRITE-CYCLE STATE TABLE

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't Care	Valid Data
Block-write operation with nonpersistent write-per-bit	L	Write Mask	Valid Data
Block-write operation with persistent write-per-bit	L	Don't Care	Valid Data

Write-mask data 0: I/O write disable
1: I/O write enable DQ
Column-mask data DQi – DQi + 7 0: column-write disable
(i = 0,8) 1: column-write enable

COLUMN MASK DATA

	DQ0-15	COLUMN MASK DATA	
Lower Byte	DQ0	Column 0 (A0 = 0, A1 = 0, A2 = 0)	Low: Mask High: No Mask
	DQ1	Column 1 (A0 = 1, A1 = 0, A2 = 0)	
	DQ2	Column 2 (A0 = 0, A1 = 1, A2 = 0)	
	DQ3	Column 3 (A0 = 1, A1 = 1, A2 = 0)	
	DQ4	Column 4 (A0 = 0, A1 = 0, A2 = 1)	
	DQ5	Column 5 (A0 = 1, A1 = 0, A2 = 1)	
	DQ6	Column 6 (A0 = 0, A1 = 1, A2 = 1)	
	DQ7	Column 7 (A0 = 1, A1 = 1, A2 = 1)	
Upper Byte	DQ8	Column 0 (A0 = 0, A1 = 0, A2 = 0)	Low: Mask High: No Mask
	DQ9	Column 1 (A0 = 1, A1 = 0, A2 = 0)	
	DQ10	Column 2 (A0 = 0, A1 = 1, A2 = 0)	
	DQ11	Column 3 (A0 = 1, A1 = 1, A2 = 0)	
	DQ12	Column 4 (A0 = 0, A1 = 0, A2 = 1)	
	DQ13	Column 5 (A0 = 1, A1 = 0, A2 = 1)	
	DQ14	Column 6 (A0 = 0, A1 = 1, A2 = 1)	
	DQ15	Column 7 (A0 = 1, A1 = 1, A2 = 1)	

FIGURE 39: ENHANCED-PAGE-MODE BLOCK-WRITE-CYCLE TIMING

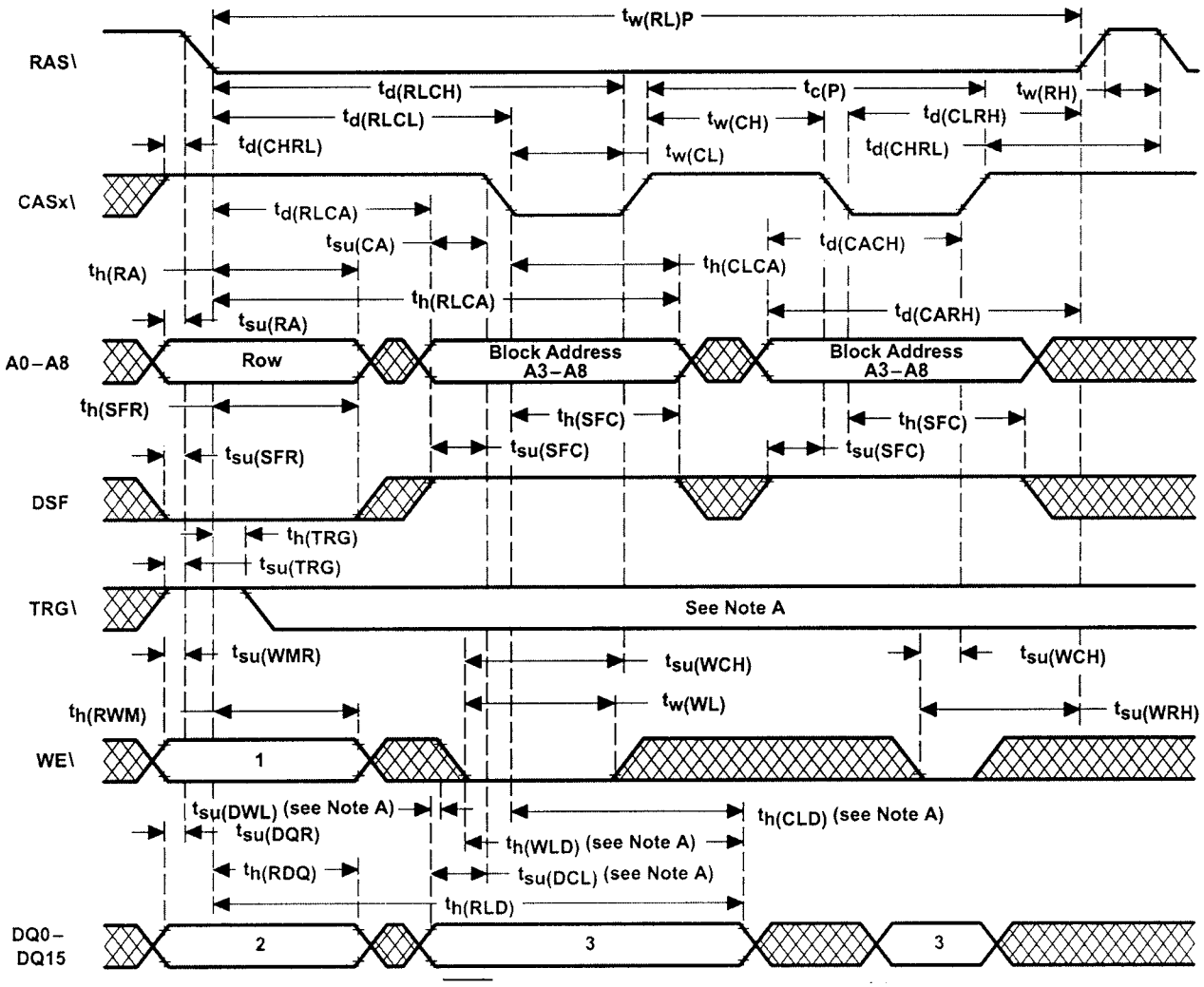


TABLE 14: ENHANCED-PAGE-MODE BLOCK-WRITE-CYCLE STATE TABLE

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't Care	Valid Data
Block-write operation with nonpersistent write-per-bit	L	Write Mask	Valid Data
Block-write operation with persistent write-per-bit	L	Don't Care	Valid Data

Write-mask data 0: I/O write disable
1: I/O write enable DQ
Column-mask data DQi – DQi + 7 0: column-write disable
(i = 0,8) 1: column-write enable

COLUMN MASK DATA

	DQ0-15	COLUMN MASK DATA	
Lower Byte	DQ0	Column 0 (A0 = 0, A1 = 0, A2 = 0)	Low: Mask High: No Mask
	DQ1	Column 1 (A0 = 1, A1 = 0, A2 = 0)	
	DQ2	Column 2 (A0 = 0, A1 = 1, A2 = 0)	
	DQ3	Column 3 (A0 = 1, A1 = 1, A2 = 0)	
	DQ4	Column 4 (A0 = 0, A1 = 0, A2 = 1)	
	DQ5	Column 5 (A0 = 1, A1 = 0, A2 = 1)	
	DQ6	Column 6 (A0 = 0, A1 = 1, A2 = 1)	
	DQ7	Column 7 (A0 = 1, A1 = 1, A2 = 1)	
Upper Byte	DQ8	Column 0 (A0 = 0, A1 = 0, A2 = 0)	Low: Mask High: No Mask
	DQ9	Column 1 (A0 = 1, A1 = 0, A2 = 0)	
	DQ10	Column 2 (A0 = 0, A1 = 1, A2 = 0)	
	DQ11	Column 3 (A0 = 1, A1 = 1, A2 = 0)	
	DQ12	Column 4 (A0 = 0, A1 = 0, A2 = 1)	
	DQ13	Column 5 (A0 = 1, A1 = 0, A2 = 1)	
	DQ14	Column 6 (A0 = 0, A1 = 1, A2 = 1)	
	DQ15	Column 7 (A0 = 1, A1 = 1, A2 = 1)	

FIGURE 40: RAS\-ONLY REFRESH-CYCLE TIMING

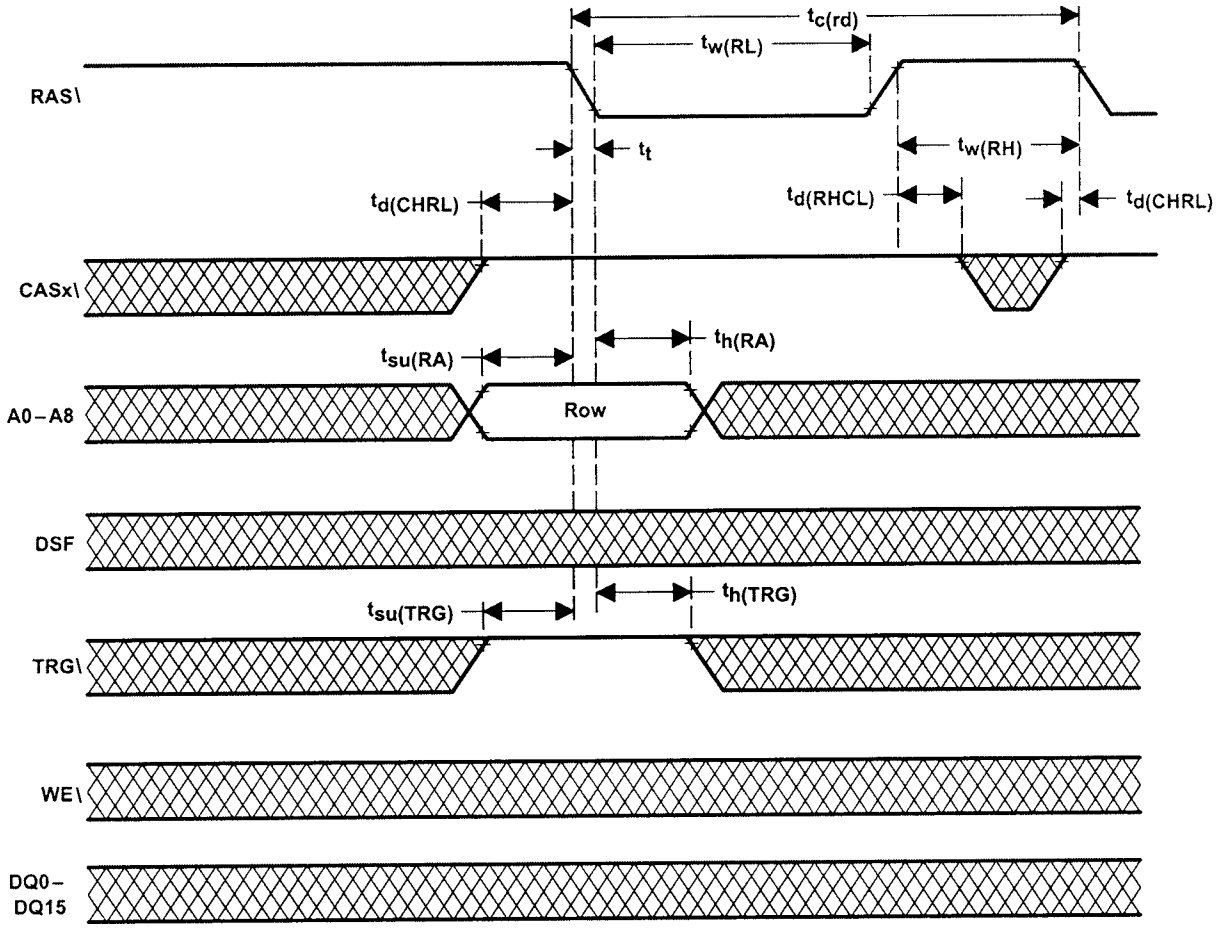


FIGURE 41: CBR-REFRESH-CYCLE TIMING

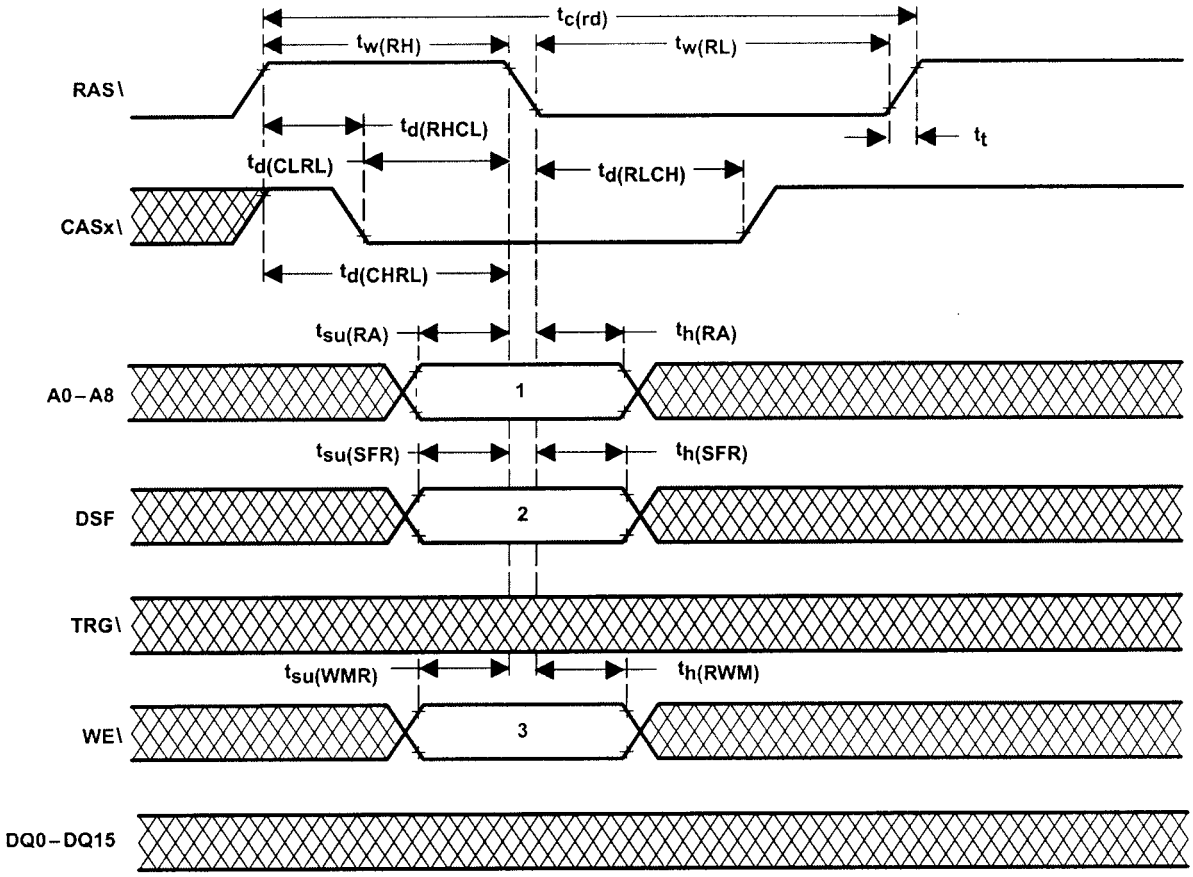


TABLE 15: CBR-CYCLE STATE TABLE

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't Care	L	H
CBR refresh with no reset	Don't Care	H	H
CBR refresh with stop-point set and no reset	Stop Address	H	L

FIGURE 42: HIDDEN-REFRESH-CYCLE TIMING

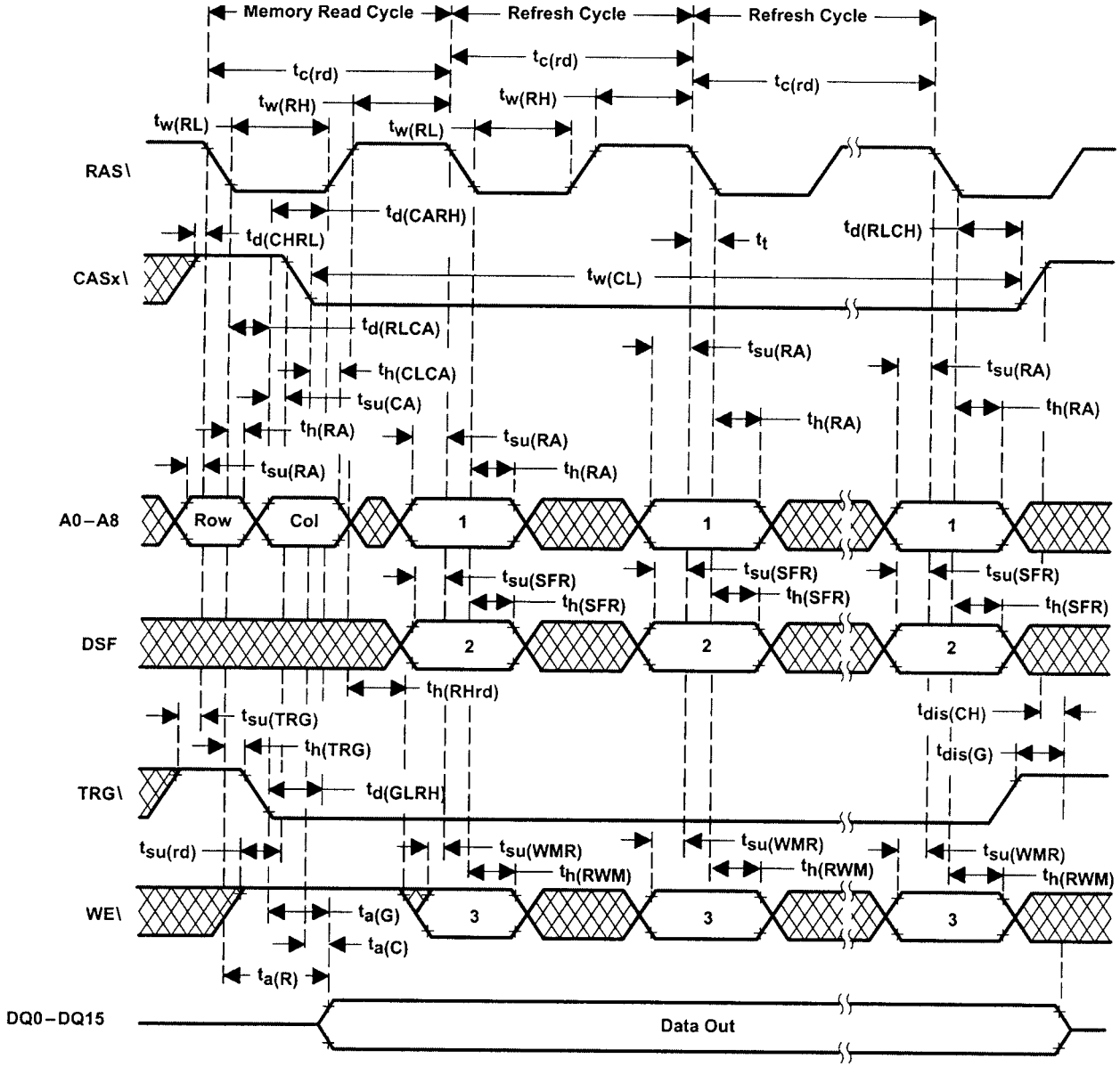
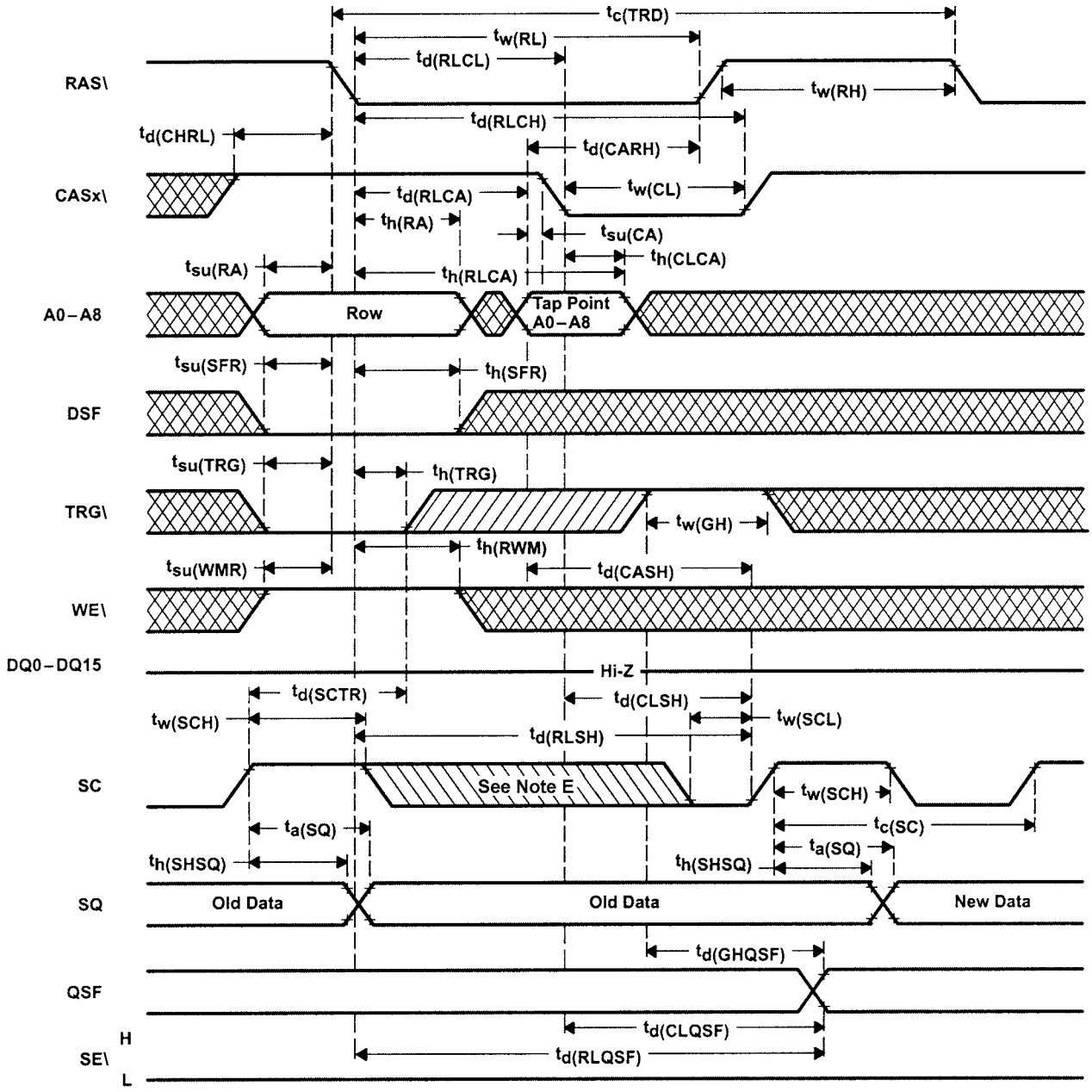


TABLE 16: HIDDEN-REFRESH-CYCLE STATE TABLE

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't Care	L	H
CBR refresh with no reset	Don't Care	H	H
CBR refresh with stop-point set and no reset	Stop Address	H	L

FIGURE 43: FULL-REGISTER TRANSFER-READ TIMING, EARLY-LOAD OPERATIONS



NOTES:

A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written to from the 512 corresponding columns of the selected row.

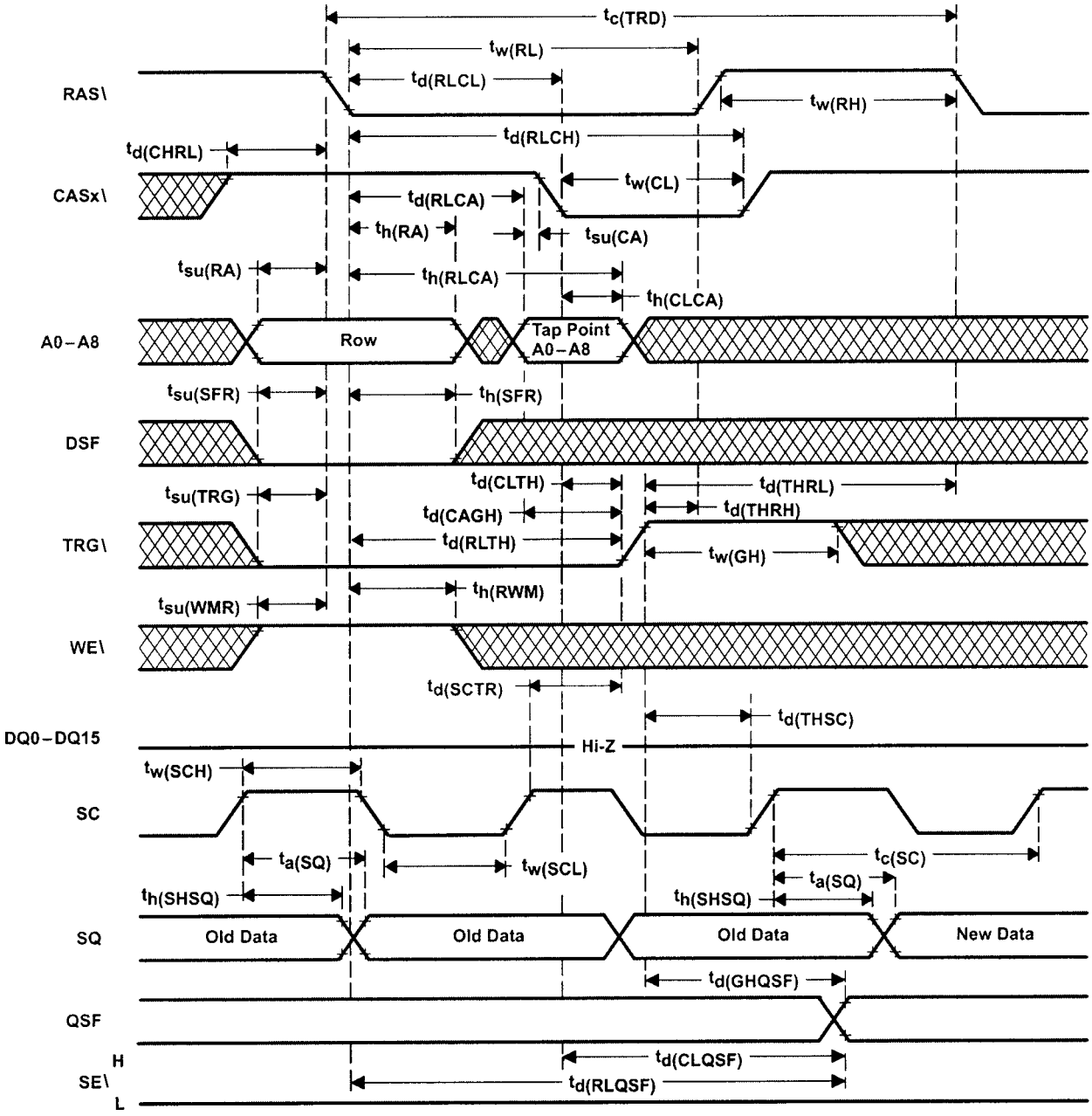
B. Once data is transferred into the data registers, the SAM is in the serial-read mode, that is, the SQ is enabled, allowing data to be shifted out of the registers. Also, the first bit to read from the data register after TRG\ has gone high must be activated by a positive transition of SC.

C. A0 – A8.

D. Early-load operation is defined as $t_{h(TRG)}$ MIN < $t_{h(TRG)}$ < $t_{d(RLTH)}$ MIN.

E. There must be no rising transitions.

FIGURE 44: FULL-REGISTER TRANSFER READ-TIMING, REAL-TIME LOAD OPERATION/LATE-LOAD OPERATION



NOTES:

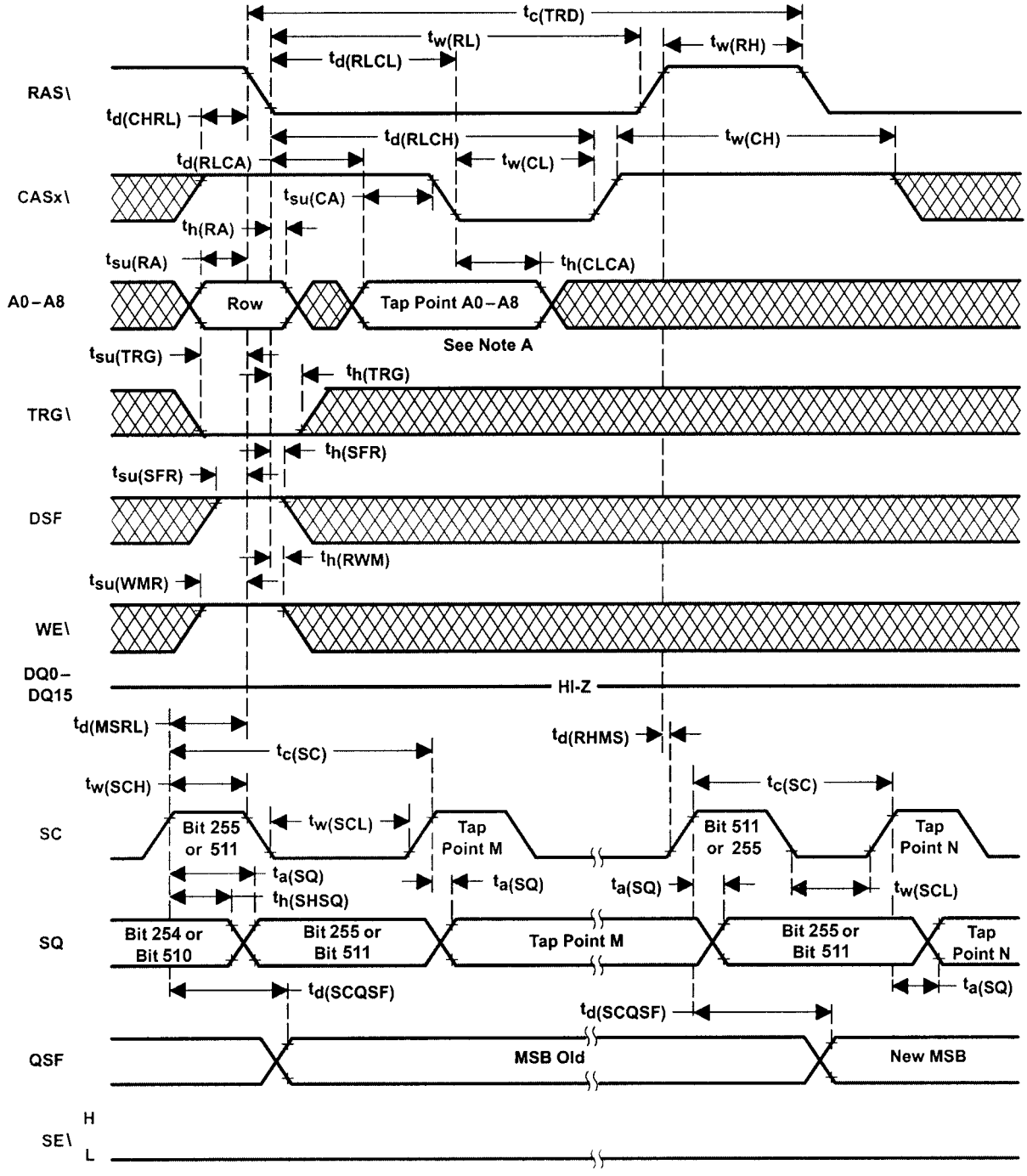
A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written to from the 512 corresponding columns of the selected row.

B. Once data is transferred into the data registers, the SAM is in the serial-read mode, that is, the SQ is enabled, allowing data to be shifted out of the registers. Also, the first bit to read from the data register after TRG\ has gone high must be activated by a positive transition of SC.

C. A0–A8.

D. Late load operation is defined as $t_{d(THRH)} < 0$ ns.

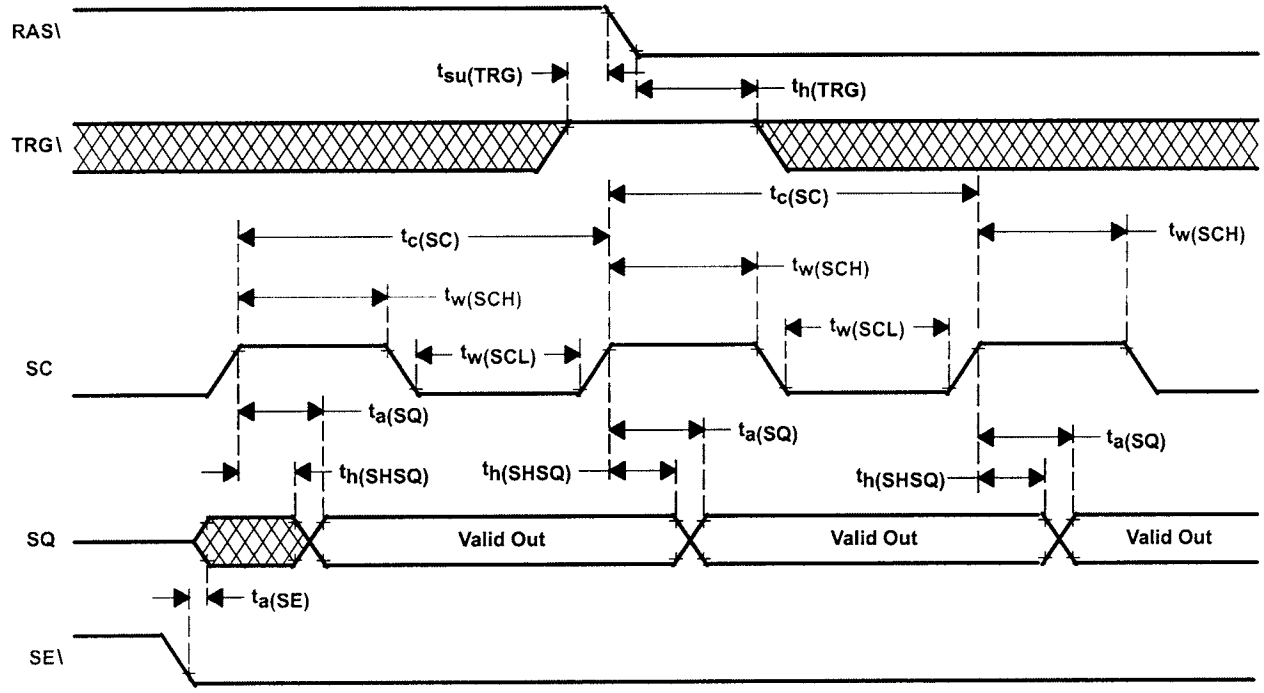
FIGURE 45: SPLIT-REGISTER-TRANSFER-READ TIMING



NOTES:

A. A0–A7: tap point of the given half; A8: identifies the DRAM row half

FIGURE 46: SERIAL-READ-CYCLE TIMING (SE\ = V_{IL})



NOTES:

A. While the data is being read through the serial-data register, TRG\ is a don't care; however, TRG\ must be held high when RAS\ goes low. This is to avoid the initiation of a register-data transfer operation.

B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer-read cycle.

FIGURE 47: SERIAL-WRITE-CYCLE TIMING

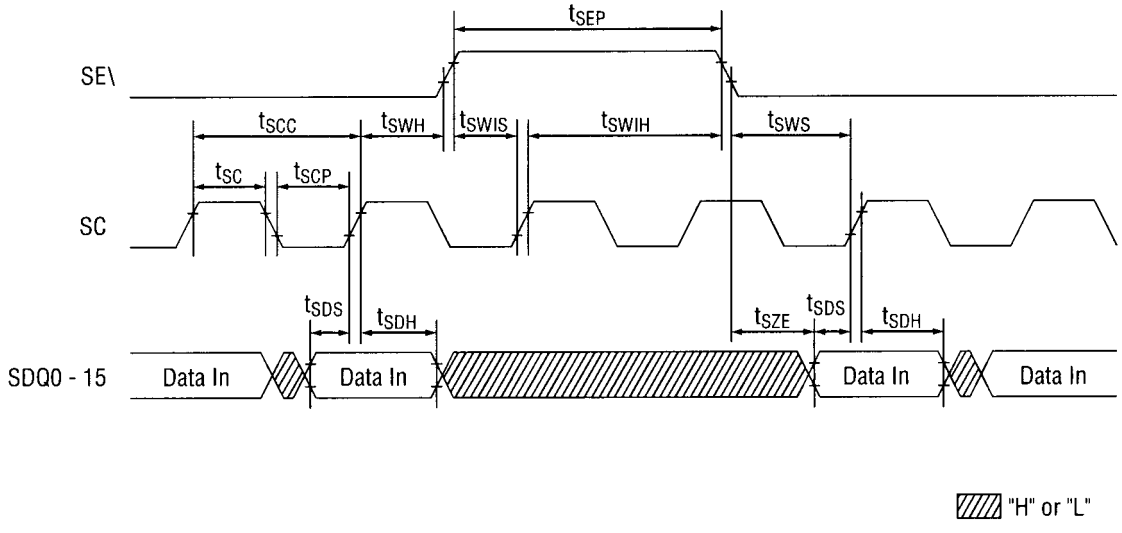
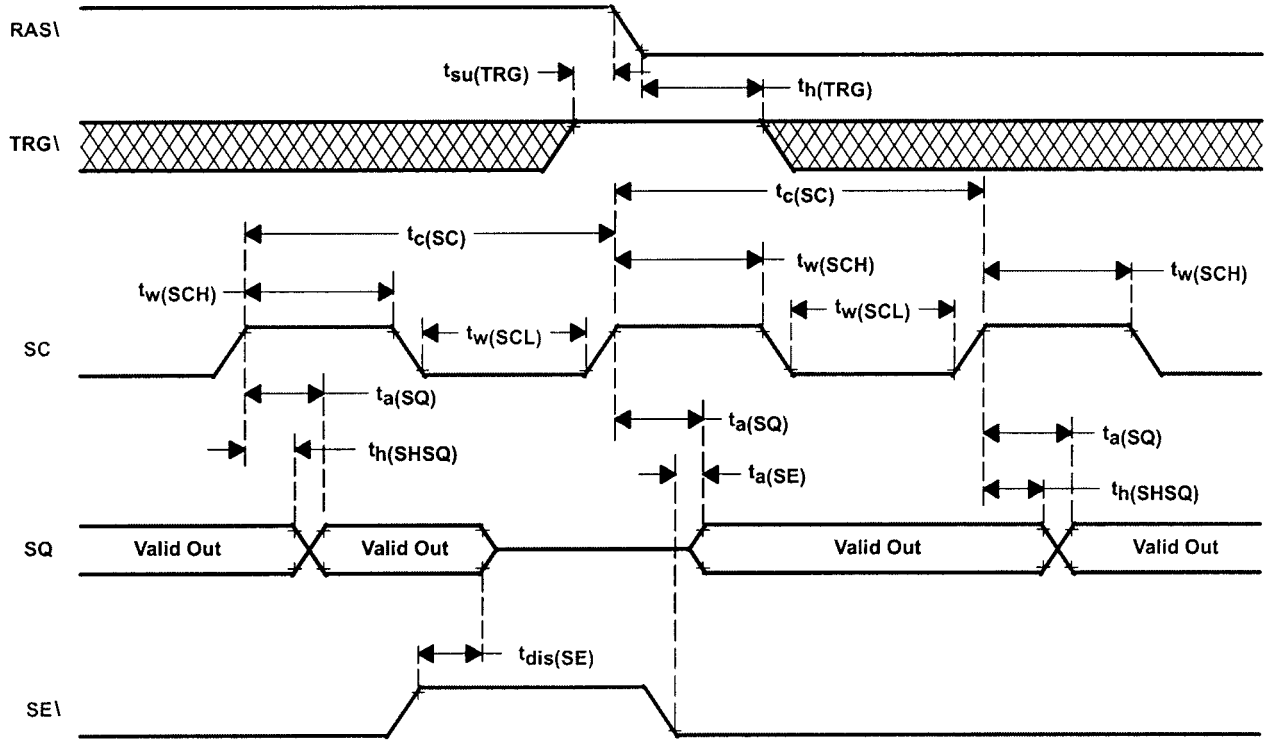


FIGURE 48: SERIAL-READ TIMING (SE\-CONTROLLED READ)

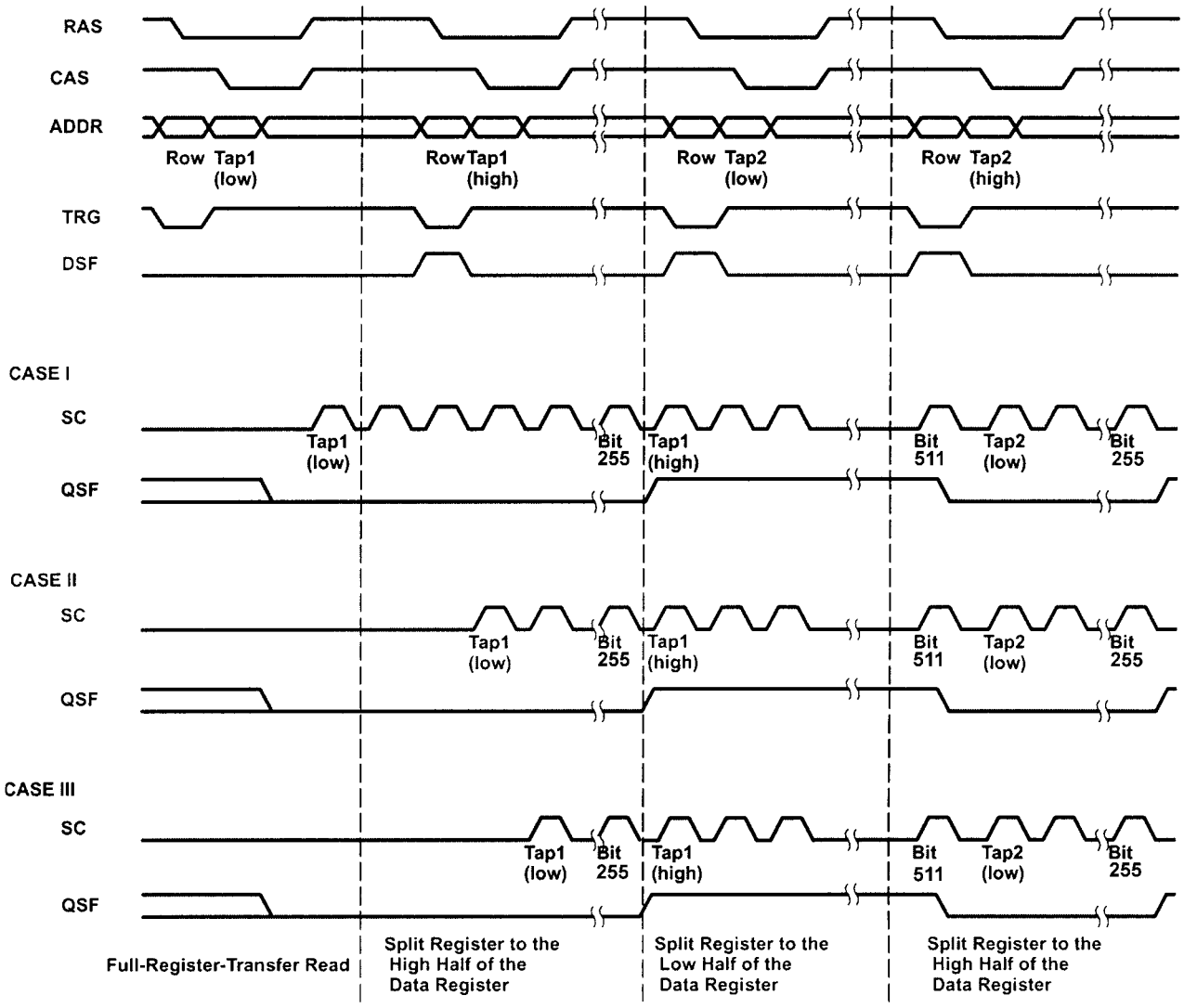


NOTES:

A. While the data is being read through the serial-data register, TRG\ is a don't care; however, TRG\ must be held high when RAS\ goes low. This is to avoid the initiation of a register-data transfer operation.

B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer-read cycle.

FIGURE 49: SPLIT-REGISTER OPERATING SEQUENCE

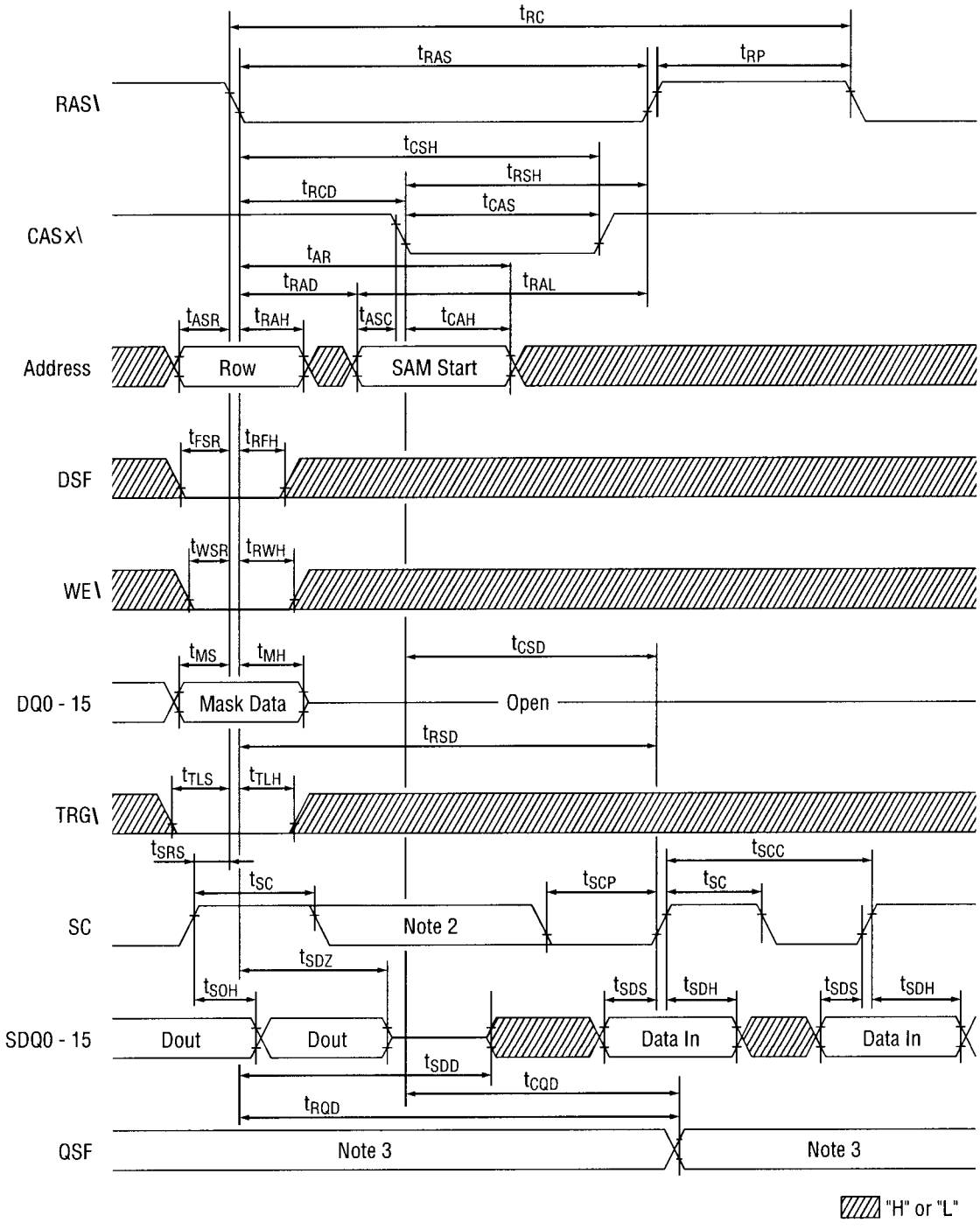


NOTES:

A. To achieve proper split-register operation, a full-register-transfer read must be performed before the first split-register-transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can begin either after the full-register-transfer-read cycle (CASE I), during the first split-register-transfer cycle (CASE II), or even after the first split-register-transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register transfer-read cycle and the first split-register cycle.

B. A split-register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 255 or 511) and the falling edge of RAS\ of the split-register-transfer cycle into the inactive half. After the $t_{d(MSRL)}$ requirement is met, the split-register transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of RAS\ of the split-register-transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 255 or 511).

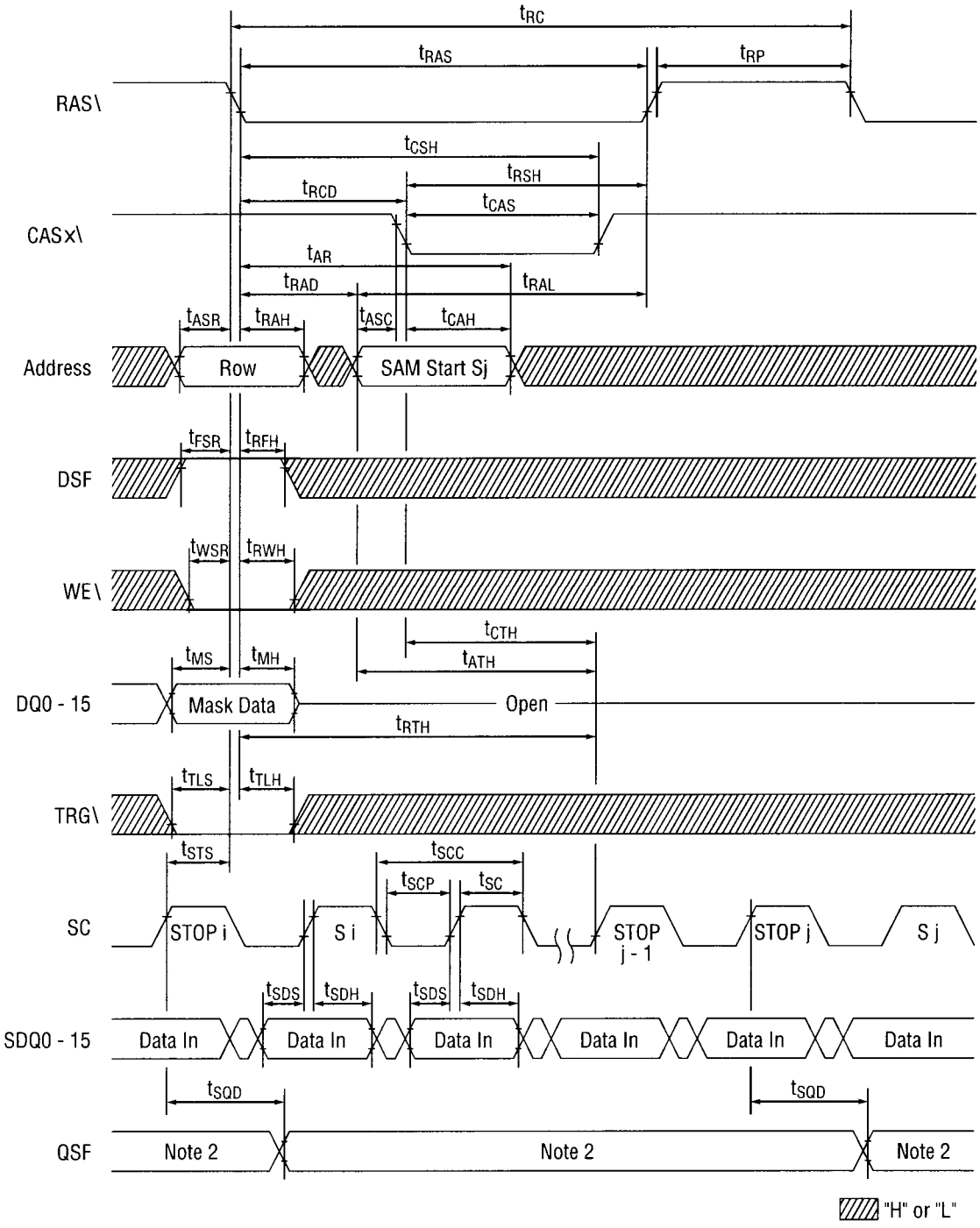
FIGURE 50: MASKED WRITE TRANSFER



NOTES:

1. SE\ = "L"
2. There must be no rising transitions.
3. QSF = "L" - Lower SAM (0-255) is active.
   QSF = "H" - Upper SAM (256-511) is active.

FIGURE 51: MASKED SPLIT WRITE TRANSFER

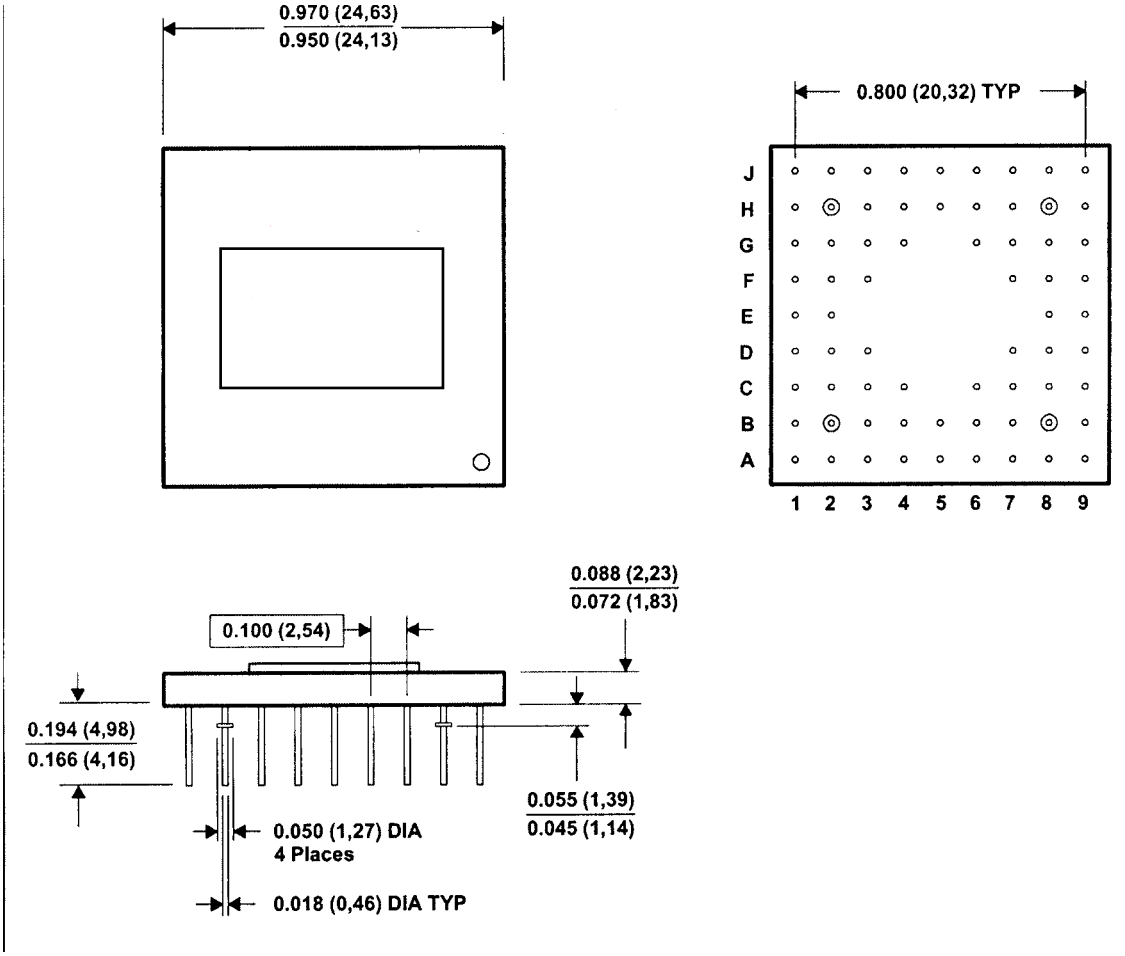


NOTES:

1. SE\ = "L"
2. QSF = "L" - Lower SAM (0-255) is active.
   QSF = "H" - Upper SAM (256-511) is active.
3. Si is the SAM start address in before SWT.
4. STOP i and STOP j are programmable stop addresses.

MECHANICAL DEFINITIONS*

Package Designator GB
SMD 5962-94549, Case Outline X

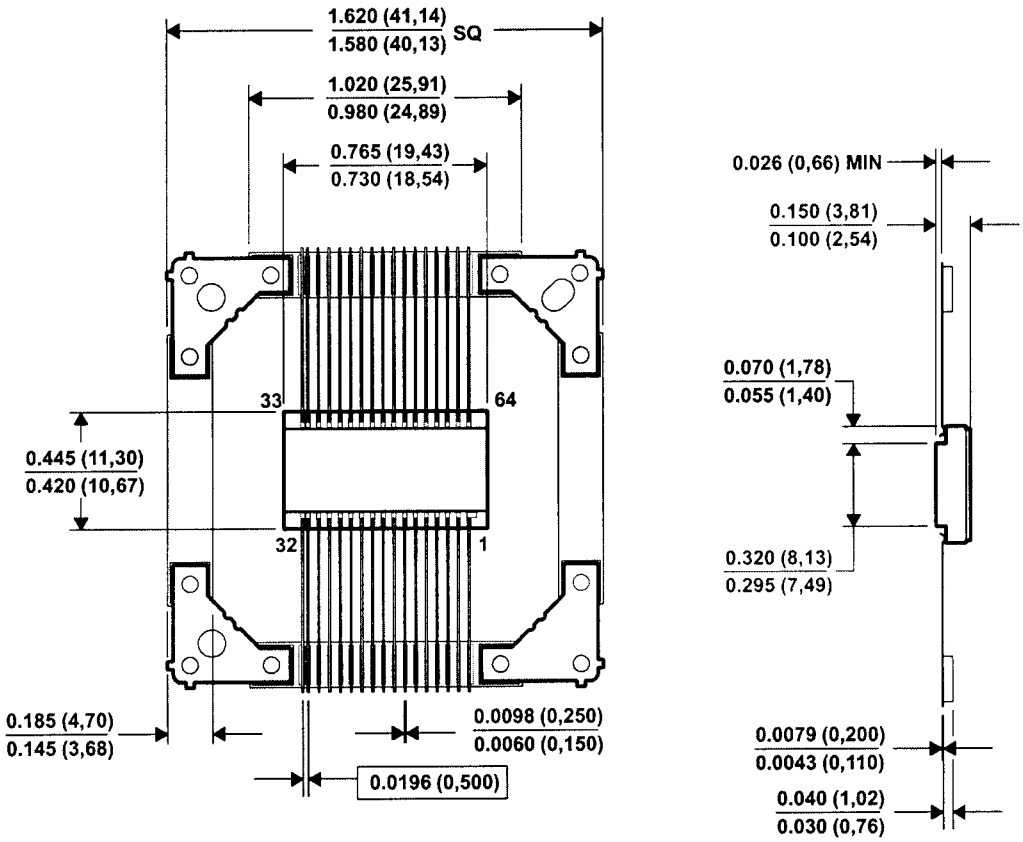


NOTES:

1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Index mark may appear on top or bottom depending on package vendor.
4. Pins are located within 0.005 (0,13) radius of true position relative to each other at maximum material condition and within 0.015 (0,38) radius relative to the center of the ceramic.
5. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
6. The pins can be gold plated or solder dipped.
7. Falls within MIL-STD-1835 CMGA1-PN and CMGA13-PN and JEDEC MO-067AA and MO-066AA, respectively

MECHANICAL DEFINITIONS*

Package Designator HKC
SMD 5962-94549, Case Outline Y



NOTES:

1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a metal lid.
4. The terminals are gold plated.
5. All leads not shown for clarity purposes.

ORDERING INFORMATION

EXAMPLE: SM55161A-75GBI

Prefix*	Part Number	Speed	Package	Temp
SM	55161A	-70	GB	M or I
SMX	55161A	-70	GB	M or I
SM	55161A	-75	GB	M or I
SMX	55161A	-75	GB	M or I
SM	55161A	-80	GB	M or I
SMX	55161A	-80	GB	M or I

EXAMPLE: SM55161A-80HKCM

Prefix*	Part Number	Speed	Package	Temp
SM	55161A	-70	HKC	M or I
SMX	55161A	-70	HKC	M or I
SM	55161A	-75	HKC	M or I
SMX	55161A	-75	HKC	M or I
SM	55161A	-80	HKC	M or I
SMX	55161A	-80	HKC	M or I

SM Prefix: Standard Military Processing using MIL-STD-883C flow & methods but non-complaint to para 1.2.1

SMX Prefix: strictly commercial flow samples

I suffix: -40C to +85C
M suffix: -55C to 125C

ASI TO DSCC PART NUMBER CROSS REFERENCE

Package Designator GB

ASI Part #	SMD Part #
TO BE COMPLETED WHEN SMD LISTING IS RELEASED	

Package Designator HKC

ASI Part #	SMD Part #
TO BE COMPLETED WHEN SMD LISTING IS RELEASED	