

SN54ABTE16245, SN74ABTE16245 16-BIT INCIDENT-WAVE SWITCHING BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS226J – JULY 1993 – REVISED DECEMBER 2001

- Members of the Texas Instruments Widebus™ Family
- Support the VME64 ETL Specification
- Reduced, TTL-Compatible, Input Threshold Range
- High-Drive Outputs ($I_{OH} = -60$ mA, $I_{OL} = 90$ mA) Support 25- Ω Incident-Wave Switching
- V_{CCBIAS} Pin Minimizes Signal Distortion During Live Insertion
- Internal Pullup Resistor on \overline{OE} Keeps Outputs in High-Impedance State During Power Up or Power Down
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Equivalent 25- Ω Series Damping Resistor on B Port
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors

description

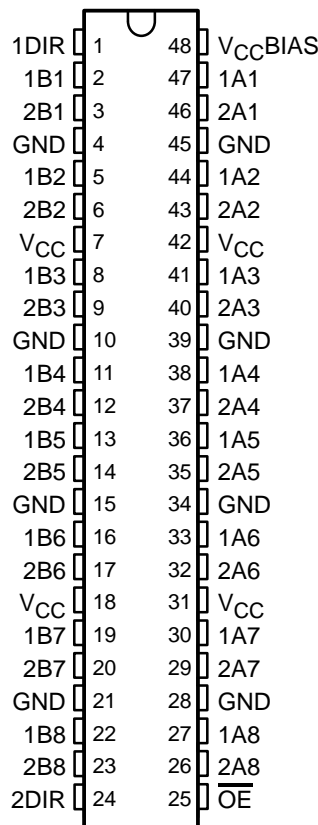
The 'ABTE16245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated. When \overline{OE} is low, the device is active.

The B port has an equivalent 25- Ω series output resistor to reduce ringing. Active bus-hold inputs also are on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CCBIAS} , which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

SN54ABTE16245 . . . WD PACKAGE
SN74ABTE16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



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Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

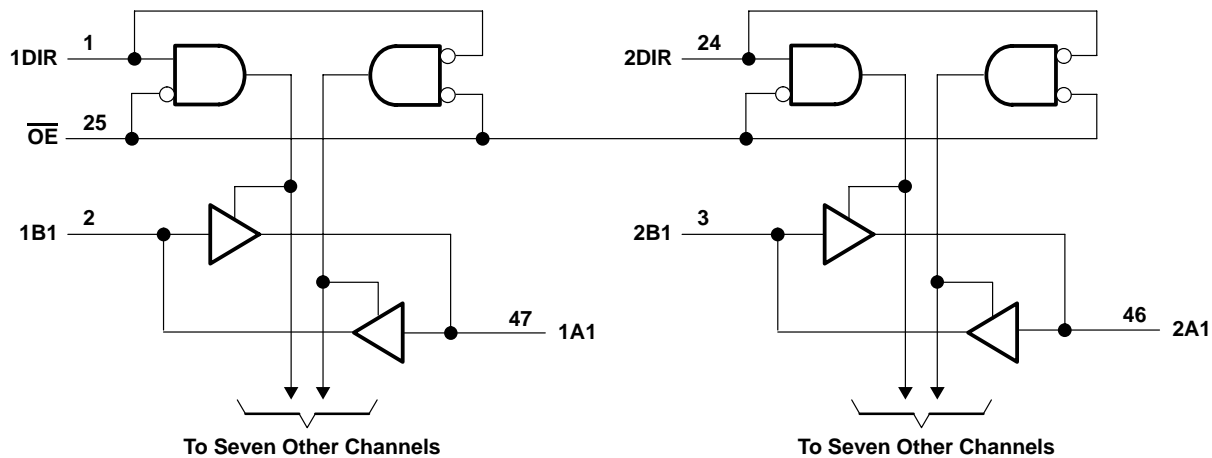
T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74ABTE16245DL	ABTE16245
		Tape and reel	SN74ABTE16245DLR	
–55°C to 125°C	CFP – WD	Tape and reel	SN74ABTE16245DGGR	ABTE16245
		Tube	SNJ54ABTE16245WD	SNJ54ABTE16245WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	A data to B bus
L	H	B data to A bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} and V _{CC} BIAS	–0.5 V to 7 V
Input voltage range, V _I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V _O	–0.5 V to 5.5 V
Current into any output in the low state, I _O	128 mA
Input clamp current, I _{IK} (V _I < 0)	–18 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DL package	63°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

			SN54ABTE16245			SN74ABTE16245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} , V_{CCBIAS}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	\overline{OE}	2			2			V
		Except \overline{OE}	1.6			1.6			
V_{IL}	Low-level input voltage	\overline{OE}			0.8			0.8	V
		Except \overline{OE}			1.4			1.4	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	B bus			-12			-12	mA
		A bus			-24			-60	
I_{OL}	Low-level output current	B bus			12			12	mA
		A bus			64			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
T_A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ABTE16245			SN74ABTE16245			UNIT		
		MIN	TYP†	MAX	MIN	TYP†	MAX			
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V		
V _{OH}	B port	V _{CC} = 5.5 V, I _{OH} = -100 μA		V _{CC} -0.2			V _{CC} -0.2		V	
		V _{CC} = 4.5 V	I _{OH} = -1 mA	2.4		2.4				
	I _{OH} = -12 mA		2		2					
	A port	V _{CC} = 5.5 V, I _{OH} = -1 mA				4.5		4.5		
		V _{CC} = 4.5 V	I _{OH} = -32 mA	2.4		2.4				
			I _{OH} = -64 mA			2				
V _{OL}	B port	V _{CC} = 4.5 V	I _{OL} = 1 mA			0.4		0.4	V	
			I _{OL} = 12 mA					0.8		
	A port	V _{CC} = 4.5 V	I _{OL} = 64 mA			0.55		0.55		
			I _{OL} = 90 mA					0.9		
I _I (hold)	B port	V _{CC} = 4.5 V	V _I = 0.8 V	100		100		μA		
			V _I = 2 V	-100		-100				
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		μA	
	A or B ports				±20		±20			
I _{OZH} ‡	A port	V _{CC} = 5.5 V, V _O = 2.7 V			10		10		μA	
I _{OZL} ‡	A port	V _{CC} = 5.5 V, V _O = 0.5 V			-10		-10		μA	
I _O	A port	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-120	-180	-50	-180	mA		
	B port		-25	-52	-90	-25	-90			
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V, V _{CC} BIAS = 0		±100		±100		μA		
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		28	36	28	36	mA	
			Outputs low		38	48	38	48		
			Outputs disabled		20	32	20	32		
I _{CCD}	A or B ports	V _{CC} = 5 V, C _L = 50 pF	\overline{OE} high		0.02		0.02		mA/ MHz	
			\overline{OE} low		0.33		0.33			
C _i	Control inputs	V _I = 2.5 V or 0.5 V		10		2.5	4	pF		
C _{io}	I/O ports	V _O = 2.5 V or 0.5 V		13		4.5	8	pF		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.



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live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54ABTE16245			SN74ABTE16245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I _{CC} (V _{CC} BIAS)		V _{CC} = 0 to 4.5 V, V _{CC} BIAS = 4.5 V to 5.5 V, I _O (DC) = 0		250	700		250	700	μA	
		V _{CC} = 4.5 V to 5.5 V‡, V _{CC} BIAS = 4.5 V to 5.5 V, I _O (DC) = 0		20			20			
V _O	A port	V _{CC} = 0	V _{CC} BIAS = 4.5 V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	V
			V _{CC} BIAS = 4.75 V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	
I _O	A port	V _{CC} = 0, V _{CC} BIAS = 4.5 V		V _O = 0	-20		-100		μA	
				V _O = 3 V	20		100			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ V_{CC} - 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABTE16245		SN74ABTE16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	B	1.5	3.3	4.2	1.5	5.4	1.5	5.2	ns
t _{PHL}			1.5	3.8	4.6	1.5	5.4	1.5	5.2	
t _{PLH}	B	A	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t _{PHL}			1.5	3.1	4	1.5	4.7	1.5	4.5	
t _{PZH}	OE	A	2	3.9	5.3	2	6.4	2	6.2	ns
t _{PZL}			2	4.4	5.9	2	7	2	6.8	
t _{PZH}	OE	B	2	4.5	6	2	7.3	2	7.1	ns
t _{PZL}			2	5	6.4	2	7.5	2	7.3	
t _{PHZ}	OE	A	2	4.9	5.9	2	7	2	6.7	ns
t _{PLZ}			2	3.7	4.6	2	5.4	2	5.1	
t _{PHZ}	OE	B	2	5.2	6.2	2	7.2	2	7	ns
t _{PLZ}			2	4	5	2	5.8	2	5.5	



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extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABTE16245		SN74ABTE16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	B	A	$R_X = 13 \Omega$	1.5	3.2	4	1.5	5	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.8	1.5	5.6	
t_{PLH}	B	A	$R_X = 26 \Omega$	1.5	3.1	4	1.5	4.8	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	5.2	1.5	4.9	
t_{PLH}	B	A	$R_X = 56 \Omega$	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	5.1	1.5	4.7	
$t_{sk(p)}$	B	A	$R_X = \text{Open}$		0.1	0.6		2		2	ns
	A	B	$R_X = \text{Open}$		0.4	0.8		2		2	
	B	A	$R_X = 26 \Omega$		0.3	0.8		2		2	
$t_{sk(o)}$	B	A	$R_X = \text{Open}$		0.3	0.7		1.3		1.3	ns
	A	B	$R_X = \text{Open}$		0.7	1.1		1.3		1.3	
	B	A	$R_X = 26 \Omega$		0.5	1		1.3		1.3	
t_t^\dagger	B	A	$R_X = 26 \Omega$	0.5	0.8	1.5	0.5	1.5	0.5	1.5	ns
t_t^\ddagger	A	B	$R_X = \text{Open}$	3.5	5.5	7.3	3.5	8.1	3.5	7.9	ns

$^\dagger t_t$ is measured between 1 V and 2 V of the output waveform.

$^\ddagger t_t$ is measured between 10% and 90% of the output waveform.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (see Figures 1 and 2)

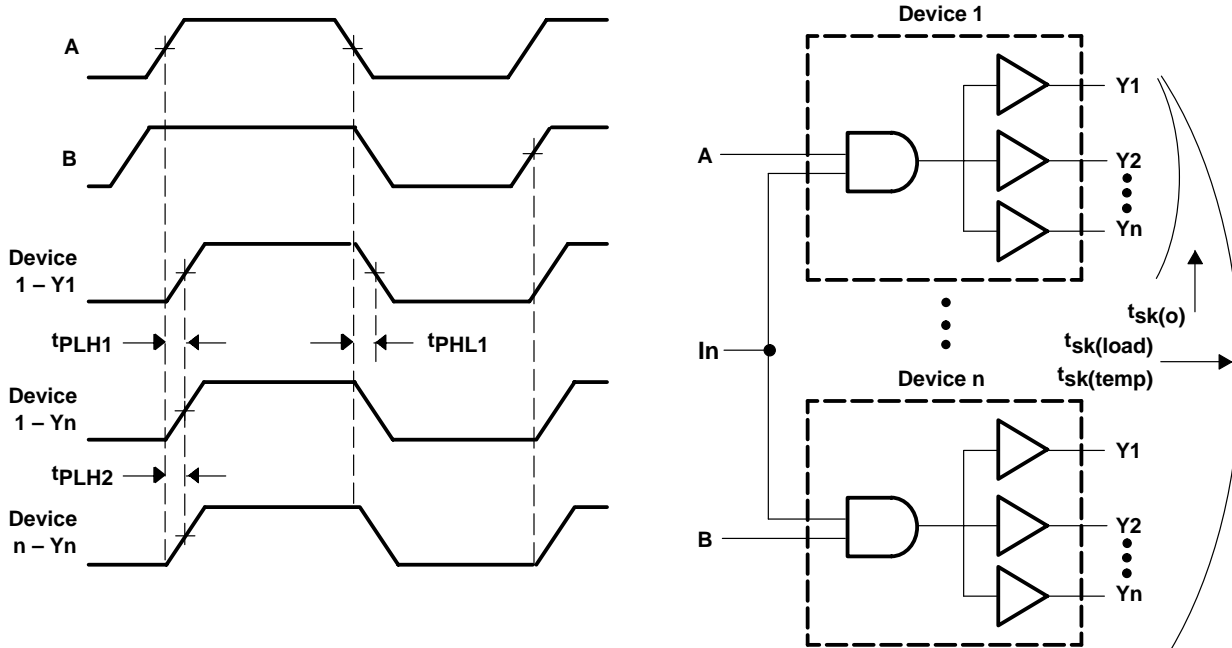
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	SN54ABTE16245		SN74ABTE16245		UNIT
					MIN	MAX	MIN	MAX	
$t_{sk(temp)}$	A	B	$V_{CC} = \text{constant},$ $\Delta T_A = 20^\circ$ C			3		2.5	ns
	B	A		$R_X = 56 \Omega$		4.5		4	
$t_{sk(load)}$	B	B	$V_{CC} = \text{constant},$ Temperature = constant	$R_X = 13, 26,$ or 56Ω		4.5		4	ns



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PARAMETER MEASUREMENT INFORMATION



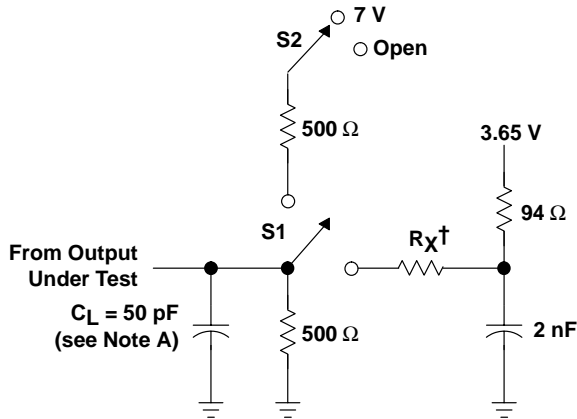
- NOTES:
- A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation-delay times t_{PLH1} and t_{PHL1} on the same terminal at identical operating conditions.
 - B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of any two outputs of the same device switching in the same direction (e.g., $|t_{PLH1} - t_{PLH2}|$).
 - C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of $V_{CC} \pm 1\%$ and with package temperature differences of 20°C .
 - D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at $13\ \Omega$ for one unit and $56\ \Omega$ for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

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PARAMETER MEASUREMENT INFORMATION

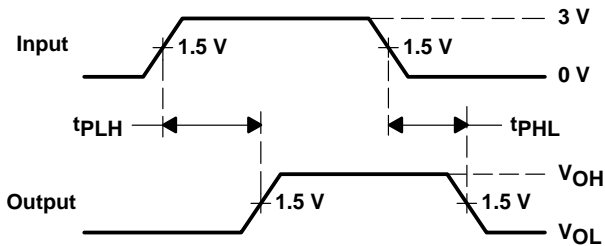


† $R_X = 13, 26, \text{ or } 56 \Omega$

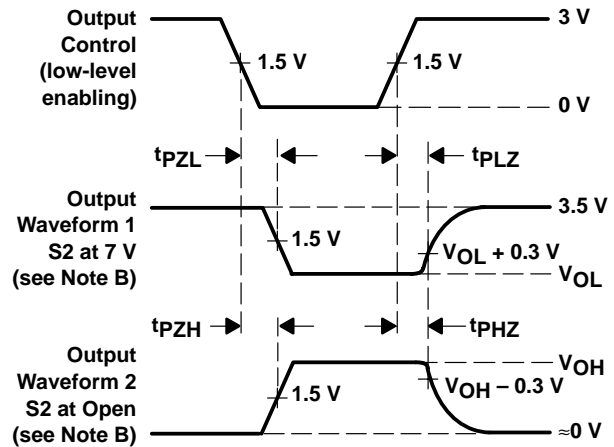
SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (A and B port)	Up	Open
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH}	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open

LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_t is measured between 1 V and 2 V of the output waveform.
 - t_t is measured between 10% and 90% of the output waveform.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9677501QXA	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type
74ABTE16245DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABTE16245DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABTE16245DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTE16245DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTE16245DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTE16245DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTE16245DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABTE16245WD	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTE16245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ABTE16245DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTE16245DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74ABTE16245DLR	SSOP	DL	48	1000	346.0	346.0	49.0

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

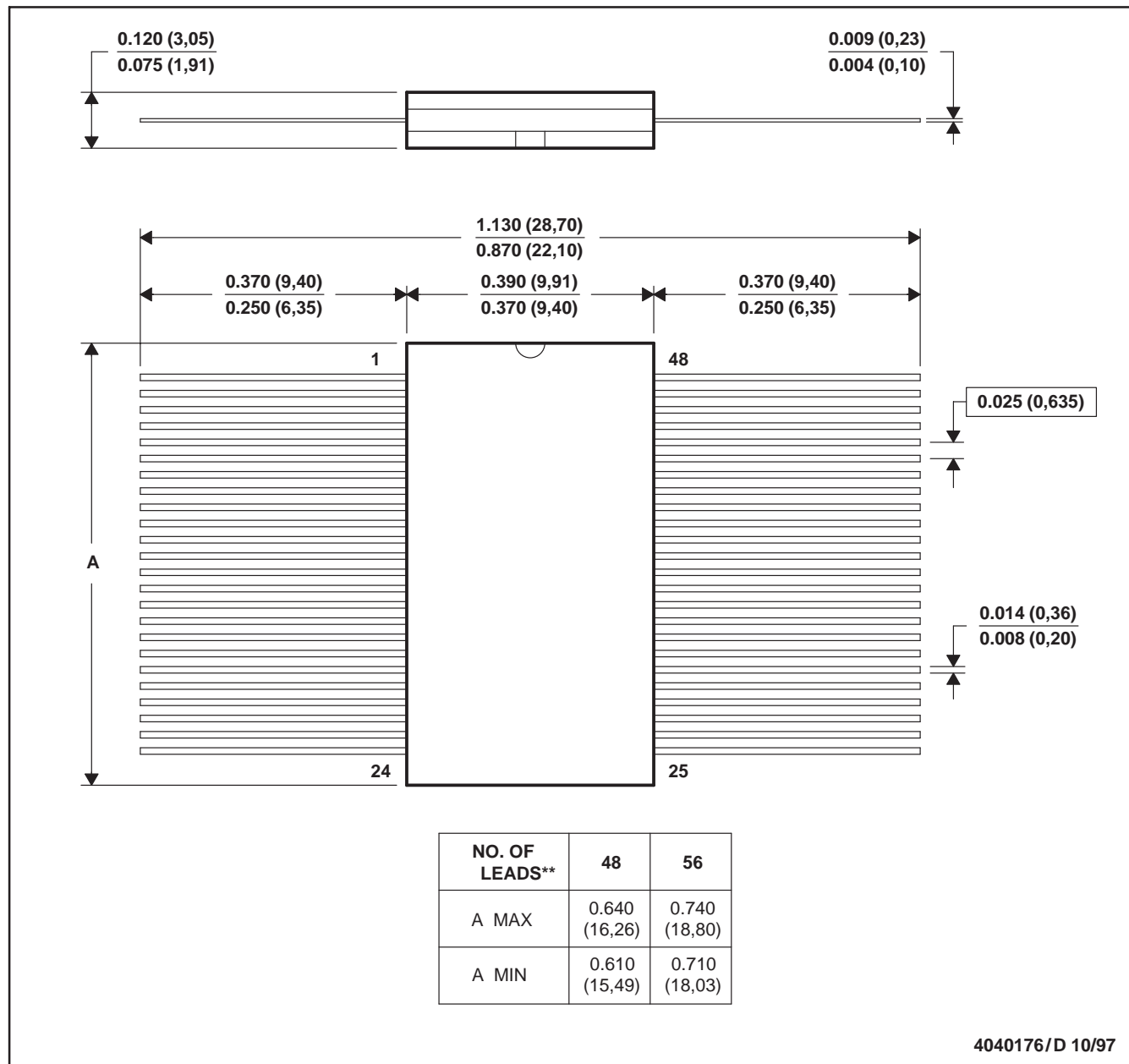


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

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