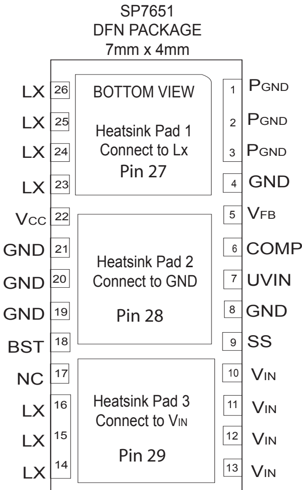
SP7651

Wide Input Voltage Range 3Amp 900kHz Buck Regulator

FEATURES

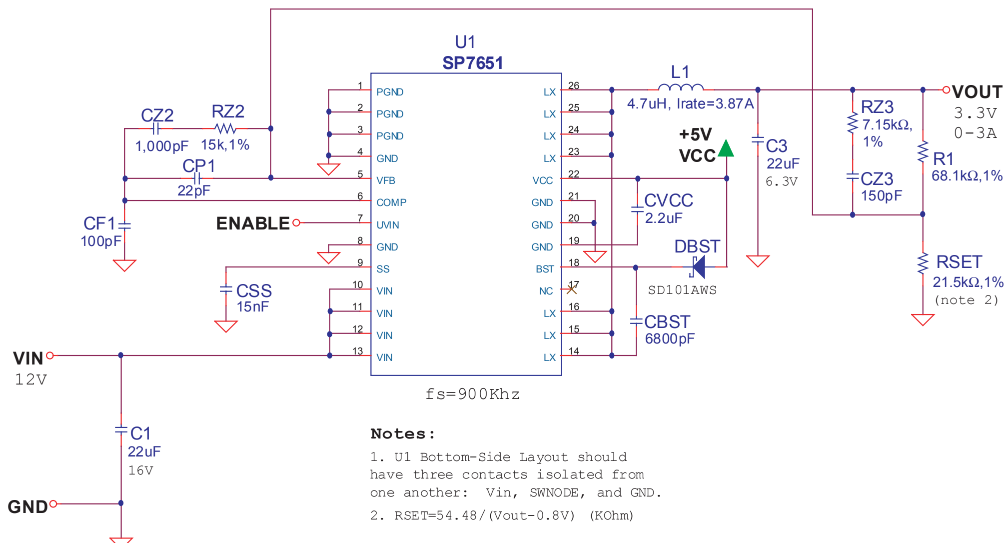
- 2.5V to 20V Step Down Achieved Using Dual Input
- Output Voltage down to 0.8V
- 3A Output Capability (Up to 5A with Air Flow)
- Built in Low R_{DSON} Power FETs (40 mΩ typ)
- Highly Integrated Design, Minimal Components
- 900 kHz Fixed Frequency Operation
- UVLO Detects Both V_{CC} and V_{IN}
- Over Temperature Protection
- Short Circuit Protection with Auto-Restart
- Wide BW Amp Allows Type II or III Compensation
- Programmable Soft Start
- Fast Transient Response
- High Efficiency: Greater than 92% Possible
- Asynchronous Start-Up into a Pre-Charged Output
- Small 7mm x 4mm DFN Package
- U.S. Patent #6,922,041



DESCRIPTION

The SP7651 is a high voltage synchronous step-down switching regulator optimized for high efficiency. The part is designed to be especially attractive for dual supply, 12V step down with 5V used to power the controller. This lower V_{CC} voltage minimizes power dissipation in the part. The SP7651 is designed to provide a fully integrated buck regulator solution using a fixed 900kHz frequency, PWM voltage mode architecture. Protection features include UVLO, thermal shutdown and output short circuit protection. The SP7651 is available in the space saving 7mm X 4mm DFN package.

TYPICAL APPLICATION CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} 7V
V_{IN} 22V
I_{LX} 5A
BST 35V
LX-BST .... -0.3V to 7V
LX .... -1V to 20V

All other pins .... -0.3V to V_{CC}+0.3V

Storage Temperature .... -65°C to 150°C
Power Dissipation .... Internally Limited
ESD Rating .... 2kV HBM
Thermal Resistance Θ_{JC} .... 5°C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: -40°C < T_{AMB} < 85°C, -40°C< Tj <125°C, 4.5V < V_{CC} < 5.5V, 3V< Vin < 20V, BST=LX + 5V, LX = GND = 0.0V, UVIN = 3.0V, CV_{CC} = 1µF, C_{COMP} = 0.1µF, C_{SS} = 50nF, Typical measured at V_{CC} = 5V.
The • denotes the specifications which apply over the full temperature range, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS		CONDITIONS
QUIESCENT CURRENT						
V_{CC} Supply Current (No switching)		1.5	3	mA		V_{FB} =0.9V
V_{CC} Supply Current (switching)		8	12	mA	•	
BST Supply Current (No switching)		0.2	0.4	mA		V_{FB} =0.9V
BST Supply Current (switching)		4	6	mA	•	
PROTECTION: UVLO						
V_{CC} UVLO Start Threshold	4.00	4.25	4.5	V		
V_{CC} UVLO Hysteresis	100	200	300	mV		
UVIN Start Threshold	2.3	2.5	2.65	V	•	
UVIN Hysteresis	200	300	400	mV		
UVIN Input Current			1	µA		UVIN= 3.0V
ERROR AMPLIFIER REFERENCE						
Error Amplifier Reference	0.792	0.800	0.808	V		2X Gain Config., Measure V_{FB}; V_{CC} =5 V, T=25°C
Error Amplifier Reference						
Over Line and Temperature	0.788	0.800	0.812	V	•	
Error Amplifier Transconductance		6		mA/V		
Error Amplifier Gain		60		dB		No Load
COMP Sink Current		150		µA		V_{FB} =0.9V, COMP= 0.9V
COMP Source Current		150		µA		V_{FB} =0.7V, COMP= 2.2V
V_{FB} Input Bias Current		50	200	nA		V_{FB} = 0.8V
Internal Pole		4		MHz		
COMP Clamp		2.5		V		V_{FB} =0.7V, TA=25¼C
COMP Clamp Temp. Coefficient		-2		mV/°C		

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Unless otherwise specified: -40°C < T_{AMB} < 85°C, -40°C<Tj<125°C, 4.5V < V_{CC} < 5.5V, 3V<Vin<20V, BST=LX + 5V, LX = GND = 0.0V, UVIN = 3.0V, CV_{CC} = 1µF, C_{COMP} = 0.1µF, C_{SS} = 50nF, Typical measured at V_{CC} = 5V.
The • denotes the specifications which apply over the full temperature range, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS		CONDITIONS
CONTROL LOOP: PWM COMPARATOR, RAMP & LOOP DELAY PATH						
Ramp Amplitude	0.92	1.1	1.28	V		
RAMP Offset		1.1		V		TA = 25°C, RAMP COMP until GH starts Switching
RAMP Offset Temp. Coefficient		-2		mV/°C		
GH Minimum Pulse Width		90	180	ns	•	
Maximum Controllable Duty Ratio	92	97		%		Maximum Duty Ratio Measured just before pulsing begins
Maximum Duty Ratio	100			%		Valid for 20 cycles
Internal Oscillator Ratio	810	900	990	kHz	•	
TIMERS: SOFTSTART						
SS Charge Current:		10		µA		
SS Discharge Current:	1			mA	•	Fault Present, SS = 0.2V
PROTECTION: Short Circuit & Thermal						
Short Circuit Threshold Voltage	0.2	0.25	0.3	V	•	Measured V_{REF} (0.8V) - VFB
Hiccup Timeout		200		ms		V_{FB} = 0.5V
Number of Allowable Clock Cycles at 100% Duty Cycle		20		Cycles		
Minimum GL Pulse After 20 Cycles		0.5		Cycles		V_{FB} = 0.7V
Thermal Shutdown Temperature		145		°C		V_{FB} = 0.7V
Thermal Recovery Temperature		135		°C		
Thermal Hysteresis		10		°C		
OUTPUT: POWER STAGE						
High Side R_{DSON}		40		mΩ		V_{CC} = 5V ; I_{OUT} = 3A T_{AMB} = 25°C
Synchronous FET R_{DSON}		40		mΩ		V_{CC} = 5V ; I_{OUT} = 3A T_{AMB} = 25°C
Maximum Output Current	3			A		

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Pin #	Pin Name	Description
1-3	P_{GND}	Ground connection for the synchronous rectifier
4,8,19-21	GND	Ground Pin. The control circuitry of the IC and lower power driver are referenced to this pin. Return separately from other ground traces to the (-) terminal of Cout.
5	V_{FB}	Feedback Voltage and Short Circuit Detection pin. It is the inverting input of the Error Amplifier and serves as the output voltage feedback point for the Buck Converter. The output voltage is sensed and can be adjusted through an external resistor divider. Whenever V_{FB} drops 0.25V below the positive reference, a short circuit fault is detected and the IC enters hiccup mode.
6	COMP	Output of the Error Amplifier. It is internally connected to the inverting input of the PWM comparator. An optimal filter combination is chosen and connected to this pin and either ground or V_{FB} to stabilize the voltage mode loop.
7	UVIN	UVLO input for Vin voltage. Connect a resistor divider between V_{IN} and UV_{IN} to set minimum operating voltage.
9	SS	Soft Start. Connect an external capacitor between SS and GND to set the soft start rate based on the 10µA source current. The SS pin is held low via a 1mA (min) current during all fault conditions.
10-13	V_{IN}	Input connection to the high side N-channel MOSFET. Place a decoupling capacitor between this pin and P_{GND}.
14-16,23-26	LX	Connect an inductor between this pinand V_{OUT}
17	NC	No Connect
18	BST	High side driver supply pin. Connect BST to the external boost diode and capacitor as shown in the Typical Application Circuit on page 1. High side driver is connected between BST pin and SWN pin.
22	Vcc	Input for external 5V bias supply

THEORY OF OPERATION

General Overview

The SP7651 is a fixed frequency, voltage mode, synchronous PWM regulator optimized for high efficiency. The part has been designed to be especially attractive for split plane applications utilizing 5V to power the controller and 2.5V to 20V for step down conversion.

The heart of the SP7651 is a wide bandwidth transconductance amplifier designed to accommodate Type II and Type III compensation schemes. A precision 0.8V reference, present on the positive terminal of the error amplifier, permits the programming of the output voltage down to 0.8V via the V_{FB} pin. The output of the error amplifier, COMP, which is compared to a 1.1V peak-to-peak ramp, is responsible for trailing edge PWM control. This voltage ramp, and PWM control logic are governed by the internal oscillator that accurately sets the PWM frequency to 900kHz.

The SP7651 contains two unique control features that are very powerful in distributed applications. First, asynchronous driver control is enabled during startup, to prohibit the low side NFET from pulling down the output until the high side NFET has attempted to turn on. Second, a 100% duty cycle timeout ensures that the low side NFET is periodically enhanced during extended periods at 100% duty cycle. This guarantees the synchronized refreshing of the BST capacitor during very large duty ratios.

The SP7651 also contains a number of valuable protection features. Programmable UVLO allows the user to set the exact V_{IN} value at which the conversion voltage can

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safely begin down conversion, and an internal V_{CC} UVLO ensures that the controller itself has enough voltage to properly operate. Other protection features include thermal shutdown and short-circuit detection. In the event that either a thermal, short-circuit, or UVLO fault is detected, the SP7651 is forced into an idle state where the output drivers are held off for a finite period before a re-start is attempted.

Soft Start

"Soft Start" is achieved when a power converter ramps up the output voltage while controlling the magnitude of the input supply source current. In a modern step down converter, ramping up the positive terminal of the error amplifier controls soft start. As a result, excess source current can be defined as the current required to charge the output capacitor.

$$I_{VIN} = C_{OUT} * (\Delta V_{OUT} / \Delta T_{SOFT\text{-}START})$$

The SP7651 provides the user with the option to program the soft start rate by tying a capacitor from the SS pin to GND. The selection of this capacitor is based on the 10μA pullup current present at the SS pin and the 0.8V reference voltage. Therefore, the excess source can be redefined as:

$$I_{VIN} = C_{OUT} * (\Delta V_{OUT} * 10\mu A / (C_{SS} * 0.8V)$$

Under Voltage Lock Out (UVLO)

The SP7651 contains two separate UVLO comparators to monitor the internal bias (V_{CC}) and conversion (V_{IN}) voltages independently. The V_{CC} UVLO threshold is internally set to 4.25V, whereas the V_{IN} UVLO threshold is programmable through the UVIN pin. When the UVIN pin is greater than 2.5V, the SP7651 is permitted to start up pending the removal of all other faults. Both the V_{CC} and V_{IN} UVLO comparators have been designed with hysteresis to prevent noise from resetting a fault.

Thermal and Short-Circuit Protection

Because the SP7651 is designed to drive large output current, there is a chance that the power converter will become too hot. Therefore, an internal thermal shutdown (145°C) has been included to prevent the IC from malfunctioning at extreme temperatures.

A short-circuit detection comparator has also been included in the SP7651 to protect against an accidental short at the output of the power converter. This comparator constantly monitors the positive and negative terminals of the error amplifier, and if the V_{FB} pin falls more than 250mV (typical) below the positive reference, a short-circuit fault is set. Because the SS pin overrides the internal 0.8V reference during soft start, the SP7651 is capable of detecting short-circuit faults throughout the duration of soft start as well as in regular operation.

Handling of Faults:

Upon the detection of power (UVLO), thermal, or short-circuit faults, the SP7651 is forced into an idle state where the SS and COMP pins are pulled low and the NFETS are held off. In the event of UVLO fault, the SP7651 remains in this idle state until the UVLO fault is removed. Upon the detection of a thermal or short-circuit fault, an internal 200ms timer is activated. In the event of a short-circuit fault, a re-start is attempted immediately after the 200ms timeout expires. Whereas, when a thermal fault is detected the 200ms delay continuously recycles and a re-start cannot be attempted until the thermal fault is removed and the timer expires.

Error Amplifier and Voltage Loop

Since the heart of the SP7651 voltage error loop is a high performance, wide bandwidth transconductance amplifier, great care should be taken to select the optimal compensation network. Because of the amplifier's

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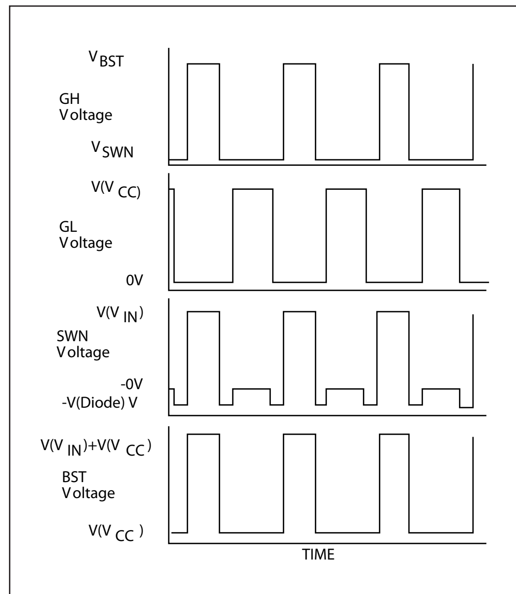
current- limited (+/-150µA) transconductance, there are many ways to compensate the voltage loop or to control the COMP pin externally. If a simple, single pole, single zero response is desired, then compensation can be as simple as an RC circuit to Ground. If a more complex compensation is required, then the amplifier has enough bandwidth (45° at 4 MHz) and enough gain (60dB) to run Type III compensation schemes with adequate gain and phase margins at crossover frequencies greater than 50kHz.

The common mode output of the error amplifier is 0.9V to 2.2V. Therefore, the PWM voltage ramp has been set between 1.1V and 2.2V to ensure proper 0% to 100% duty cycle capability. The voltage loop also includes two other very important features. One is asynchronous startup mode. Basically, the synchronous rectifier cannot turn on unless the high side NFET has attempted to turn on or the SS pin has exceeded 1.7V. This feature prevents the controller from "dragging down" the output voltage during startup or in fault modes. The second feature is a 100% duty cycle timeout that ensures synchronized refreshing of the BST capacitor at very high duty ratios. In the event that the high side NFET is on for 20 continuous clock cycles, a reset is given to the PWM flip-flop half way through the 21st cycle. This forces GL to rise for the cycle, in turn refreshing the BST capacitor.

Power MOSFETs

The SP7651 contains a pair of integrated low resistance N MOSFETs designed to drive up to 3A of output current. Maximum output current could be limited by thermal limitations of a particular application. The SP7651 incorporates a built-in over-temperature protection to prevent internal overheating.



Setting Output Voltages

The SP7651 can be set to different output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin V_{FB}, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

Vout = 0.80V (R1 / R2 + 1) =>

$$R2 = \frac{R1}{[(V_{OUT}/0.80V) - 1]}$$

Where R1 = 68.1KΩ and for Vout = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of the R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that 50KΩ < R1 < 100KΩ for overall system loop stability.

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Inductor Selection

There are many factors to consider in selecting the inductor, including: core material, inductance vs. frequency, current handling capability, efficiency, size and EMI. In a typical SP7651 circuit, the inductor is chosen primarily by operating frequency, saturation current and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. Low inductor values provide the smallest size, but cause large ripple currents, poor efficiency and require more output capacitance to smooth out the larger ripple current. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. A good compromise between size, loss and cost is to set the inductor ripple current to be within 20% to 40% of the maximum output current.

The switching frequency and the inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}\,(V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)}\,F_S\,K_r\,I_{OUT(MAX)}}$$

where:

Fs = switching frequency

Kr = ratio of the AC inductor ripple current to the maximum output current

The peak-to-peak inductor ripple current is:

$$I_{PP} = \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)}\,F_S\,L}$$

Once the required inductor value is selected, the proper selection of core material is based on peak inductor current and efficiency requirements. The core must be large enough not to saturate at the peak inductor current...

$$I_{PEAK} = I_{OUT(MAX)} + \frac{I_{PP}}{2}$$

...and provide low core loss at the high switching frequency. Low cost powdered-iron cores are inappropriate for 900kHz operation. Gapped ferrite inductors are widely available for consideration. Select devices that have operating data shown up to 1MHz. Ferrite materials, on the other hand, are more expensive and have an abrupt saturation characteristic with the inductance dropping sharply when the peak design current is exceeded. Nevertheless, they are preferred at high switching frequencies because they present very low core loss and the design only needs to prevent saturation. In general, ferrite or molypermalloy materials will be used with the SP7651.

Optimizing Efficiency

The power dissipated in the inductor is equal to the sum of the core and copper losses. To minimize copper losses, the winding resistance needs to be minimized, but this usually comes at the expense of using a larger inductor. Core losses have a more significant contribution at low output current where the copper losses are at a minimum, and can typically be neglected at higher output currents where the copper losses dominate. Core loss information is usually available from the magnetics vendor. Proper inductor selection can affect the resulting power supply efficiency by more than 15-20%!

The copper loss in the inductor can be calculated using the following equation:

$$P_{L(CU)} = I^2_{L(RMS)}\; R_{WINDING}$$

where $I_{L(RMS)}$ is the RMS inductor current that can be calculated as follows:

$$I_{L(RMS)} = I_{OUT(MAX)}\sqrt{1 + \frac{1}{3}\left(\frac{I_{PP}}{I_{OUT(MAX)}}\right)^2}$$

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Output Capacitor Selection

The required ESR (Equivalent Series Resistance) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage do not exceed the tolerance limits expected on the output voltage. During an output load transient, the output capacitor must supply all the additional current demanded by the load until the SP7651 adjusts the inductor current to the new value.

In order to maintain $V_{OUT,}$ the capacitance must be large enough so that the output voltage is held up while the inductor current ramps up or down to the value corresponding to the new load current. Additionally, the ESR in the output capacitor causes a step in the output voltage equal to the current. Because of the fast transient response and inherent 100% to 0% duty cycle capability provided by the SP7651 when exposed to an output load transient, the output capacitor is typically chosen for ESR, not for capacitance value.

The ESR of the output capacitor, combined with the inductor ripple current, is typically the main contributor to output voltage ripple. The maximum allowable ESR required to maintain a specified output voltage ripple can be calculated by:

$$R_{ESR} \leq \frac{\Delta V_{OUT}}{I_{PK-PK}}$$

where:

ΔV_{OUT} = Peak-to-Peak Output Voltage Ripple

I_{PK-PK} = Peak-to-Peak Inductor Ripple Current

The total output ripple is a combination of the ESR and the output capacitance value and can be calculated as follows:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP}(1-D)}{C_{OUT}F_S}\right)^2 + (I_{PP}R_{ESR})^2}$$

F_S = Switching Frequency

D = Duty Cycle

C_{OUT} = Output Capacitance Value

Input Capacitor Selection

The input capacitor should be selected for ripple current rating, capacitance and voltage rating. The input capacitor must meet the ripple current requirement imposed by the switching current. In continuous conduction mode, the source current of the high-side MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. Most of this current is supplied by the input bypass capacitors. The RMS value of input capacitor current is determined at the maximum output current and under the assumption that the peak-

to-peak inductor ripple current is low; it is given by:

$$I_{CIN(rms)} = I_{OUT(max)} \sqrt{D(1 - D)}$$

The worse case occurs when the duty cycle D is 50% and gives an RMS current value equal to $I_{OUT}/2$. Select input capacitors with adequate ripple current rating to ensure reliable operation.

The power dissipated in the input capacitor is:

$$P_{ON} = I^2_{ON(RMS)} R_{ESR(CIN)}$$

This can become a significant part of power losses in a converter and hurt the overall energy transfer efficiency. The input voltage ripple primarily depends on the input capacitor ESR and capacitance. Ignoring the inductor ripple current, the input voltage ripple can be determined by:

$$\Delta V_{IN} = I_{OUT(MAX)} R_{ESR(CIN)} + \frac{I_{OUT(MAX)} V_{OUT} (V_{IN} - V_{OUT})}{F_S C_{IN} V_{IN}^2}$$

The capacitor type suitable for the output capacitors can also be used for the input capacitors. However, exercise extra caution

when tantalum capacitors are used. Tantalum capacitors are known for catastrophic failure when exposed to surge current, and input capacitors are prone to such surge current when power supplies are connected “live” to low impedance power sources.

Loop Compensation Design

The open loop gain of the whole system can be divided into the gain of the error amplifier, PWM modulator, buck converter output stage, and feedback resistor divider. In order to cross over at the selected frequency FCO, the gain of the error amplifier compensates for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate loop frequency response such that its gain crosses over 0db at a slope of -20db/dec. The first step of compensation design is to pick the loop crossover frequency.

High crossover frequency is desirable for fast transient response, but often jeopardizes the higher than the ESR zero but less than 1/5 of the switching frequency. The ESR zero is contributed by the ESR associated with the output capacitors and can be determined by:

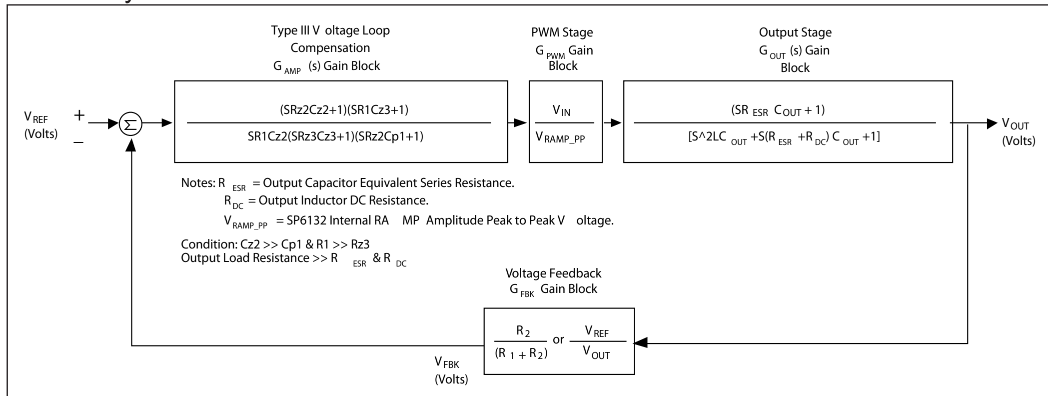
system stability. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The ESR zero is contributed by the ESR associated with the output capacitors and can be determined by:

$$f_{Z(ESR)} = \frac{1}{2\pi\, C_{OUT}\, R_{ESR}}$$

The next step is to calculate the complex conjugate poles contributed by the LC output filter,

$$f_{P(LC)} = \frac{1}{2\pi \sqrt{L\, C_{OUT}}}$$

When the output capacitors are Ceramic type, the SP7651 Evaluation Board requires a Type III compensation circuit to give a phase boost of 180° in order to counteract the effects of an underdamped resonance of the output filter at the double pole frequency.



SP7651 Voltage Mode Control Loop with Loop Dynamic

Definitions:

R_{ESR} = Output Capacitor Equivalent Series Resistance

R_{DC} = Output Inductor DC Resistance

R_{RAMP_PP} = SP7651 internal RAMP Amplitude Peak-to-Peak Voltage

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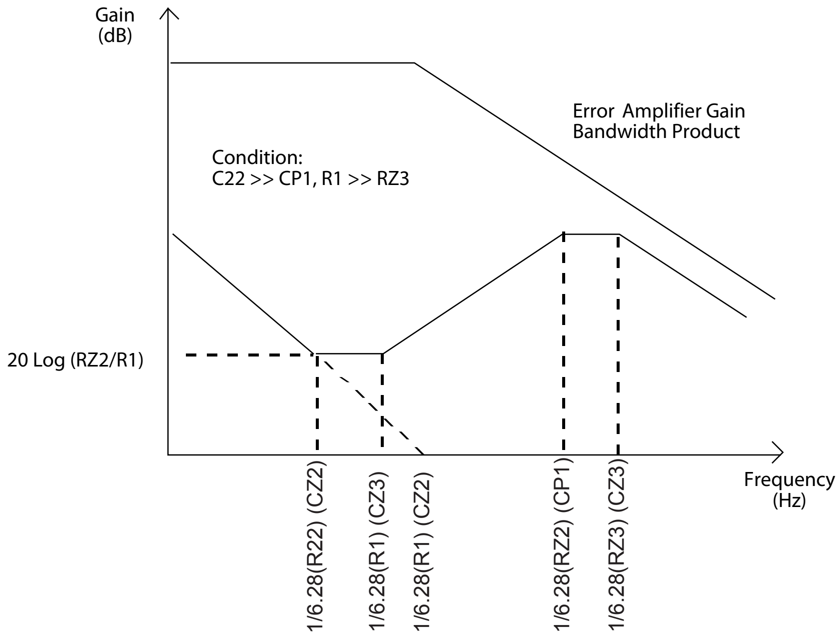
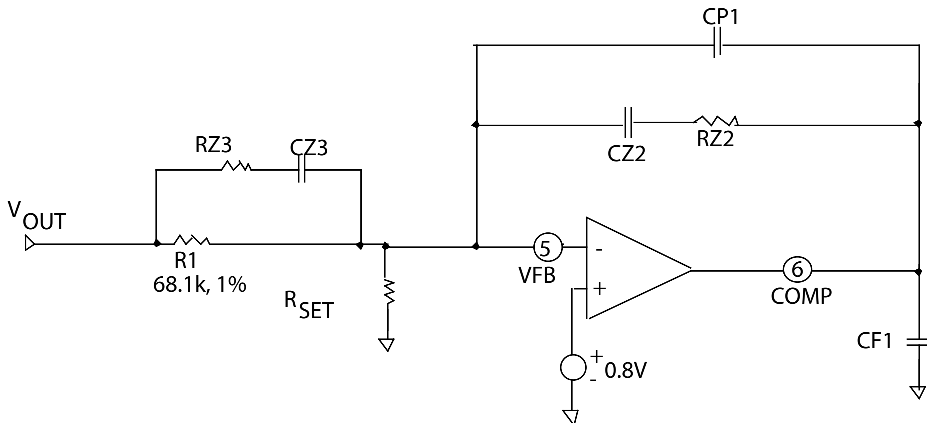


Bode Plot of Type III Error Amplifier Compensation.



Type III Error Amplifier Compensation Circuit

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SP765X Thermal Resistance

The SP765X family has been tested with a variety of footprint layouts along with different copper area and thermal resistance has been measured. The layouts were done on 4 layer FR4 PCB with the top and bottom layers using 3oz copper and the power and ground layers using 1oz copper.

For the Minimum footprint, only about 0.1 square inch of 3 ounces of copper was used on the top or footprint layer, and this layer had no vias to connect to the 3 other layers. For the Medium footprint, about 0.7 square inches of 3 ounces of copper was used on the top layer, but vias were used to connect to the other 3 layers. For the Maximum footprint, about 1.0 square inch of 3 ounces of copper was used on the top layer and many vias were used to connect to the 3 other layers.

The results show that only about 0.7 square inches of 3 ounces of copper on the top layer and vias connecting to the 3 other layers are needed to get the best thermal resistance of 36°C/W. Adding area on the top beyond the 0.7 square inches did not reduce thermal resistance.

Using a minimum of 0.1 square inches of (3 ounces of) Copper on the top layer with no vias connecting to the 3 other layers produced a thermal resistance of 44°C/W. This thermal impedance is only 22% higher than the medium and large footprint layouts, indicating that space constrained designs can still benefit thermally from the Powerblox family of ICs. This indicates that a minimum footprint of 0.1 square inch, if used on a 4 layer board, can produce 44°C/W thermal resistance. This approach is still very worthwhile if used in a space constrained design.

The following page shows the footprint layouts from an ORCAD file. The thermal data was taken for still air, not with forced air. If forced air is used, some improvement in thermal resistance would be seen.

SP765X Thermal Resistance

4 Layer Board:
Top Layer 3ounces Copper
GND Layer 1ounce Copper
Power Layer 1ounce Copper
Bottom Layer 3ounces Copper

Minimum Footprint: 44°C/W
Top Layer: 0.1 square inch
No Vias to other 3 Layers

Medium Footprint: 36°C/W
Top Layer: 0.7 square inch
Vias to other 3 Layers

Maximum Footprint: 36°C/W
Top Layer: 1.0 square inch
Vias to other 3 Layers

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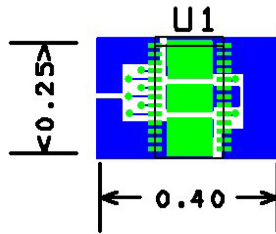
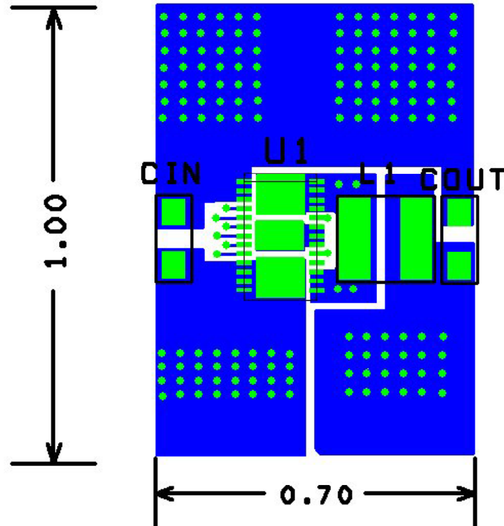
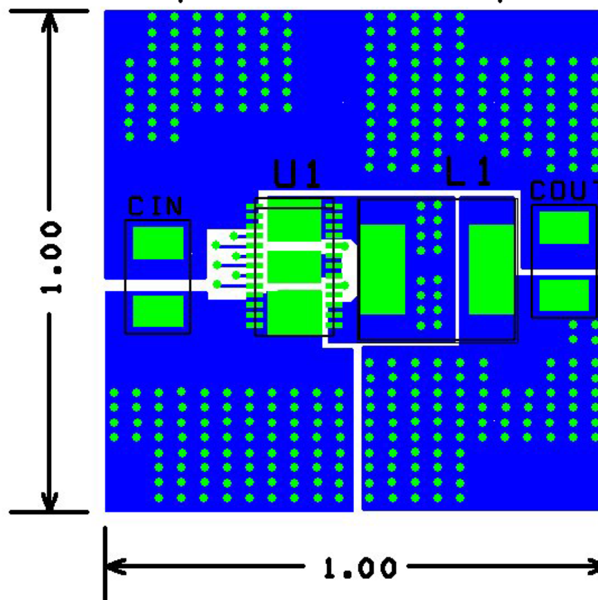
MINIMUM FOOTPRINT = 0.10 SQ IN.



MEDIUM FOOTPRINT = 0.70 SQ IN.





MAXIMUM FOOTPRINT = 1.0 SQ IN.

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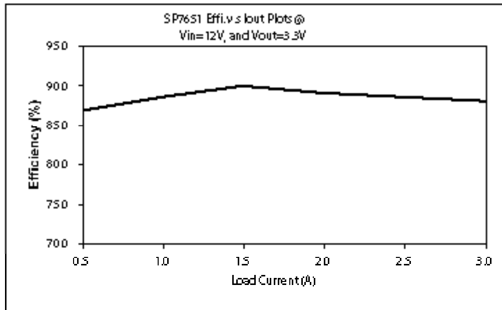

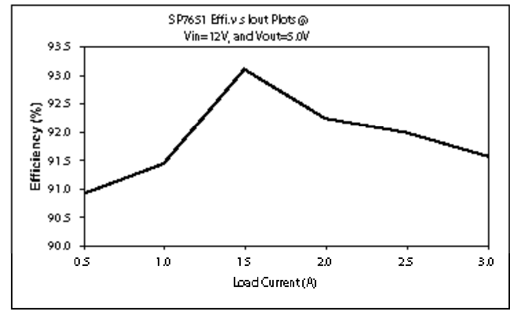

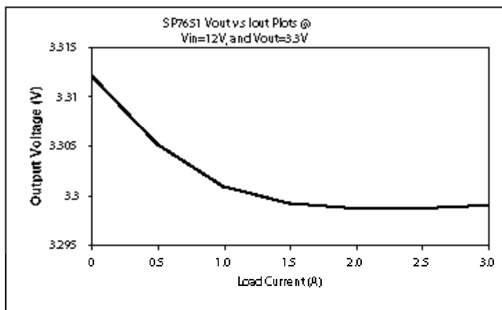

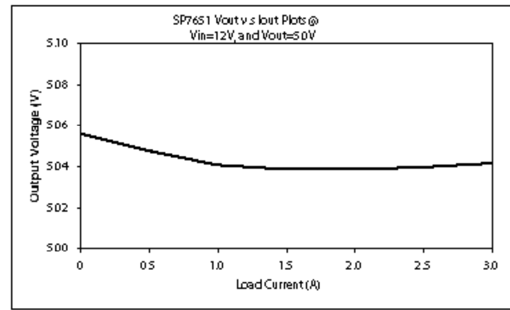

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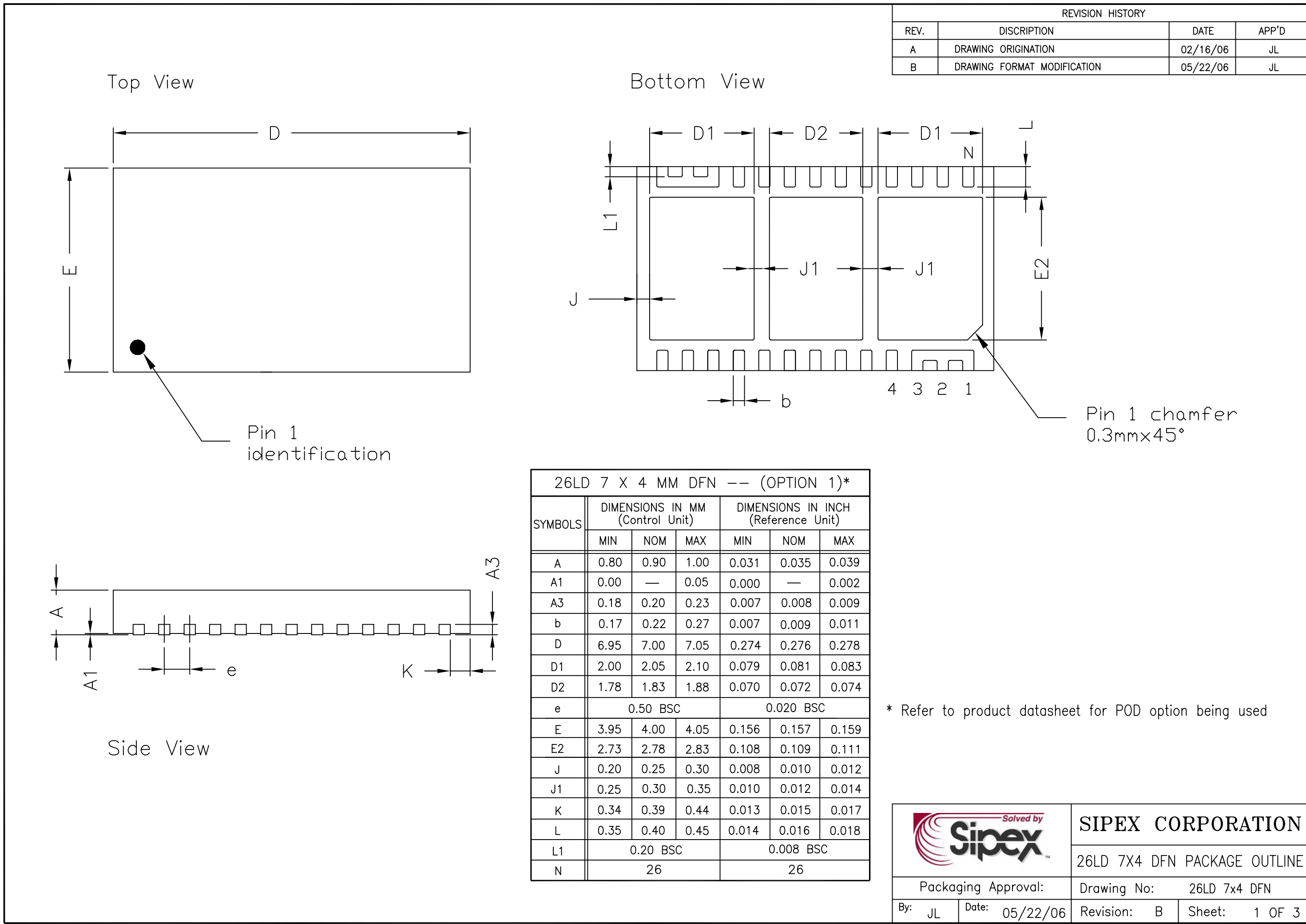

REVISION HISTORY

REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	02/16/06	JL
B	DRAWING FORMAT MODIFICATION	05/22/06	JL

26LD 7 X 4 MM DFN -- (OPTION 1)*

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	—	0.05	0.000	—	0.002
A3	0.18	0.20	0.23	0.007	0.008	0.009
b	0.17	0.22	0.27	0.007	0.009	0.011
D	6.95	7.00	7.05	0.274	0.276	0.278
D1	2.00	2.05	2.10	0.079	0.081	0.083
D2	1.78	1.83	1.88	0.070	0.072	0.074
e		0.50 BSC			0.020 BSC	
E	3.95	4.00	4.05	0.156	0.157	0.159
E2	2.73	2.78	2.83	0.108	0.109	0.111
J	0.20	0.25	0.30	0.008	0.010	0.012
J1	0.25	0.30	0.35	0.010	0.012	0.014
K	0.34	0.39	0.44	0.013	0.015	0.017
L	0.35	0.40	0.45	0.014	0.016	0.018
L1		0.20 BSC			0.008 BSC	
N		26			26	

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Part Number	Package Code	RoHS	MIN. Temp. (°C)	MAX. Temp.(°C)	Status	Pack Quantity
SP7651ER	DFN26		-40	85	Active	Bulk
SP7651ER/TR	DFN26		-40	85	Active	500 Tape & Reel
SP7651ER-L	DFN26	▪	-40	85	Active	Bulk
SP7651ER-L/TR	DFN26	▪	-40	85	Active	500 Tape & Reel

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Appendix and Web Link Information

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The following sections contain information which is more changeable in nature and is therefore generated as appendices.

1) **Package Outline Drawings**
2) **Ordering Information**

If Available:

3) **Frequently Asked Questions**
4) **Evaluation Board Manuals**
5) **Reliability Reports**
6) **Product Characterization Reports**
7) **Application Notes for this product**
8) **Design Solutions for this product**

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APPLICATION NOTE ANP4

CAD Layout Recommendations for the PowerBlox™ Family

Introduction

The Sipex PowerBlox™ family of parts offers designers a very high power density solution for wide input range buck requirements. As a result of down converting power that can be greater than 50W in a 7 x 4 mm package, care is needed with the layout in order to manage the thermal requirements. In addition, the 26 pin DFN package selected for its excellent thermal performance must be used in conjunction with the correct CAD shape, to ensure good solder-ability during the manufacturing stage. This application note will address these, along with more general layout issues.

General Layout Recommendations.

As with all dc to dc designs, good layout practice is essential to getting the correct operation and expected performance from a solution. Below is a list of guidelines for the PowerBlox™ family:

1) A typical application circuit is shown in figure 1. All components in the power path should be located on one side (which will be referred to as the topside) of the PCB, and as physically close as possible to the PowerBlox™ device. For PowerBlox™ designs these components are: Input Capacitors (connected between Vin and PGnd – C1 in Figure 1); Output Capacitors (connected between Vout and PGnd – C3); Inductor (L1); PowerBlox™ (SP765x) device. Note: If an additional Schottky diode and/or snubber network is used connected between LX and Pgnd, these should also be subject to the same constraints.

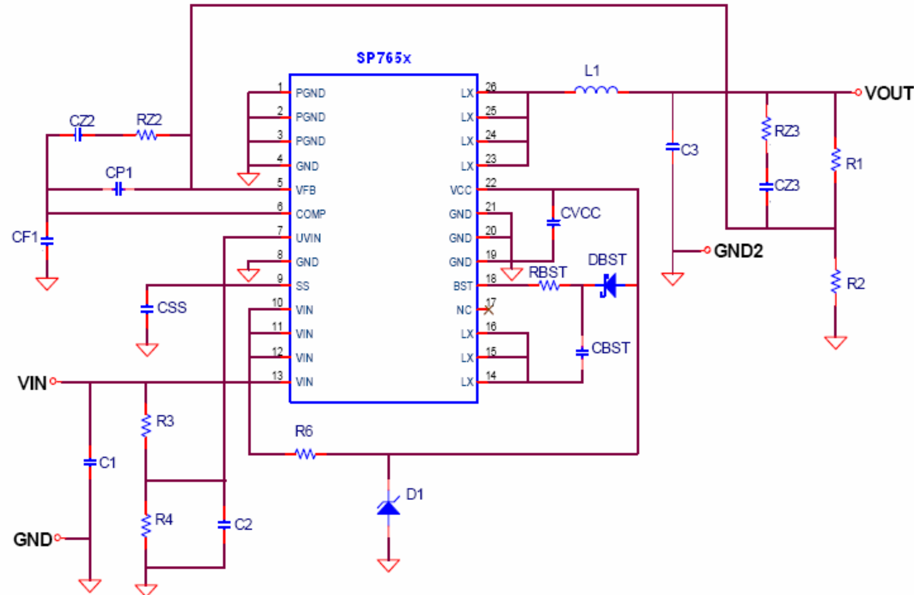

Figure 1 Typical PowerBlox™ Circuit

2) All routing to and from the above components should be done on the topside of the PCB. The routing should be done by making local split topside planes for Vin, Vout, Pgnd and LX or copper fills between the components (see example in Figure 2). Note: The use of vias in the power path is to be avoided.

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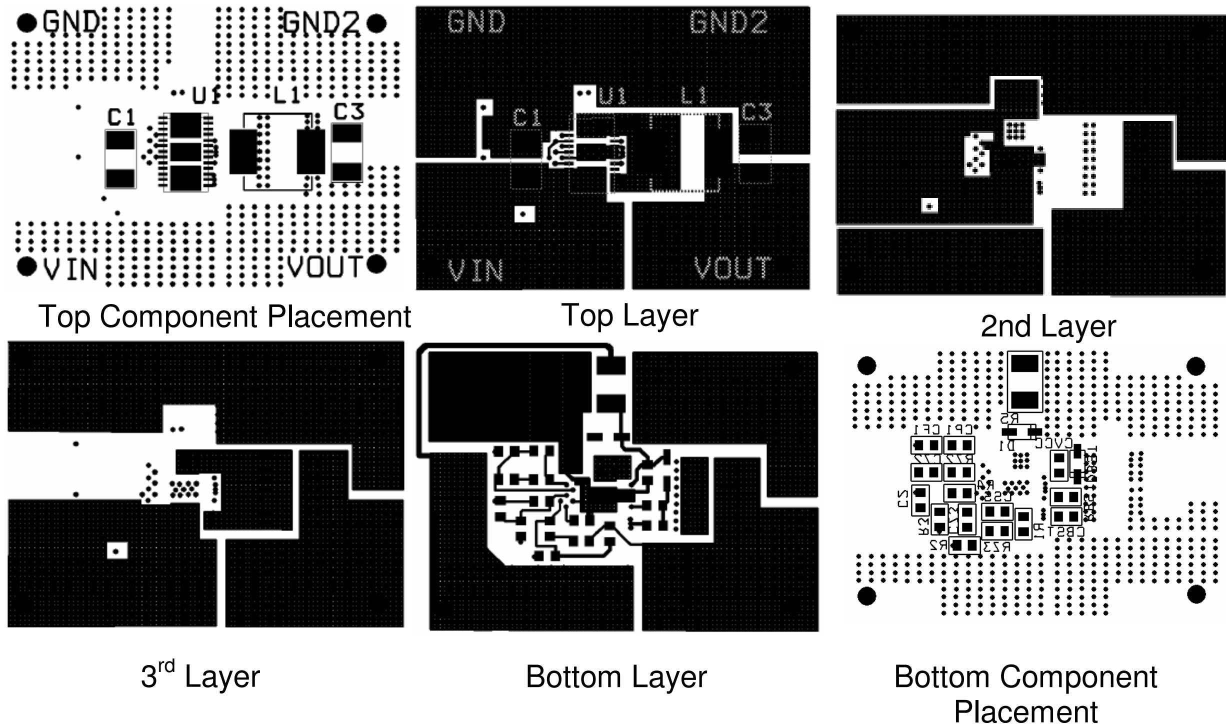

Figure 2 Example PowerBlox™ Layout (2 Sided Component Placement)

3) If components are to be placed on both sides of the PCB then all feedback, compensation and bias supply passives should be on the bottom side of the PCB. Routing to these parts should also be done on the side on which they are mounted (see Figure 2). If an additional routing layer is available and required, then the layer closest to the bottom one is preferred. The path from the feedback resistor chain (R1 and R2 in Figure 1) should not be routed underneath the LX node or inductor.

4) Pgnd and Gnd should be kept as separate nets, with a single common connection (star), made by a short track from Pgnd to Gnd power pad under the device (Figure 3).

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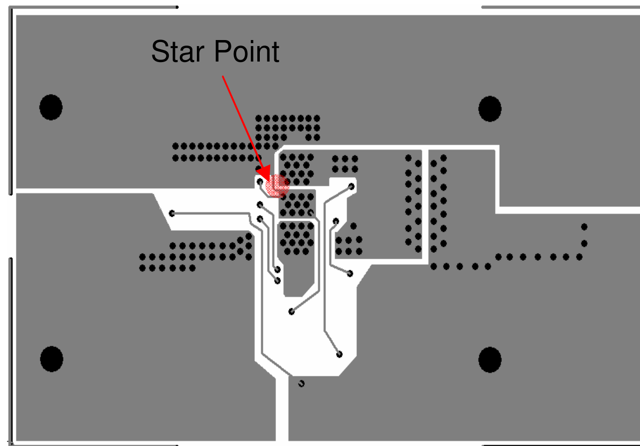

Figure 3 Common Connection point for Pgnd and Gnd

Thermal Considerations

The 26 pin DFN package is thermally enhanced by providing 3 separate pads on its lower side. These are electrically connected to the LX, Gnd and Vin pins. The shape and size of the pads used on the CAD footprint, and the surrounding PCB layout thus determine the thermal performance of the complete assembly. Two sizes of layout are recommended for the PowerBlox™ parts, their performance is a trade off between space available and thermal capacity.

Figure 4 shows the smaller layout. In this set up there are no vias required linking any planes to the power pads beneath the device. It should be noted that although this layout has no vias on the thermal pads, there is some thermal conductivity between the relatively small component layer planes and the much larger inner layer planes and bottom planes, which helps reduce thermal resistance. It has a θ_{ja} of 44˚C/W.

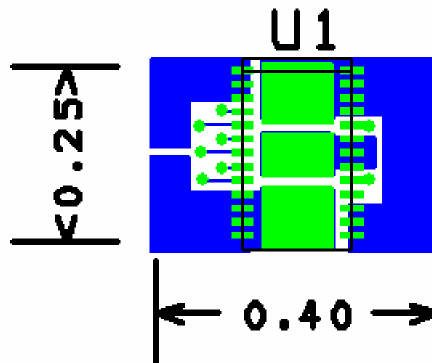

Figure 4 SP765x Minimum Footprint (0.1 in^2)

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The larger layout shown in Figure 5 has an improved thermal resistance of θ_{ja} = 36˚C/W. This layout also uses 6 vias per pad onto 3 other PCB planes. Since this layout has vias connecting to much larger planes below, increasing the top area size beyond 0.7 in^2 has little effect in decreasing the thermal resistance.

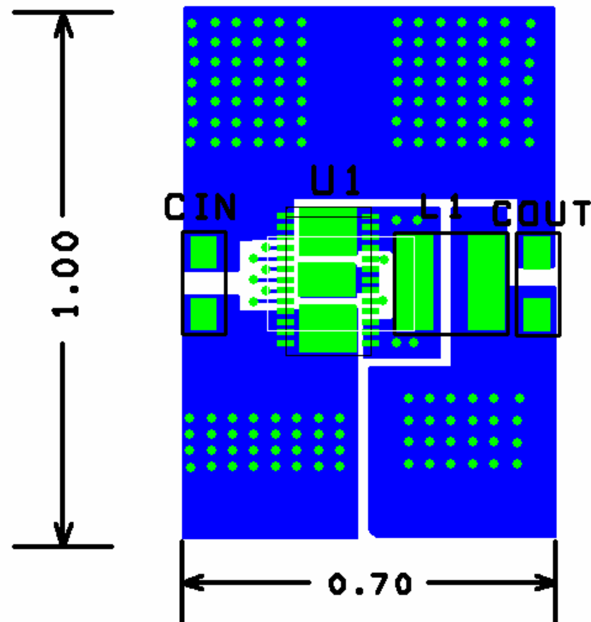

Figure 5 SP765x Maximum Footprint (0.7 in^2)

It should be noted that the above figures are based upon a 4 layer FR4 PCB, with 3oz copper on the top and bottom layers, 1 oz copper on inner layers. For lower densities of copper, since the relationship between area and density with respect to thermal conductivity is linear, a lower density can be compensated for by a proportional increase in area.

CAD Footprint Recommendations

The correct CAD footprint is not only important to effective thermal management of the solution, it can also have a marked effect on the ease of manufacture. To evaluate the reliability of the CAD footprint, a solder test was performed using 3 different footprint shapes. The first shape used a footprint with signal pads 2x the length of PowerBlox™ pads, and the 3 power pads were about the same size as the PowerBlox™ thermal pads. The second footprint also used signal pads 2x the length of the PowerBlox™ signal pads, but the power pads width was reduced to about 15mils less than the PowerBlox™ power pads. The third shape used signal pads 1.5x the length of the PowerBlox™ signal pads and the power pads width reduced about 15mils less than the PowerBlox™ power pads.
The 3 footprints were all tested the way: we made 2 layer PCBs and had a contract manufacturer using pick and place equipment and reflow soldering system to assemble 20 parts of each footprint. The parts were burned in by thermal cycling from 0 to 100degC and -65 to 150degC. All the assembled parts were visually inspected for defects and electrically tested for continuity at read points of 0, 500, 1000 cycles. All passed visual and electrical tests and no there were no solder joint cracks. Footprint number 3 was selected as the recommended footprint for two

reasons: preferences by some customers for the solder land = 1.5x the actual land on the package, plus the thermal pad size was considered better by our packaging engineer to be smaller than the size on the package.

The recommended footprint is reproduced in Figure 6.

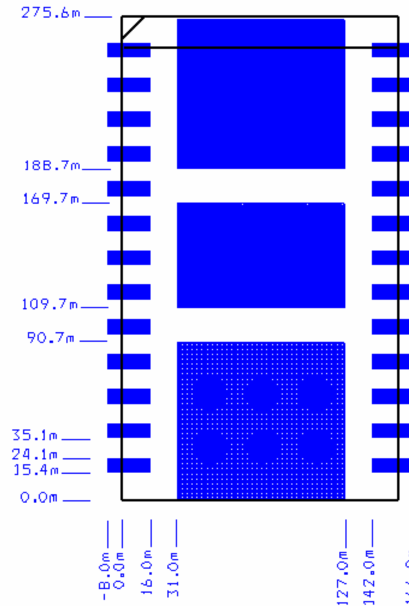

Figure 6 Recommended SP765x CAD Footprint

A 4 mil stencil should be used during the manufacturing stage, with pads the same size as the CAD footprint pads. If vias are determined to be necessary, these should be limited to a maximum of 9 per pad. (Additional ones give very limited improvement to θ_{ja}). The pads should be joined to the corresponding electrically connected power pads by a short, direct track (see Figure 7), not by filling the gap area with copper. Note that special plugging of the vias prior to reflow is not required.

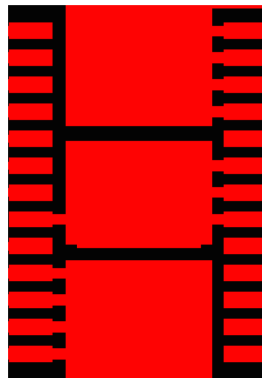

Figure 7 Correct Joining of Signal to Power Pads

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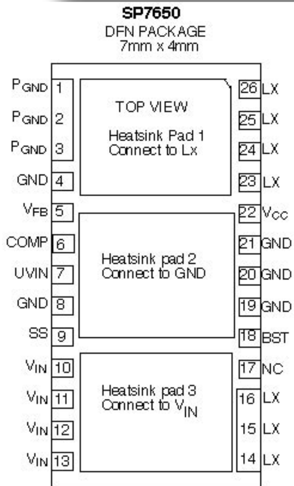
Sipex® Application Note PowerBlox™

Thermal Resistance on SP765X Devices

by Brian Kennedy



The SP765X series of devices is a family of synchronous step-down switching regulators optimized for high efficiency, with industry leading power density. The parts are designed to be especially attractive for dual supply, 12V or 24V distributed power systems step down with 5V used to power the controller. This lower V_{CC} voltage minimizes power dissipation in the part and is used to drive the top switch. The SP765x family is designed to provide a fully integrated buck regulator solution using a fixed frequency, PWM voltage mode architecture. Protection features include UVLO, thermal shutdown and output short circuit protection. The SP765X are available in the space saving and robust DFN package. This application note explains the thermal resistance characteristics of the family of devices and the implications for usage.

Available in Lead Free Packaging

SP765X Thermal Resistance

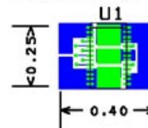
4 Layer Board:
Top Layer 3oz copper
GND Layer 1oz copper
Power Layer 1oz copper
Bottom Layer 3oz copper

Minimum Footprint: 44°C/W
Top Layer: 0.1 sq in.
No Vias to other 3 Layers

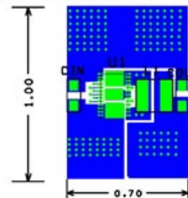
Medium Footprint: 36°C/W
Top Layer: 0.7 sq in.
Vias to other 3 Layers

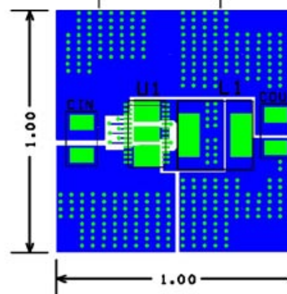
Maximum Footprint: 36°C/W
Top Layer: 1.0 sq in.
Vias to other 3 Layers

MINIMUM FOOTPRINT = 0.10 SQ IN.



MEDIUM FOOTPRINT = 0.70 SQ IN.





MAXIMUM FOOTPRINT = 1.0 SQ IN.

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SP765X Thermal Resistance Application Note

The SP765X family has been tested with a variety of footprint layouts along with different copper area and thermal resistance has been measured. The layouts were done on 4 layer FR4 PCB with the top and bottom layers using 3oz copper and the power and ground layers using 1oz copper.

For the Minimum footprint, only about 0.1 sq in. of 3oz copper was used on the top or footprint layer, and this layer had no vias to connect to the 3 other layers. For the Medium footprint, about 0.7 sq in of 3oz copper was used on the top layer, but vias were used to connect to the other 3 layers. For the Maximum footprint, about 1.0 sq in. of 3oz copper was used on the top layer and many vias were used to connect to the 3 other layers.

The results show that only about 0.7sq in. of 3oz copper on the top layer and vias connecting to the 3 other layers are needed to get the best thermal resistance of 36°C/W. Adding area on the top beyond the 0.7 sq in. did not reduce thermal resistance.

Using a minimum of 0.1 sq in. of 30z copper on the top layer with no vias connecting to the 3 other layers produced a thermal resistance of 44°C/W. This value of 44°C/W is only 22% more than the best thermal resistance of 36°C/W. This indicates that a minimum footprint of 0.1sq in. if used on a 4 layer board can produce 44°C/W thermal resistance, which is still very good if used in a space constrained design.

The following page shows the footprint layouts from an ORCAD file. The thermal data was taken for still air, not with forced air. If forced air is used, some improvement in thermal resistance would be seen.

ANALOG EXCELLENCE

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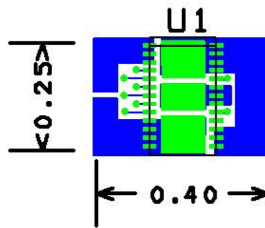
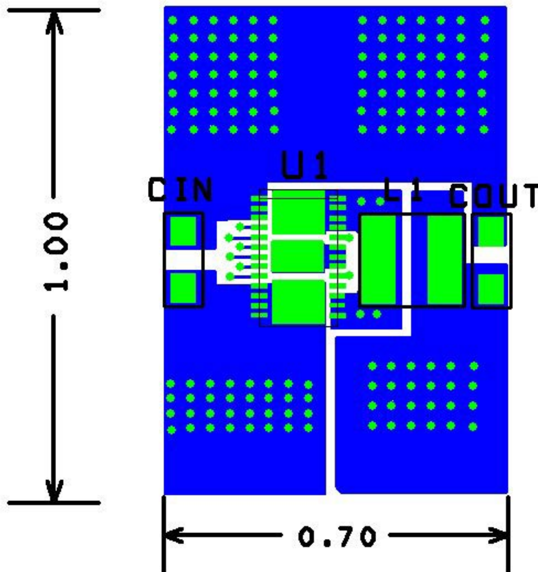
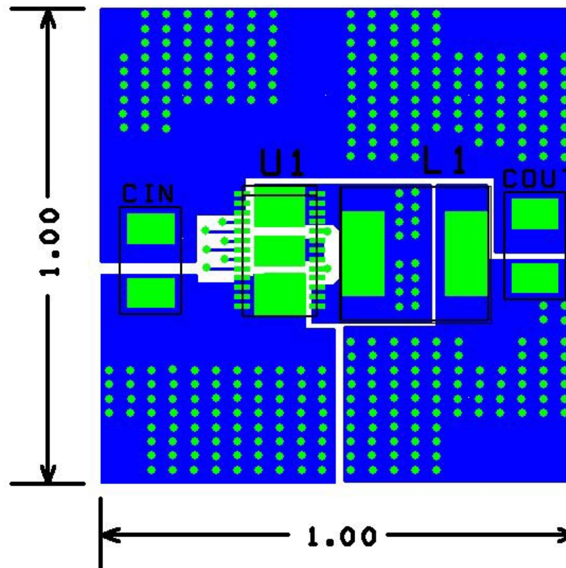
MINIMUM FOOTPRINT = 0.10 SQ IN.



MEDIUM FOOTPRINT = 0.70 SQ IN.





MAXIMUM FOOTPRINT = 1.0 SQ IN.

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Application Note ANP6

PowerBlox™ in Distributed Power Architectures

Introduction

The challenges in designing POL converters for distributed power architectures (see Figure 1) in telecom systems are many. System boards are very space constrained and the power solution must occupy minimal PCB real estate. Efficiency is of great importance to improve the throughput efficiency of the system as well as to minimize temperature rise in components and ensure long life. Also, the loads on the system board require complex and unique protocols that are provided in the ASIC or NPU manufacturer specifications. This sequencing function is usually done using a proprietary IC and high current MOSFETs on the output of each rail. These MOSFETs are 100% duty cycle switches that lower the efficiency of the system, generate heat and increase the cost of the system.

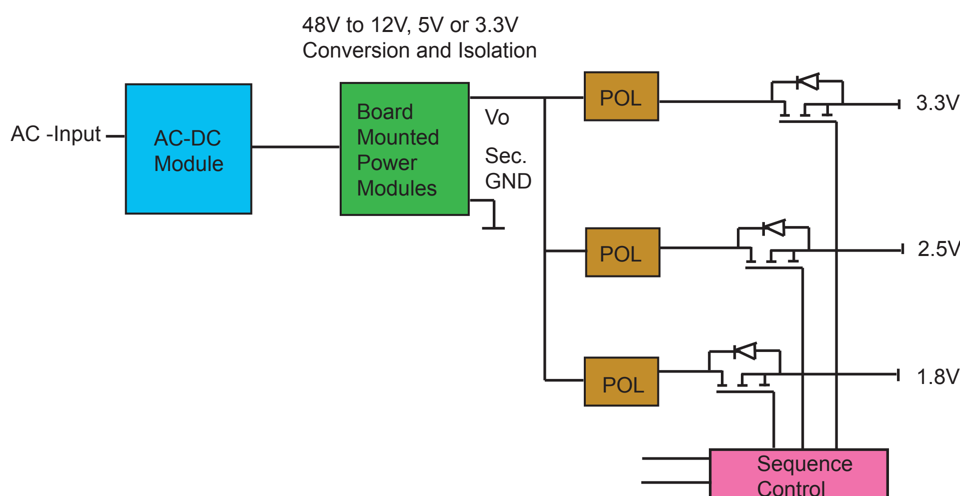

Figure 1. Distributed Power Architecture in a Telecommunications System

The PowerBlox™ Solution

Sipex has introduced a family of high current regulators called PowerBlox™ that address these system level requirements. The PowerBlox™ family of products are available in a range of output current levels from 3A to 8A and switching frequencies from 300kHz to 1.2MHz. An example of such a device is the SP7652 available in a space saving 7mm x 4mm DFN package. It is capable of accepting a wide input voltage and can provide up to 6A at output voltages as low as 0.8V. Since the switching frequency of the SP7652 is 600kHz, output filter size is reduced, enabling a very small solution ideal for applications where PCB real estate is at a premium. The built in low RDS(on) FETs enable high efficiency. Figure 2 shows the SP7652 delivering over 92% efficiency over the entire load range.

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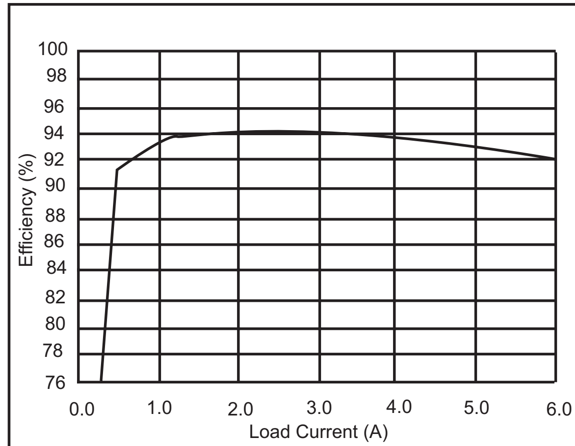

Figure 2. Efficiency versus Load Current for SP7652 at $5V_{IN}$ and $3.3V_{OUT}$

The SP7652 includes protection features such as UVLO on both V_{CC} and V_{IN} pins, programmable soft start and thermal shutdown. The SP7652 also has short circuit protection with auto-restart. This auto-restart feature is key in today's end telecom or networking systems, many of which are in remote locations. Auto-restart capabilities increase up-time and reduce maintenance costs thereby improving QoS.

Implementing Power-Up Protocols

One of the most compelling reason for using this part in telecom systems is the ability to easily implement power-up protocols.

There are essentially three types of power-up protocols used in distributed power architectures: Sequential, ratiometric, and simultaneous (or output tracking). These protocols are described below.

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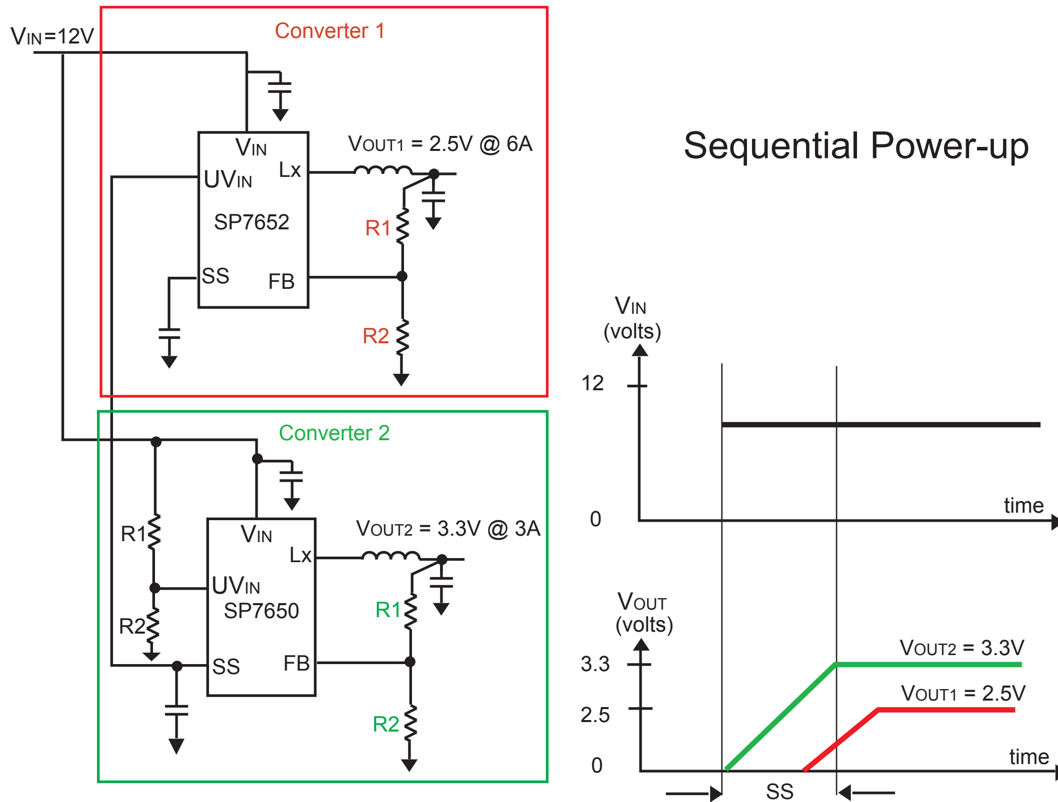

Figure 3. Sequential Power-up Implemented with PowerBlox™

1. Sequential Power-up

In sequential power-up, one voltage rail is turned on and, after a predetermined interval, the second voltage is turned on. Sequential power-up is required in systems where the core voltage rail must turn on before the I/O or chipset rails are turned on. This start up protocol can be easily implemented using the PowerBlox™ chips, by connecting the UVIN of one converter to the soft start of the other as shown in Figure 3.

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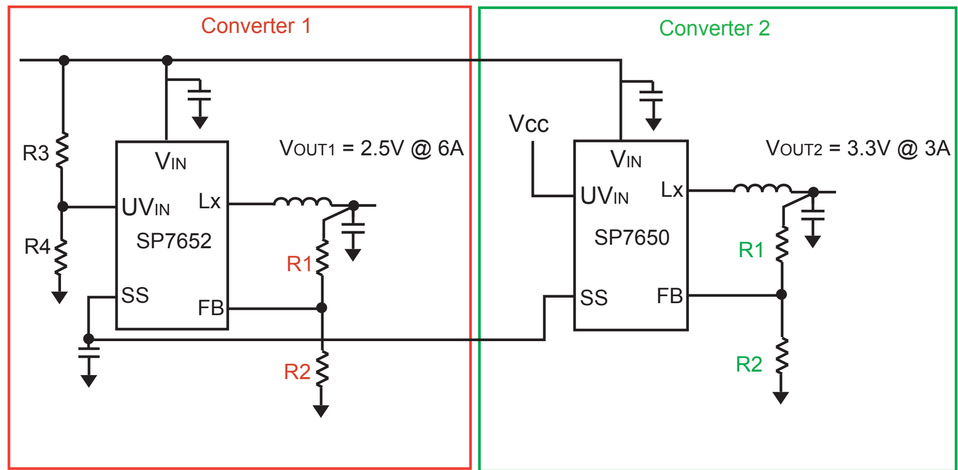

Ratiometric Power-up

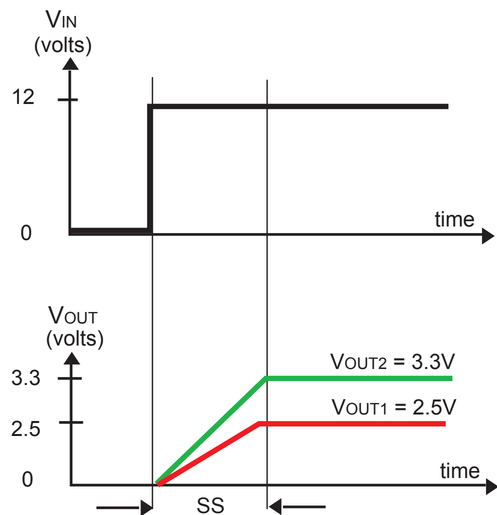

Figure 4. Ratiometric Power-up Using PowerBlox™

2. Ratiometric Power-Up

The second type of start-up is the ratiometric method: The two supplies are turned on simultaneously, reaching regulation at their respective set-points at the same time. In this method, the two rails are controlled with different slew rates, so that the two different voltages are realized at the same time. Figure 4 shows how to implement ratiometric power up simply by tying the soft start pins together.

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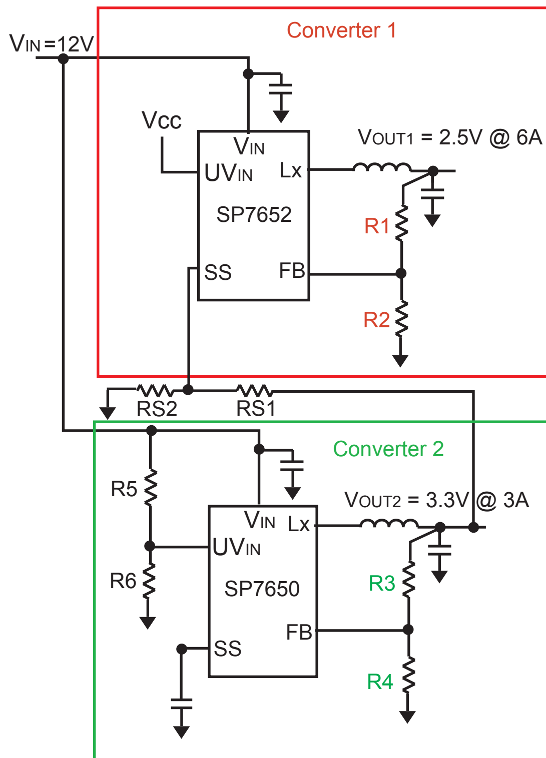

Simultaneous Power-up

$$RS1 = \frac{R1}{R2} \bullet RS2$$

Where R1 and R2 are the output voltage setpoint resistors for the lower output voltage supply.

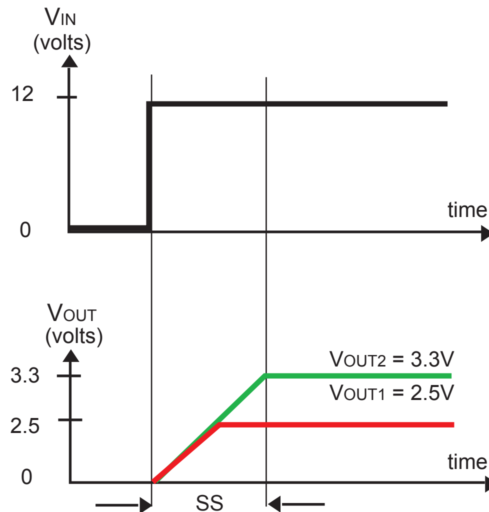

Figure 5. Simultaneous Power-up Using PowerBlox™

3. Simultaneous (Output Tracking) Power-up
The simultaneous power-up sequence is the third approach to power sequencing. Both the rails start up simultaneously and rise at the same slew rate. As a result, the lower voltage rail reaches regulation first, and the higher rail reaches regulation later. In order to implement simultaneous power-up using PowerBlox™, the output of the converter with the higher output voltage is tied through a resistor divider to the soft start of the other converter. The formula for calculating the resistor divider values is shown along with the application diagram in Figure 5. Note that RS2 should be set to 8kΩ.

Thus, the soft start and UVIN pins can be used in various configurations to provide simultaneous, sequential or ratiometric power up as required by the system. This eliminates the use of sequencing control ICs and MOSFETs on the output of each rail, simplifying system design and reducing costs at the same time.

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Application Note ANP 15

Voltage Mode Control: The Modulator in Continuous Current Mode (CCM) of operation

There are three main components in the control loop of a voltage mode DC to DC converter. The three stages are the output stage consisting of the output filter, the modulator gain, and the voltage loop compensation. The two topologies for generating a PWM signal are fixed ramp voltage and feed forward voltage topology both of which will be discussed in this document. The issue of how the modulator gain stage affects the stability of the voltage mode open loop system and closed loop system in continuous current mode (CCM) will also be discussed.

1. Basics of operation and definitions

The actual PWM signal in a voltage mode regulator is generated by a comparator triggering on a voltage ramp as shown in diagram 1. This ramp is generated from a clock signal and it can be fixed to a particular peak voltage or it can be variable depending on V_{in} as in the feed forward topology.

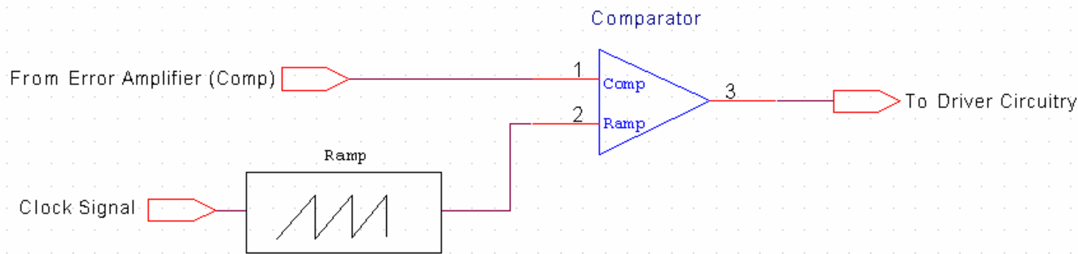

Diagram 1

When the error amplifier input (V_{comp}) is 0 V the duty cycle is 0% meaning the part is off. When the error amplifier voltage (V_{comp}) is equal to peak of the ramp voltage (V_{ramp}) the driver circuitry is at 100% duty cycle.

The duty cycle of the controller is defined as $D=t_{on}/T$ where T is the Total time defined with respect to the comp voltage and the ramp voltage.

$$D = \frac{ton}{T} \quad (1)$$

t_{on} time = V_{comp}
t_{off} time = V_{ramp}-V_{comp}
T= t_{on}+t_{off}

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This results in equation 2 by substituting t_{on} and T into the duty cycle equation 1

$$D = \frac{Vcomp}{Vcomp + Vramp - Vcomp} = \frac{Vcomp}{Vramp} \qquad (2)$$

It is important to note that these definitions could vary from controller to controller depending on what the driver logic is but for the SP613X family and the PowerBlox family of products the above definitions hold true.

The gain of the modulator is defined as

$$Gain = \frac{\partial V_{out}}{\partial V_{comp}} \qquad (3)$$

In the feed forward topology another definition is needed. In a feed forward topology the ramp voltage is no longer fixed but varies depending on what the input voltage is. The V_{ramp} signal can go full input voltage range or in many instances it is clamped to a maximum voltage. For example the SP612X family of products has a K (gain) of 5 with a maximum ramp voltage of 3V. Thus up to 15V in the IC has feed forward above that voltage it becomes a fixed ramp voltage of 3V.

$$V_{ramp} = \frac{V_{in}}{K} \qquad (4)$$

Where K is a constant

The feed forward topology has advantages over a fixed ramp voltage topology which will be further examined after the Modulator Gains are defined. The constant can be any number chosen at the time of the initial IC definition.

2. The Buck regulator topology

The buck regulator is one of the most common topologies used. It is well known how the output voltage is related to Input voltage in equation 5.

$$V_{out} = V_{in} \cdot D \qquad (5)$$

D is the Duty Cycle

Substituting Equation 2 into Equation 5

$$V_{out} = V_{in} \cdot \frac{V_{comp}}{V_{ramp}} \qquad (6)$$

To get the gain we need to take the derivative of equation 6 with respect to V_{comp}.

$$Gain = \frac{V_{in}}{V_{ramp}} \qquad (7)$$

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For a modulator with feed forward another step is needed to get the proper gain, equation 4 needs to be substituted into equation 7. The result for feed forward modulator gain of the buck converter is

$$Gain_{feedforward} = \frac{V_{in}}{\frac{1}{K} \cdot V_{in}} = K \qquad (8)$$

3. Boost Regulator

Another widely used topology is the Boost regulator. This topology will be investigated here in some detail since it is a little more complicated than the buck regulator. Once the boost regulator gain is solved, all of the other topologies can be derived in the same manner. The boost regulator V_{in} to V_{out} relationship is a follows:

$$V_{out} = V_{in} \cdot \frac{1}{1-D} \qquad (9)$$

Substituting equation 2 in for duty cycle in equation 9 we get

$$V_{out} = V_{in} \cdot \frac{1}{1-D} = V_{in} \cdot \frac{1}{1-\frac{V_{comp}}{V_{ramp}}} = \frac{V_{in} \cdot V_{ramp}}{\left[V_{ramp} - V_{comp}\right]} \qquad (10)$$

The next step is to take the derivative of equation 10 we get the following results:

$$Gain = \frac{\partial Vout}{\partial Vcomp} = \frac{V_{in} \cdot V_{ramp}}{\left[V_{ramp} - V_{comp}\right]^2} \qquad (11)$$

Substitute equation 2 after solving for V_{comp} into equation 11

$$Gain = \frac{V_{in} \cdot V_{ramp}}{\left[V_{ramp} - D \cdot V_{ramp}\right]^2} = \frac{V_{in}}{V_{ramp} \cdot (1-D)^2} \qquad (12)$$

For a feed forward topology substitute equation 4 into 12.

$$Gain_{feedforward} = \frac{K}{\left[1-D\right]^2} \qquad (13)$$

4. The Topologies summarized

Table 1 shows more voltage mode modulator gain values for different topologies. These were derived the same way as the steps outlined previously in this document. The modulator gains are for continuous conduction current mode (CCM).

TABLE 1

Topology	Duty Cycle Relationship	Modulator Gain Fixed Ramp	Modulator Gain Feed forward
Buck	$V_{out} = V_{in} \cdot D$	$\frac{V_{in}}{V_{ramp}}$	K
Boost	$V_{out} = V_{in} \cdot \frac{1}{1-D}$	$\frac{V_{in}}{V_{ramp} \cdot (1-D)^2}$	$\frac{K}{[1-D]^2}$
Negative Buck Boost	$-V_{out} = V_{in} \cdot \frac{D}{1-D}$	$\frac{V_{in}}{V_{ramp}} \cdot \frac{1}{(1-D)^2}$	$\frac{K}{[1-D]^2}$
SEPIC*	$V_{out} = V_{in} \cdot \frac{D}{1-D}$	$\frac{V_{in}}{V_{ramp}} \cdot \frac{1}{(1-D)^2}$	$\frac{K}{[1-D]^2}$
Cuk*	$V_{out} = -V_{in} \cdot \frac{D}{1-D}$	$\frac{V_{in}}{V_{ramp}} \cdot \frac{1}{(1-D)^2}$	$\frac{K}{[1-D]^2}$

5. Effects on the compensation for a Buck Regulator

To see what effect the modulator has on the output filter one has to look at the open loop Bode plot for the topology. Diagram 2 is the typical open loop filter and modulator Bode plot for a buck regulator. The modulator gain and the filter gain are added together to get the total open loop gain for the filter. The important thing to note is that in a fixed ramp topology, as Vin increases so does the total gain of the open loop filter. This in turn pushes out the crossover frequency of the filter which in turn affects the positioning of the poles and zeros of the compensation network. This problem does not exist when the gain of the modulator is fixed as it is in the feed forward topology.

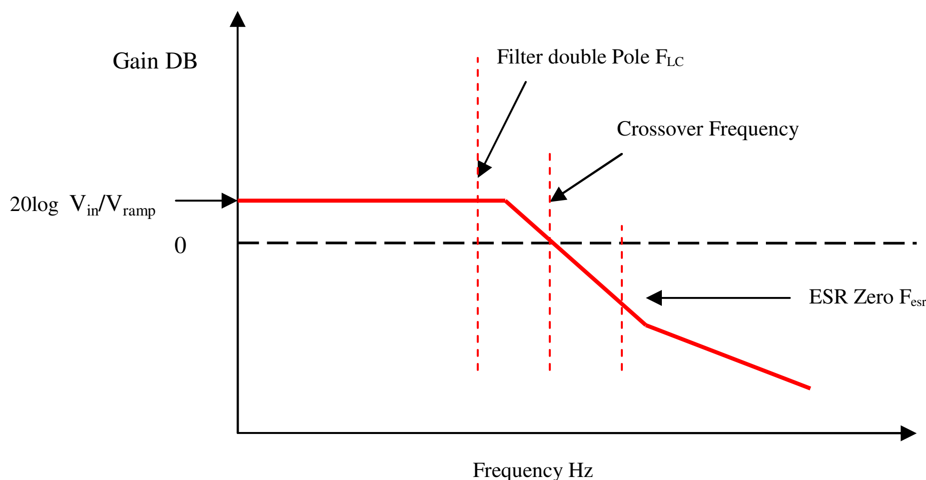

Diagram 2 Open Loop Filter Bode Plot

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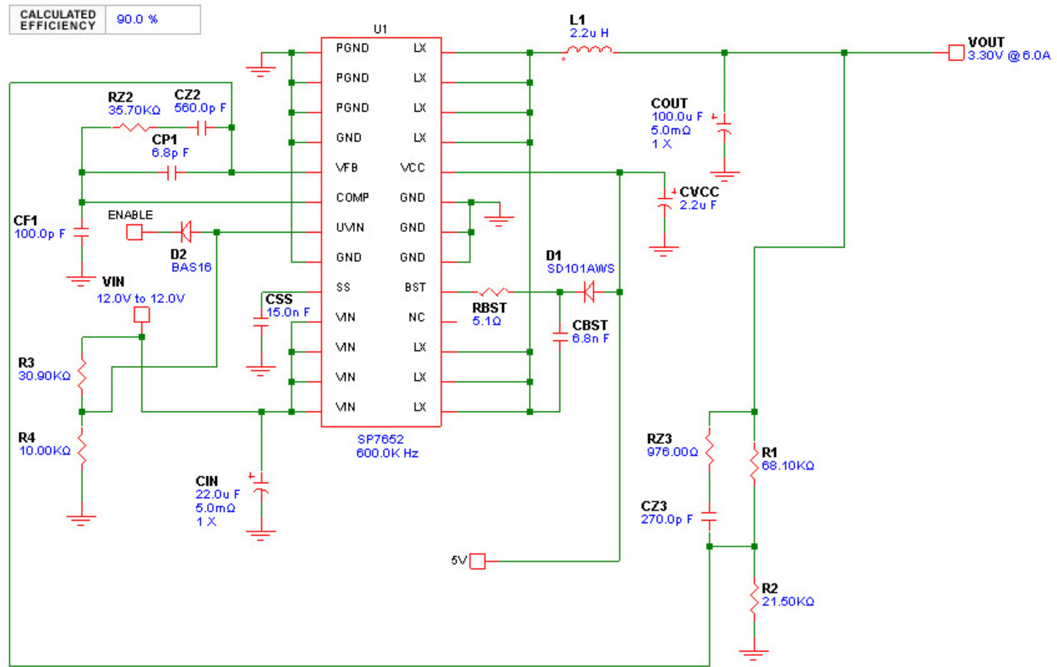

Diagram 3 Schematic for AC Analysis Simulations

In diagrams 4 5 and 6 we have Bode plots for phase and gain for a compensation network for a fixed ramp voltage regulator. The compensation was not altered between different simulations for the different input voltages. The compensation was designed for a 12V input.

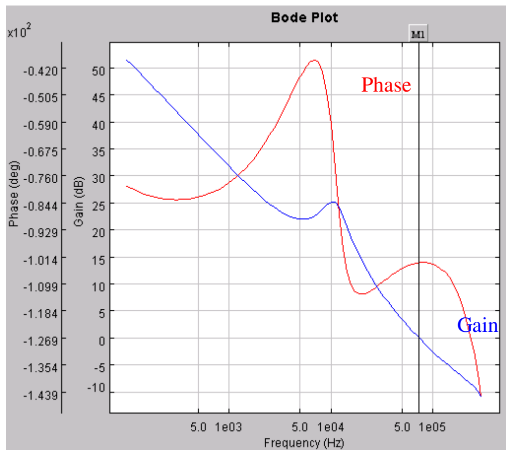

Diagram 4: V_{in} = 12V,
Crossover frequency = 73 KHz

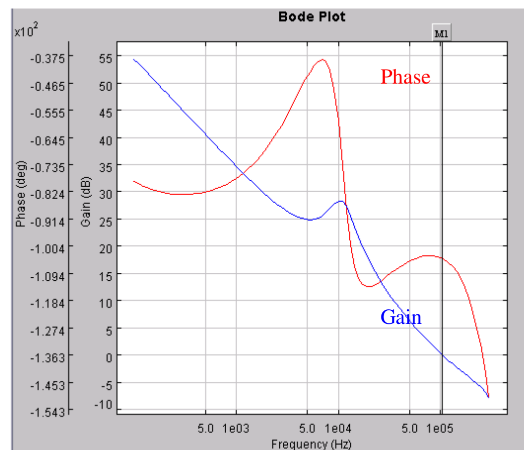

Diagram 5: V_{in} = 16V,
Crossover frequency = 100 KHz

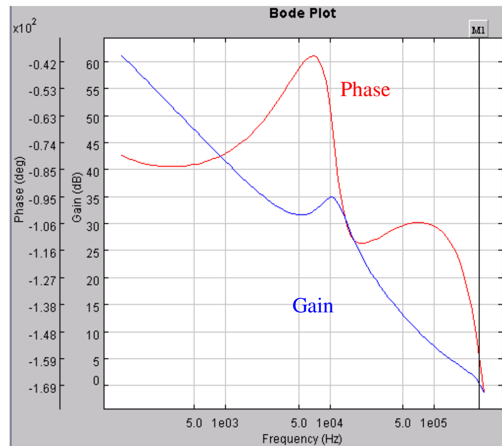

Diagram 6: V_{in} = 28V
Crossover frequency = 200 KHz

As can be clearly seen from diagrams 4, 5 and 6 as the input voltage increases so does the gain of the modulator. This in turn increases the crossover frequency. There are two well known effects on compensation when the crossover frequency increases but the compensation network does not change.

1. The first is that the crossover frequency should be no more than 1/2 of the switching frequency. This is dictated by the Sampling Theorem to try to avoid aliasing. Typically in a design 1/5 or 1/10 of the switching frequency is used as a crossover frequency. In diagram 4 it can be seen that the crossover frequency is 200KHz at 28V in.

2. The second one is that the phase margin will deteriorate as the crossover frequency increases, which will affect the stability of the converter, as can be seen Diagram 4. This is because the poles and zeros were set for a different crossover frequency to give phase boost in a certain frequency range to have proper phase margin. As the crossover frequency increases the phase will eventually decrease which will make the converter unstable.

This V_{in} gain issue is negated in the feed forward topology since the Gain is a constant K.

6. How to compensate a buck with large input voltage swings without feed forward

In the feed forward topology this is not as much of a problem, but in a fixed ramp topology to get good stable compensation with a large input voltage swing the designer needs to consider how the modulator affects the overall gain of the system. In a buck regulator this means that the compensation design needs to be done at the highest V_{in} since this will give the designer the highest gain. This gain should be the one used to set the crossover frequency. This approach will guarantee that the regulator will be stable over the whole input range. The drawback of this is that as V_{in} decreases, so will the crossover frequency, thus degrading the transient response. This will be most noticeable when the input voltage range is rather large.

7. Modulator Effects on the open loop Bode plot of a Boost Regulator

The boost converter is a lot more complicated when it comes to compensation and the effects of the modulator on the open loop gain. The problem is that the duty cycle has a big effect on both the filter and the modulator. The effect on the modulator is the same as in the buck regulator Bode plot, the modulator and output filter responses are added together. In Diagram 7a and 7b are graphs showing the modulator Gain with respect to the duty cycle for a boost regulator for specific input voltages.

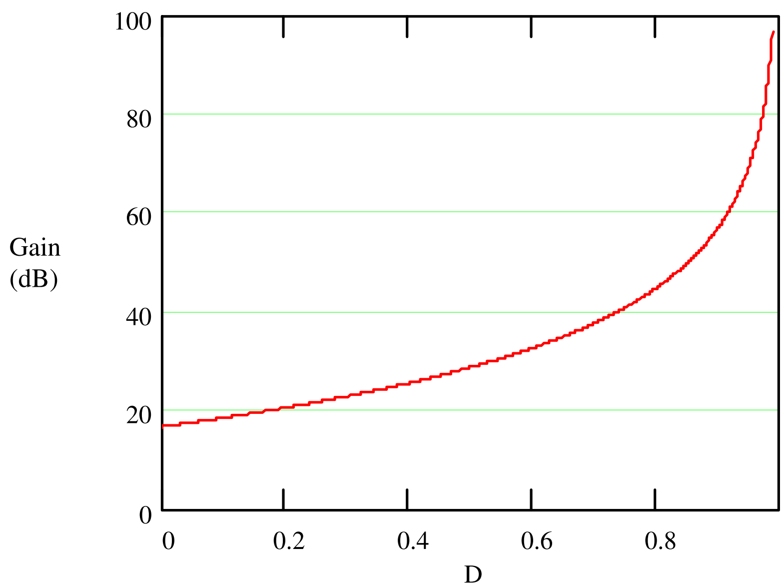

Diagram 7a Modulator gain for V_{in} of 7V and V_{ramp} 1V (From Table 1)

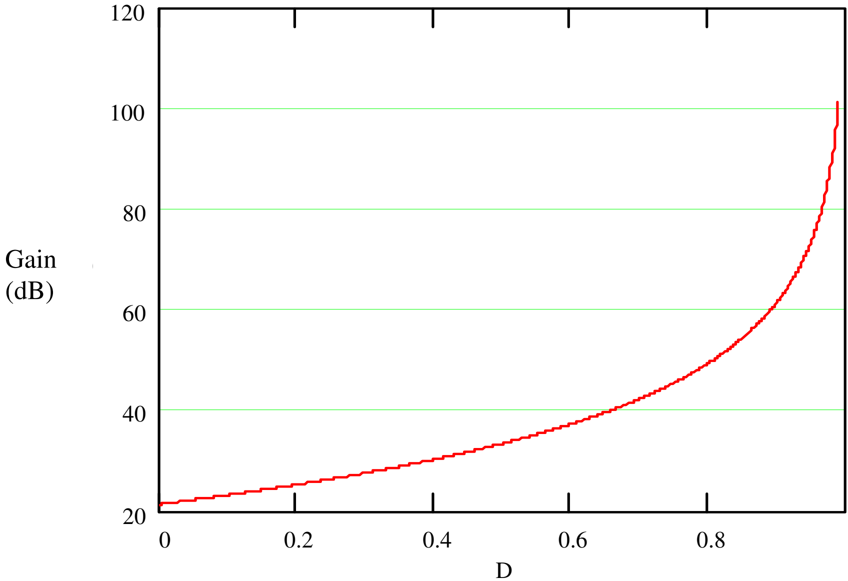

Diagram 7b Modulator gain for V_{in} of 12V and V_{ramp} 1V (From Table 1)

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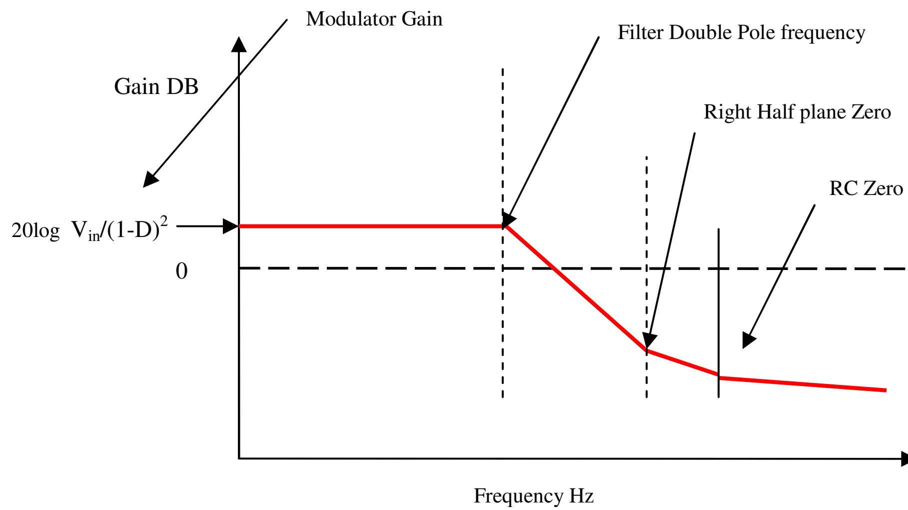

Diagram 8 Open Loop Transfer Function
of a boost converter in CCM mode

Filter Double Pole $$\omega_{LC} = \frac{1-D}{\sqrt{L \cdot C_{out}}}$$

RC zero $$\omega_{RC} = \frac{1}{ESR \cdot C_{out}}$$

Right Half Plane Zero $$\omega_{RHP} = \frac{(1-D)^2 \cdot R_L}{L}$$

Modulator Gain $$M_{db} = \frac{Vin}{(1-D)^2}$$

‘

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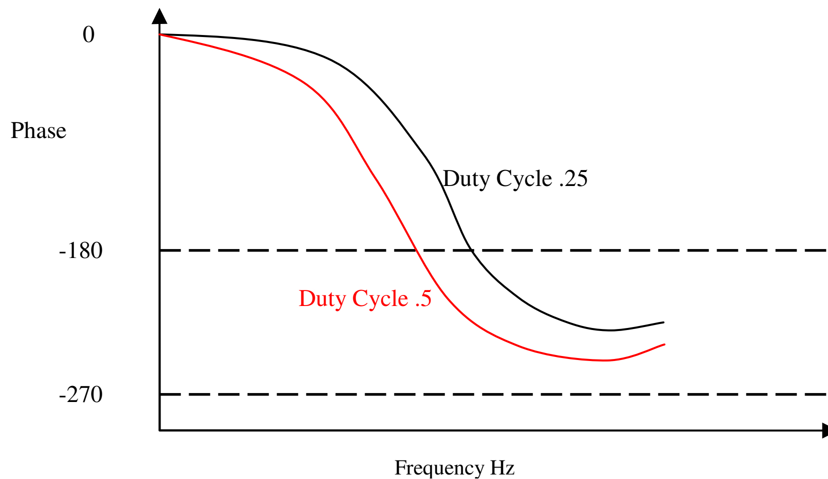

Diagram 9 Phase of a boost regulator

As can be seen from diagrams 7 and 8 and 9, it is not that straightforward when it comes to compensation of a boost. The generic Bode plot of a boost converter in Diagram 8 clearly states that the duty cycle plays an important role in defining the open loop gain.

As to the gain of the modulator it can significantly differ depending on the duty cycle, for V_{in} of 12V, at 25% duty cycle the gain of the modulator is about 25dB; at 75% percent duty cycle it is about 45dB. Another major thing to consider is that the modulator will have a gain that is approaching infinity as the duty cycle approaches 100%. The other complication is that the gain curve exists for every input voltage of the boost regulator, thus complicating the design even more. Usually as input voltage changes, so will the duty cycle of the design thus creating more variables to deal with. One saving grace is that for a fixed output the duty cycle decreases as the input voltage increases, which tends to help keep the modulator gain in check. This can be seen clearly seen from equation 14 and diagrams 7a and b.

$$D = 1 - \frac{V_{in}}{V_{out}} \qquad (14)$$

When a feed forward topology is implemented, the design can be greatly simplified by having one modulator gain curve for a specific voltage range and thus only having to deal with the variations of the duty cycle on the analysis. (Table 1)

8. Compensating the Boost Converter

Unlike the buck converter it is much harder to compensate the boost converter for wide input voltage swing when the output voltage is fixed, since changes in V_{in} will affect the duty cycle of the converter. This type of topology typically is better suited to running in narrower duty cycle ranges with compensation that is not very aggressive. To properly compensate the regulator the

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designer needs to make sure that the crossover frequency for his system occurs before the Right Half Plane Zero (RHP_{zero}) at a slope of -20dB. It is the right half plane zero that contributes to a sharp decline in phase approaching -270 degrees as seen in diagram 9. The obvious problem there is that the location of the RHP_{zero} varies with duty cycle and load. Although this can be discussed in more depth, the focus of this paper is on the modulator effects on the Bode plots. Thus unlike the buck compensation, it needs to be considered earlier in the design since the best results are when the duty cycle variation is limited to small changes around the 50% duty cycle point. At this point is where the gain of the modulator is at its most linear with changes in gain of 10 to 20db either way from 50% duty cycle point.

9. Summary

The modulator gain has a significant effect on the total open loop gain of the Bode plots. It is also one of the least talked about topics in control loop theory. Hopefully this paper helped the reader understand a small but crucial part of the compensation network.

10. Bibliography

1) Fred C. Lee, A CPES Professional Short Course at Virginia Tech Lecture Note,© 2005

2) Wu. Keng C. Pulse Width Modulated DC-DC Converters. New York: Chapman & Hall, 1997.

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APPLICATION NOTE ANP25

PowerBlox^{TM} Thermal Analysis

Introduction

The primary factor limiting how much current a PowerBlox^{TM} device can deliver is heat. Heat is generated by losses in the PowerBlox^{TM} package and comes from four main sources: conduction Losses in the FETs, switching losses in the FETs and FET drivers, losses in the internal LDO, and losses in the controller required to run the power supply. Another loss that can be significant is the power lost in the output inductor DCR. The ability of the PowerBlox^{TM} devices to dissipate heat will be closely examined in this report.

Description of Testing Completed

Three PowerBlox^{TM} configurations were tested:

A) SP7662 on a 4 layer PCB with a layout having components on one side
B) SP7662 on a 4 layer PCB with a layout having components on two sides
C) SP7655 on a 4 layer PCB with a layout having components on two sides and an increased via count

Each power supply was configured for 12Vin and 3.3Vout. An airflow chamber that could provide temperature regulated laminar airflow was used to create consistent test conditions. Each unit was monitored using an Infrared Thermal camera to record temperature levels and thermal images. The power input, output, and dissipation was measured for a variety of conditions to create power derating curves for each device. While this is useful for the particular input/output/inductor configuration, a more generic power dissipation derating curve was created that will serve as a guideline to any PowerBlox^{TM} application.

Comparison of PCBs Used

The construction of each PCB is the same, standard FR4 type material. All traces on inner and outer layers are 2 ounce copper. All the PCBs will be examined in greater detail within the report.

<u>PCB A:</u> Single Sided – No Vias. This 4 layer PCB is the SP766x evaluation board for customers wanting a solution having components only on one side. Adding no thermal vias also means the PCB uses the minimum of board space on the back side.
<u>PCB B:</u> Double Sided – Multiple Vias. This 4 layer board is the SP7662 standard evaluation board. This PCB has a total of 28 vias under the part. It also has larger areas of copper for the PowerBlox^{TM} to sink heat into. The layout places components on the top and bottom side.
<u>PCB C:</u> Double Sided – Maximum Vias. This 4 layer board is the SP7655 standard evaluation board. It is similar to 'B' but has numerous vias throughout all of the main copper areas of Vin, Vout, Ground, and the inductor pads. This further increases the heat sinking capability of the PCB. The layout places components on the top and bottom side.

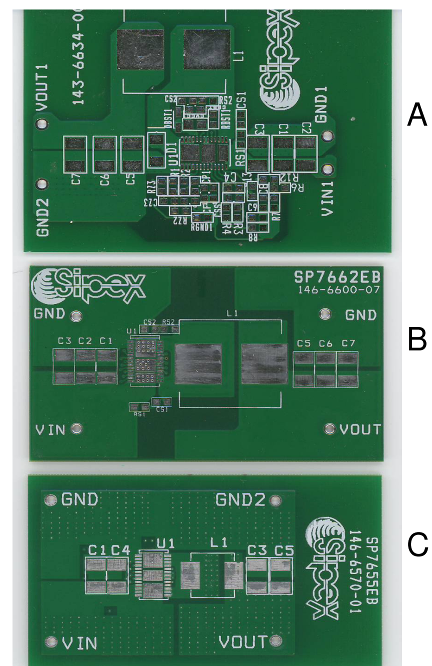

Figure 1

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Methodology

Data was collected using derating equipment and methods common to the DC-DC converter module industry shown in Figures 3 and 4. Each board was mounted in the airflow chamber so that the airflow is across the PCB from Vin to GND. In the case of the single layer board where the inductor placement would interfere more with the airflow over the device, both directions were compared.

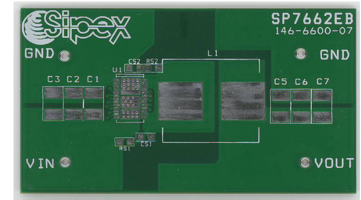
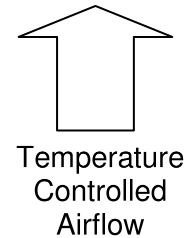


Figure 2



Temperature Controlled Airflow

Air temperature was regulated and airflow was laminar across the PCB surface. The PCB was also in the physical orientation shown here with air flowing from the floor to the ceiling and airflow, hitting the edge of the PCB across the device.

Temperatures were taken using a thermal imaging camera – FLIR Model A20, from FLIR Systems. Component temperature was recorded using the readout from the camera. Emmisivity was set for optimal temperature measurement of the PowerBlox^{TM} part. Due to the small thermal impedance between the device case and the device junction, the temperature displayed by the camera was recorded as the device junction temperature. Derating of the device was done by limiting the hottest spot on the PowerBlox^{TM} to 120˚C. At output power levels beyond ~5 Watts, the device MOSFETs would measure as the hottest areas – leaving the controller 10 or more degrees cooler than the FET. This provides further margin in the derating of the part as the controller junction is rated to 125˚C and the MOSFETs are junction-rated to 150˚C.

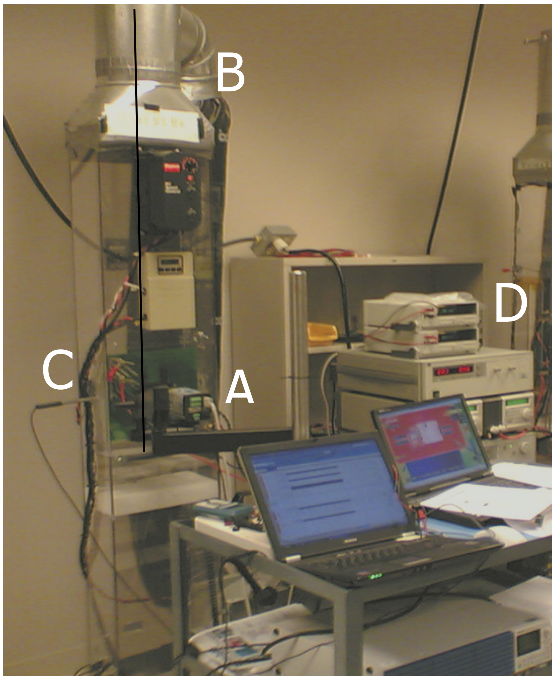


Figure 3 – Chamber Set-up

A - Thermal Camera
B - Laminar Airflow Chamber
C - Airflow Meter
D - Source and Loads
E - Device Under Test

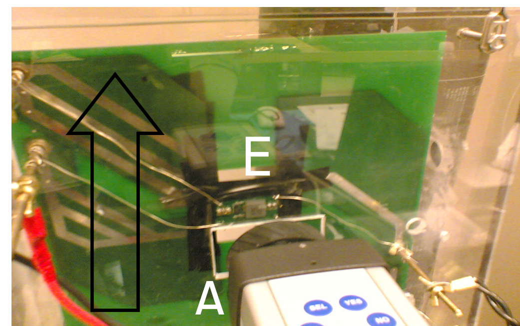


Figure 4
DUT and Infrared Camera – arrow showing airflow direction.
Eval board is mounted to a larger test fixture but is not soldered to the fixture.
No additional heat sinking was added to the eval board.

Understanding the Thermal Images

A description of the temperature measurements and plots are shown in Figure 5 and 6.

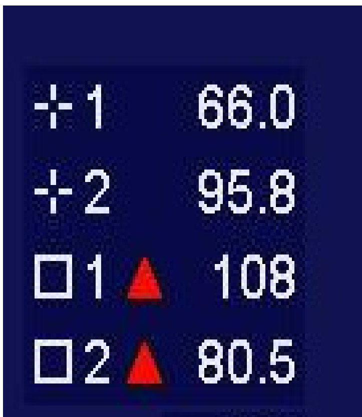


Figure 5

Camera Readings:

+1 - The temperature measured at the center of cursor cross hair 1

+2 - The temperature measured at the center of cursor cross hair 2 (Typically the low-side FET)

☐1∆ -The hottest temperature measured in BOX 1 (Typically the high-side FET)

☐2∆ - The hottest temperature measured in BOX 2 A cursor is not shown indicating the hottest spot as in Box 1 (This is the inductor core material temperature)

Sample Image:

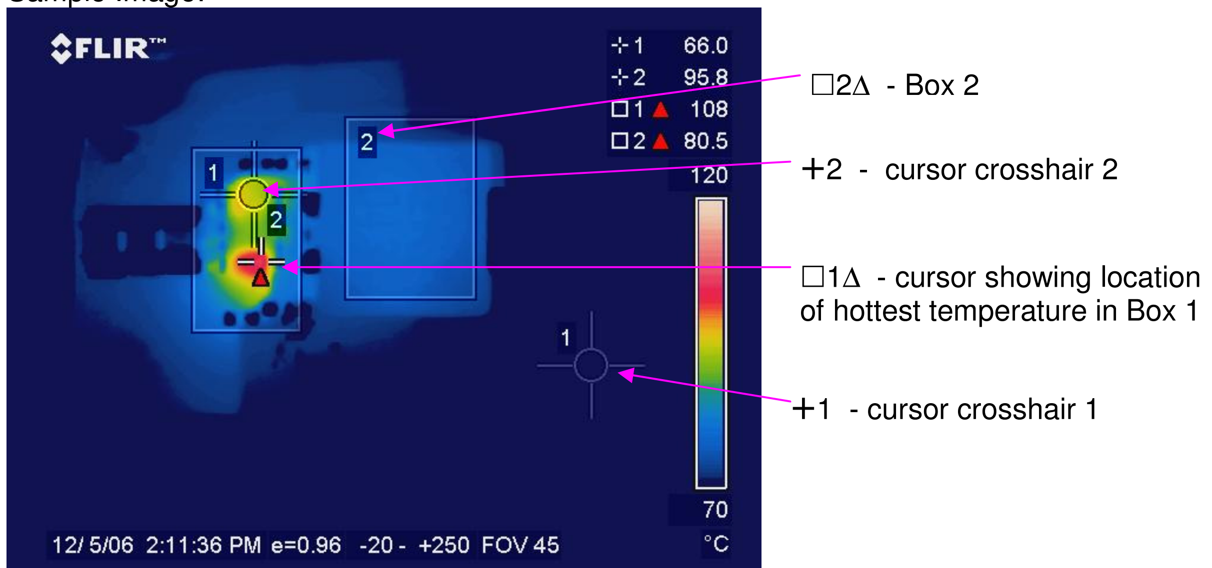
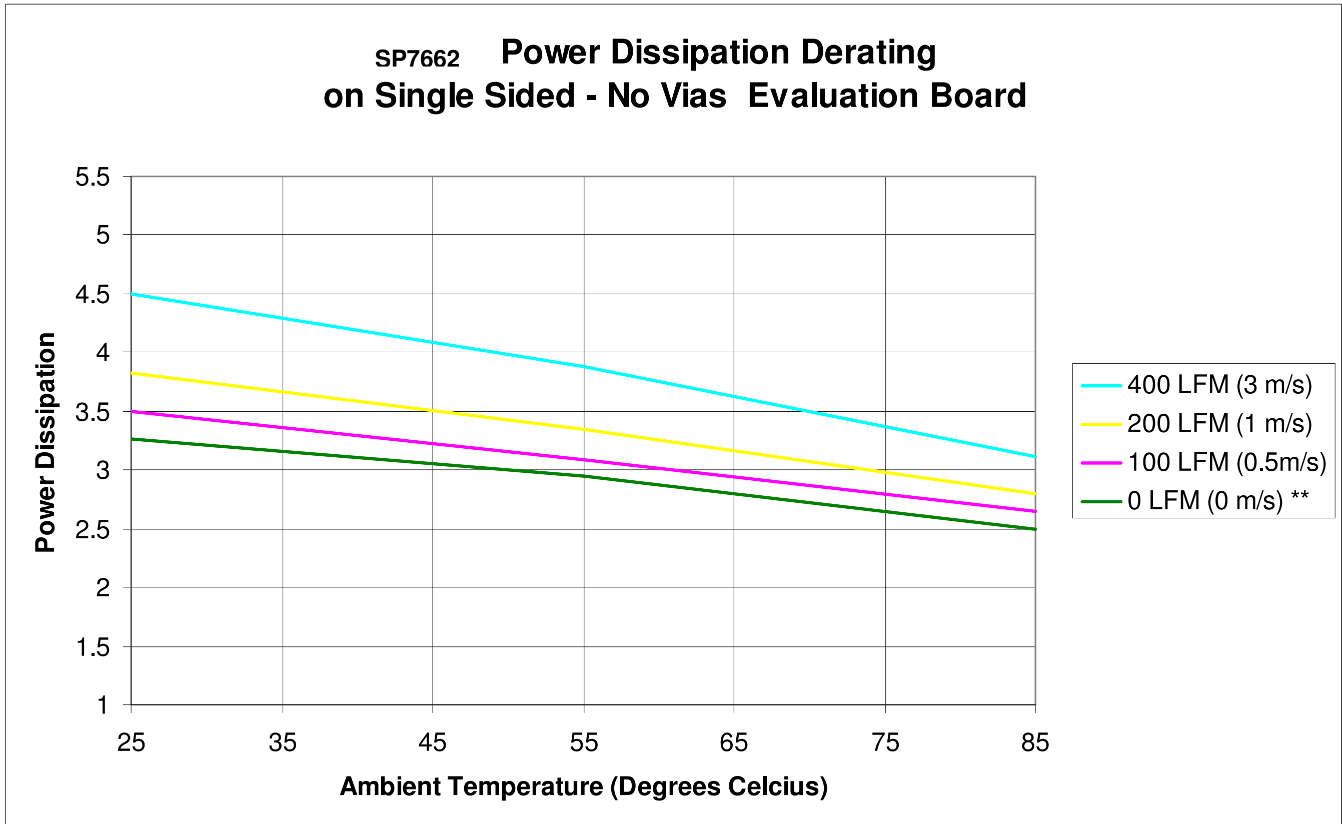
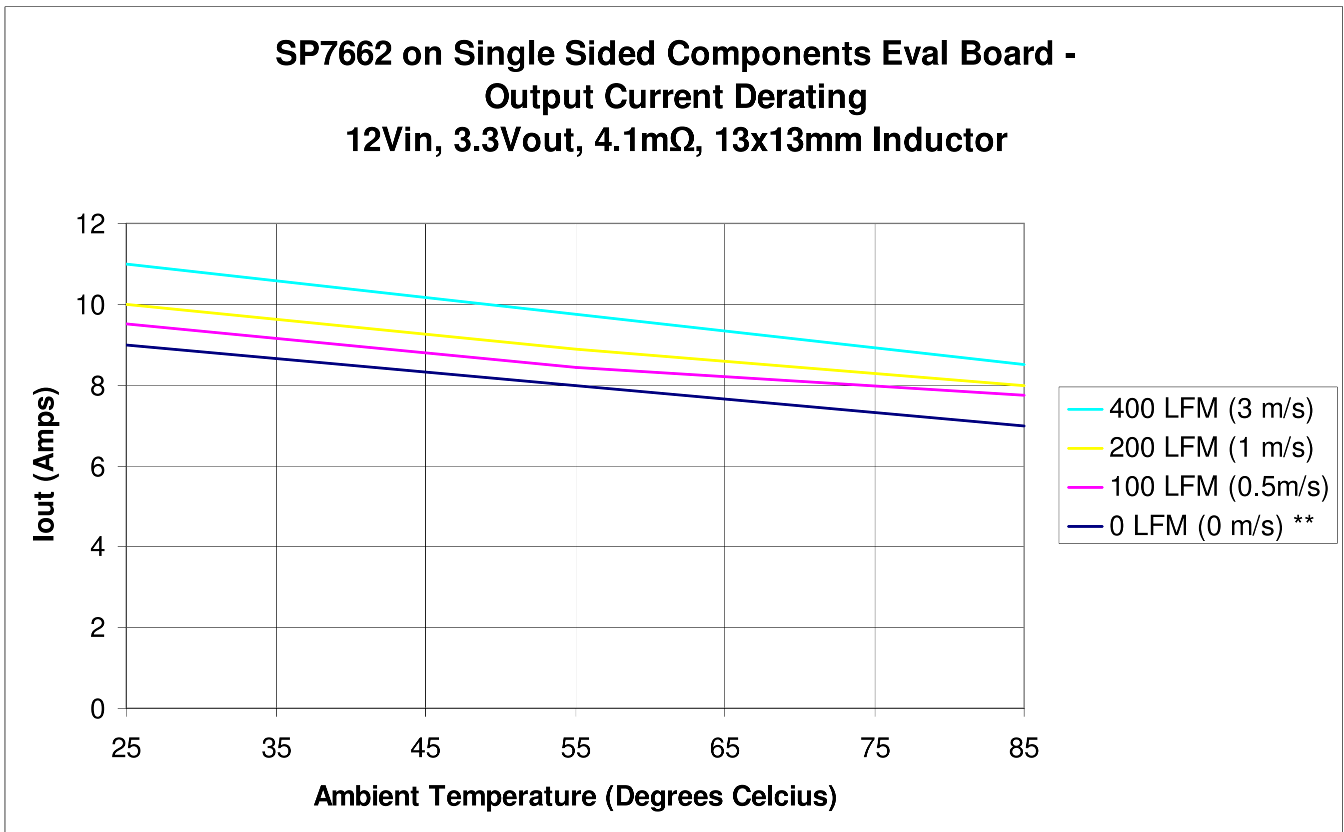


Figure 6

Results: PCB A – Single Sided Components – No Vias – Derating / SOA





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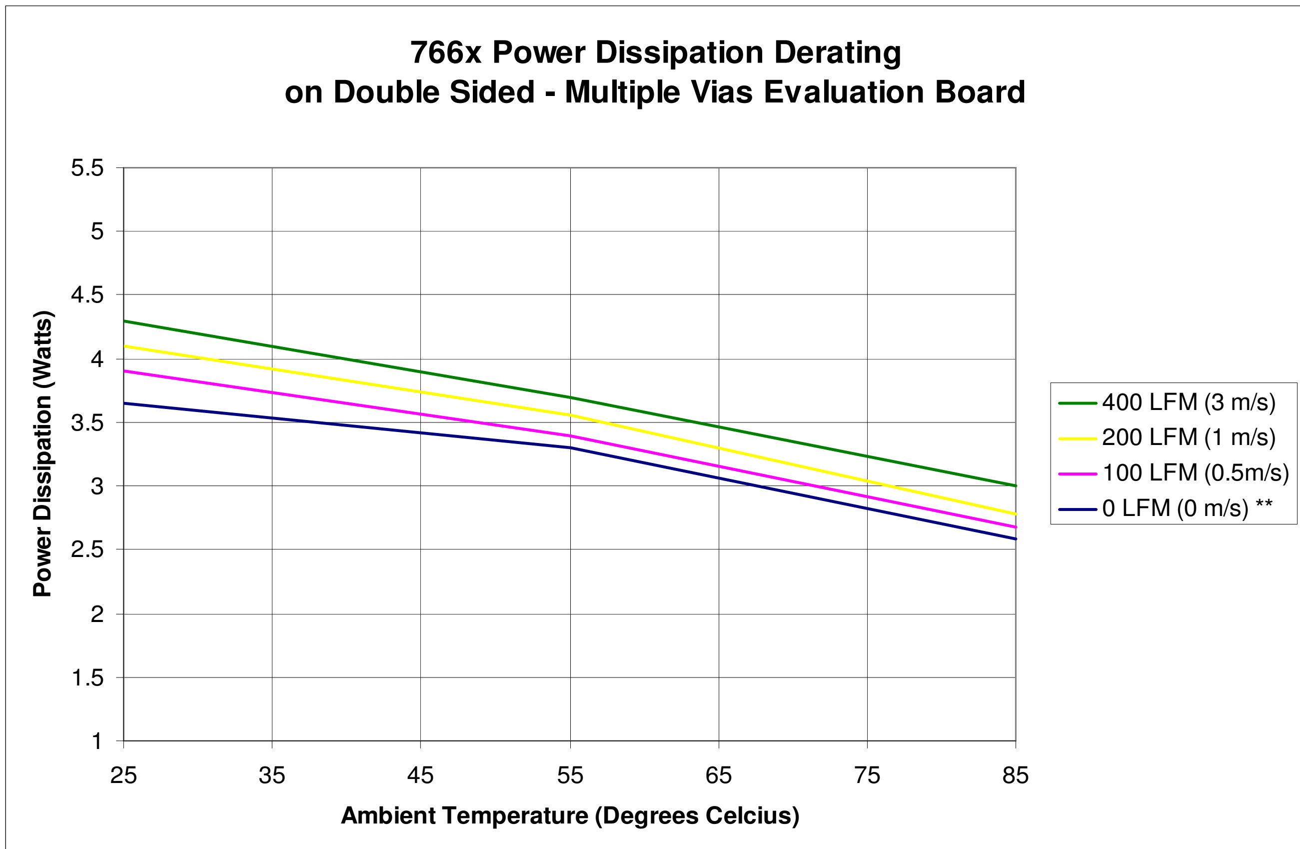
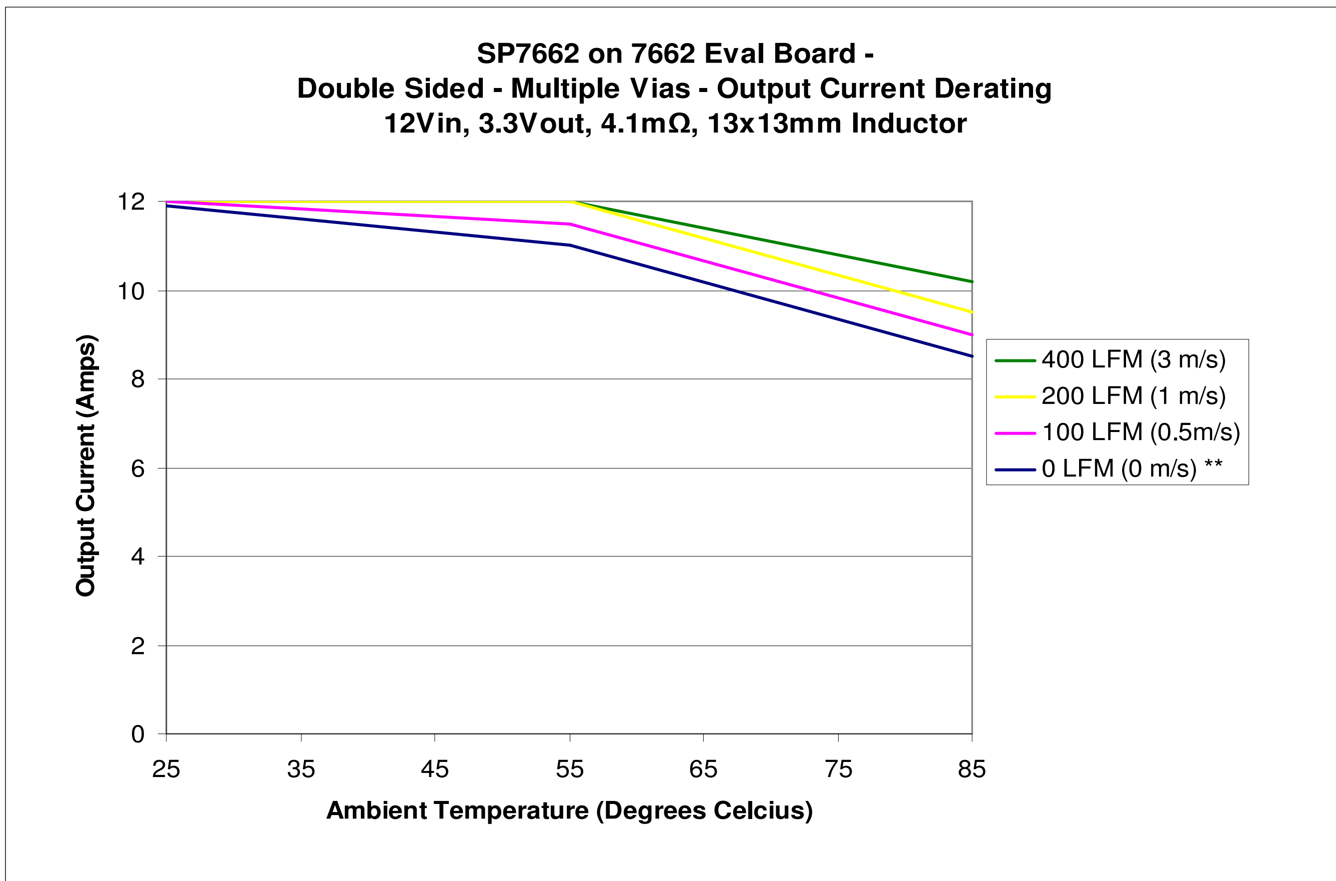
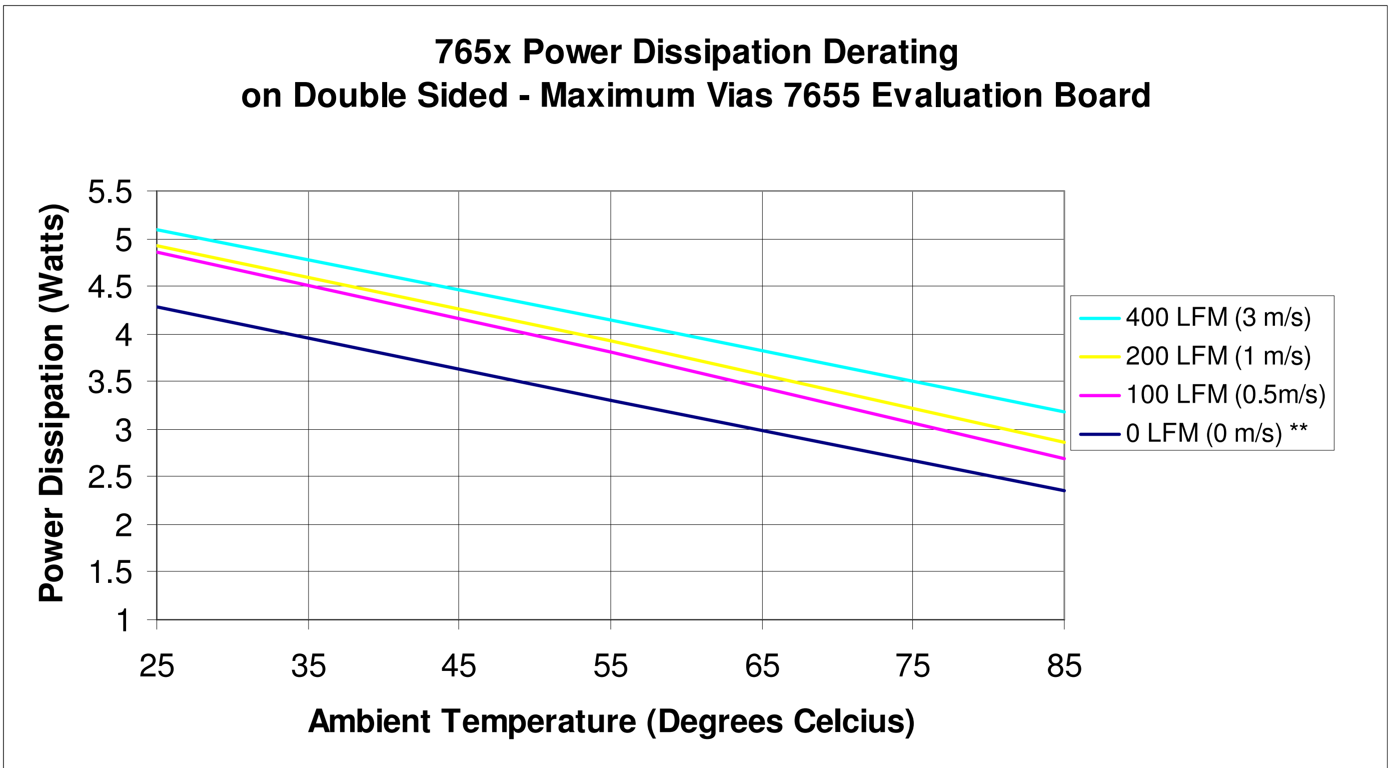
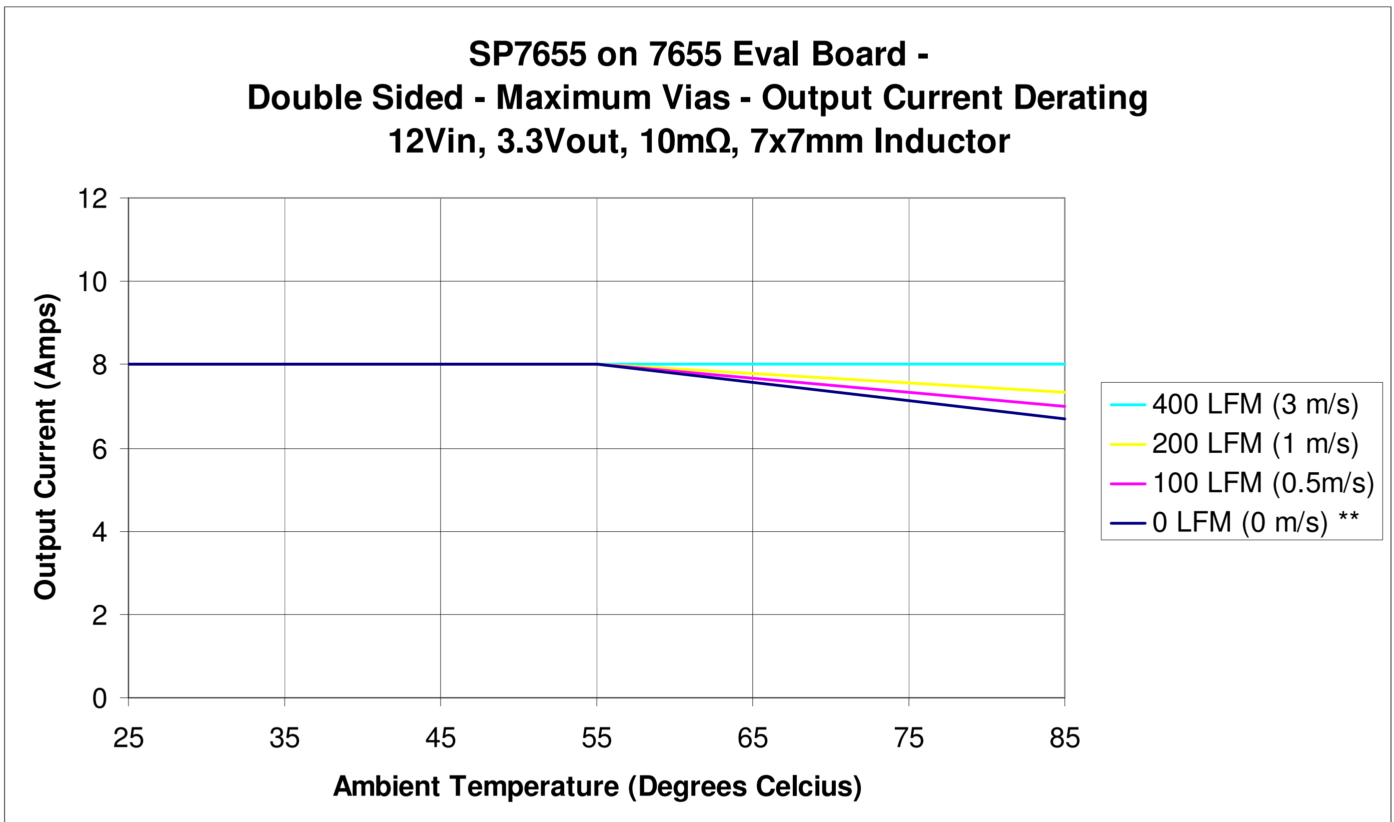
Results: PCB B - Double Sided Components – Multiple Vias PCB – Derating / SOA





Results: PCB C - Double Sided Components - Maximum Vias – Derating / SOA





Note: 7655 Maximum Output Current is 8Amps

Power Dissipation vs. Temperature Results Analysis

In general the achievable power dissipation for all PCBs, SP7662, and SP7655 devices was similar. The highest achievable power dissipation was measured on the SP7655 PCB with maximum vias and 400lfm (linear feet per minute) of airflow at 25˚C at approximately 5Watts. The following chart summarizes the results:

Power Dissipation (Watts)	0lfm	400lfm
25 Degrees		
PCB A– Single Sided 766x – No Vias	3.3	4.5
PCB B– Double Side 7662 – Multiple Vias	3.7	4.3
PCB C– 7655 Eval Board – Maximum Vias	4.3	5.1
85 Degrees		
PCB A– Single Sided 766x – No Vias	2.5	3.1
PCB B– Double Side 7662 – Multiple Vias	2.6	3
PCB C– 7655 Eval Board – Maximum Vias	2.4	3.2

* lfm – linear feet per minute

All three boards at 0 lfm and 85˚C are generally similar, we can basically call them the same. This was also true at 85˚C and 400lfm. A larger difference shows up at 25˚C and 0 lfm where there is a greater delta between the component surfaces and the air temperature. Under this condition, any paths for heat transfer are fully utilized and the effects of more copper attached to the device can be seen. When 400lfm of airflow is added, the A and B boards perform similarly, and again the board with more vias has the greater cooling ability. Also in PCB A the PowerBlox™ is in a rotated orientation and has a more open layout compared to the other boards. Airflow across the device is less restricted and would account for the slightly better performance at 400lfm than PCB B.

The straight current derating of each supply is summarized below and can be used for the individual supplies and as a guideline.

Maximum Output, 12Vin, 3.3Vout	0lfm	400lfm
25 Degrees		
PCB A– Single Sided 766x – No Vias	9	11
PCB B– Double Side 7662 – Multiple Vias	12	12
PCB C– 7655 Eval Board – Maximum Vias	8 (max limit)	8 (max limit)
85 Degrees		
PCB A– Single Sided 766x – No Vias	7	8.5
PCB B– Double Side 7662 – Multiple Vias	8.5	10
PCB C– 7655 Eval Board – Maximum Vias	6.7	8

Note that each supply will have a different efficiency for a given output current, and hence a difference power dissipation. Also, the SP7655 supply used a smaller 7x7mm inductor which gives it a disadvantage compared to the other eval boards. The smaller package and higher DCR caused the part to generate significantly more heat. As will be shown in the thermal images of the SP7655 supply, the inductor runs very hot compared to the 13x13mm inductors and makes the performance worse by heating the SP7655 part.

Results Comparison

A ‘Power Dissipation Derating Curve’ was generated for each system to act as a guideline for various PowerBlox^{TM} solutions operating in various conditions. The versatility of the PowerBlox^{TM} parts in end applications makes a more general approach to its characterization necessary. The following is an example comparing the tested results.

Using the SP7662 Standard Evaluation Board - PCB B – and the same derating fixture and set-up - a 20Vin, 1.8Vout supply was tested. The power dissipation figures are checked against our new data on a few points. The supply used a 13x13mm, 3.5mΩ inductor, but of a lower profile than the previous 3 test examples. The 9% duty ratio versus the previous 27.5% duty ratio, and the higher Vin which will demand more of the internal LDO, introduces a very different operating condition for the supply.

* Note that in all calculations of PowerBlox^{TM} power dissipation the power dissipation of the inductor DCR is subtracted from the overall power dissipation of the converter to obtain the power dissipation of the PowerBlox^{TM}.

Example:
Condition 1: 0 lfm, 25 degrees, SP7662 on 7662 multiple vias eval board (PCB B)
Condition 2: 100lfm, 85 degrees, SP7662 on 7662 multiple vias eval board (PCB B)

	Vin (volts)	Vout (volts)	Efficiency	**Power Blox Pdiss**	**Quoted Pdiss Limit for 120˚C Case Max**	**Peak Case Temperature Measurement**
Condition 1	20	1.8	83.44%	**2.82 Watts**	**3.7 Watts**	**86.5˚C**
Condition 2	20	1.8	82.89%	**2.00 Watts**	**2.68 Watts**	**100˚C**

When less than recommended power was dissipated in the device, we can see the temperature of the device was lower than 120˚C.

Unfortunately the requirements for this test were a maximum case temperature of 100˚C so we can not test the full 120˚C limit of our results, however it still shows the figures are good. In condition 2 the supply is dissipating 0.68Watts less power than the recommended maximum and it is 20 degrees cooler.

Summary

The versatility of the PowerBlox^{TM} family means that power supplies can be created with a very large number of variations in Input Voltage, Output Voltage, Output Inductor value and package size, as well as Layout. All of these factors influence the thermal performance of the device. To use an Output-Current-only Derating curve and apply it to any PowerBlox^{TM} solution would be entirely reckless. The Output Current derating curves should be used as a performance guideline for the solutions presented. The Output Power Dissipation Derating is a much better way to predict the thermal performance of any solution.

Derating of devices was done by limiting the hottest spot on the PowerBlox^{TM} to 120˚C. In the case of the SP7662 devices, this spot was always associated with the high side FET. In the case of the SP7655, this spot was always the low side FET. In both cases the controller (the center of the device) was 10 or more degrees cooler then the FET. This provides further margin in the derating of the part as the controller junction is rated to 125˚C and the MOSFETs are junction-rated to 150˚C

Results:

Power Dissipation (Watts)	**0lfm**	**400lfm**
25 Degrees		
PCB A – Single Sided 7662	3.3	4.5
PCB B – Double Side 7662	3.7	4.3
PCB C – 7655 Eval Board w/multiple vias	4.3	5.1

This data can be used to predict a safe operating region for various PowerBlox^{TM} power supplies operating on a variety of PCBs under a variety of input, output, inductor choices, and resulting efficiencies.

For more information on the thermal resistance of the PowerBlox^{TM} you can refer to the application note ANP5 'Thermal Resistance on 765x Devices ' from this link: http://www.sipex.com/applicationNotes.aspx?p=appNotesPower . ANP5 characterizes the PowerBlox^{TM} device on various PCB layouts as a singular device. Keep in mind the results in ANP5 do not include thermal effects of the presence of the output inductor.

APPENDIX

Thermal Scans Airflow is always from the bottom to top of the image
Note: The thermal camera automatically adjusts the scale, colors and temperature minimums and maximums are not always the same.

Layout Plots Layout Design Tip: Copper areas under the Power Blox and Inductor are important and help with device power dissipation even when not electrically connected by vias.

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Results: PCB A – Single Sided, No Vias, 4 Layer PCB

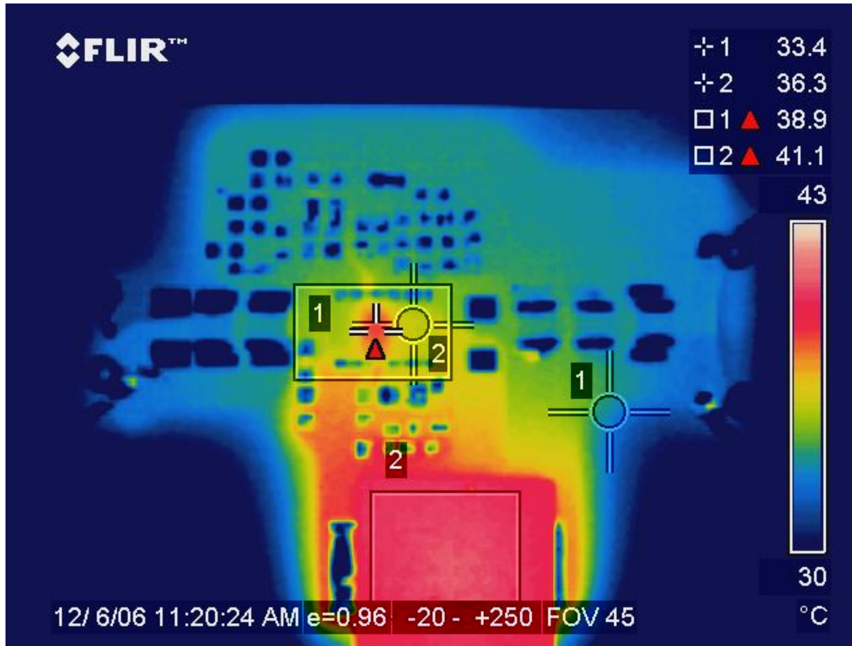

Image 1 – Vin: 12V Iout: 0Amps Ambient Temp: 25˚C Airflow: 0lfm Pdiss: Minimum

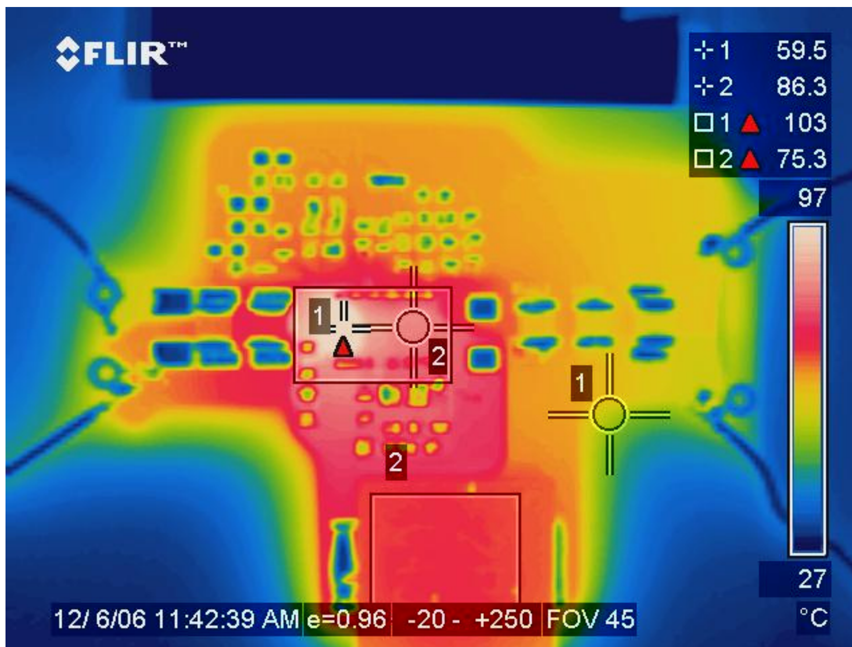

Image 2 – Vin: 12V Iout: 8.0Amps Ambient Temp: 25˚C Airflow: 0lfm Pdiss: 3.1W

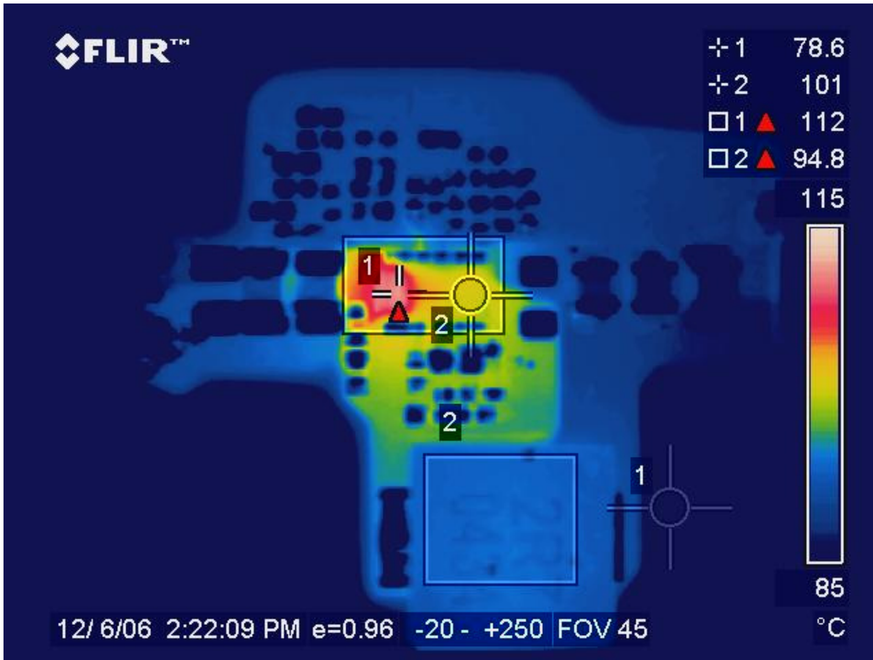

Image 3 – Vin: 12V Iout: 6.75Amps Ambient Temp: 85˚C Airflow: 400lfm Pdiss: 2.48W Orientation #1

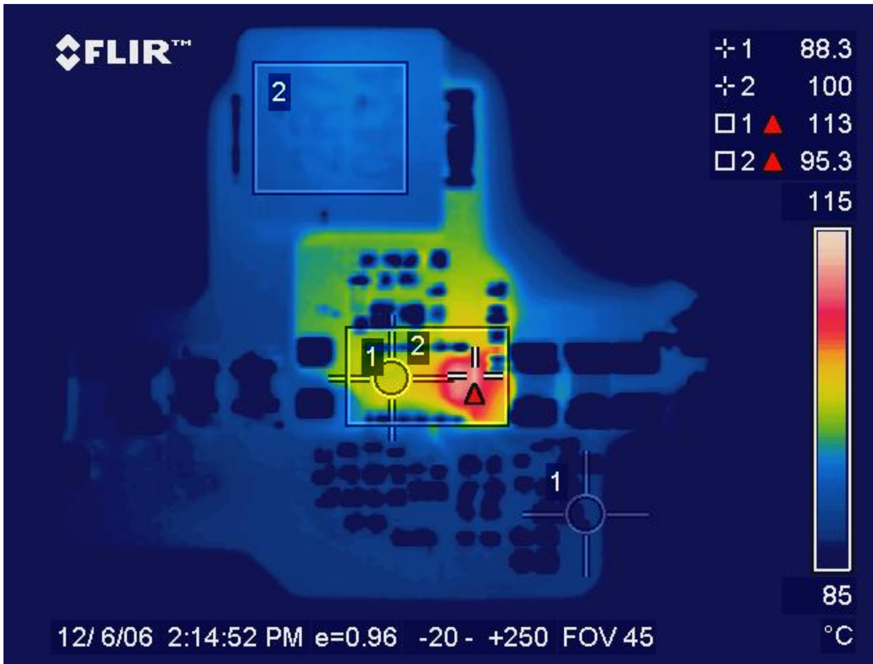

Image 4 – Vin: 12V Iout: 6.75Amps Ambient Temp: 85˚C Airflow: 400lfm Pdiss: 2.48W Orientation #2

Almost no difference is seen in temperature for this example.

Results: PCB B – Double Sided, Multiple Vias, 4 Layer 7662 Evaluation PCB

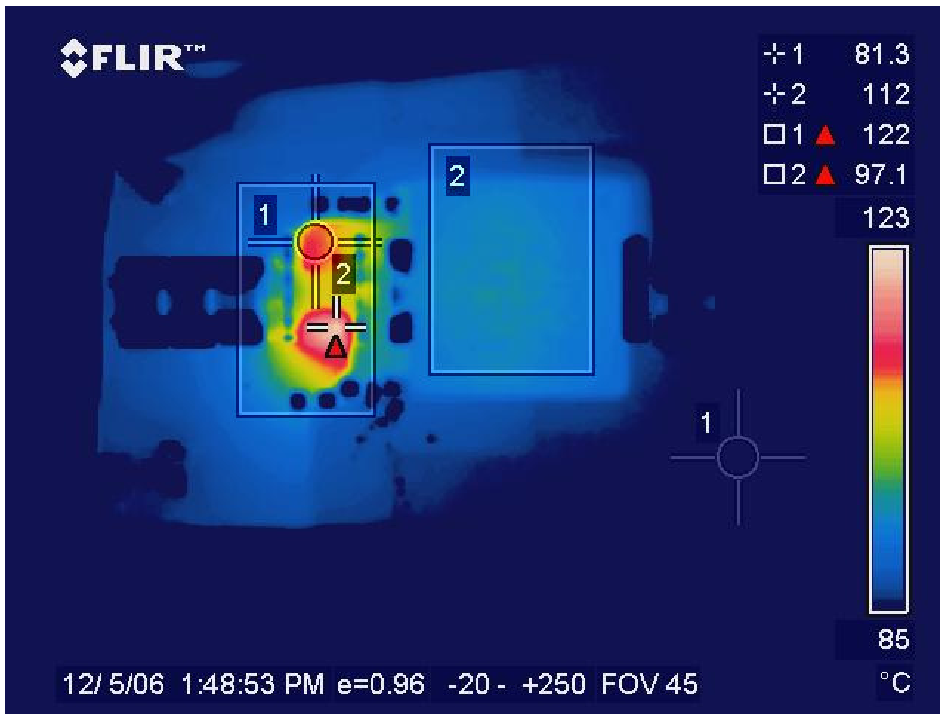

Image 5 – Vin: 12V Iout: 12Amps Ambient Temp: 25˚C Airflow: 0lfm Pdiss: 3.65W

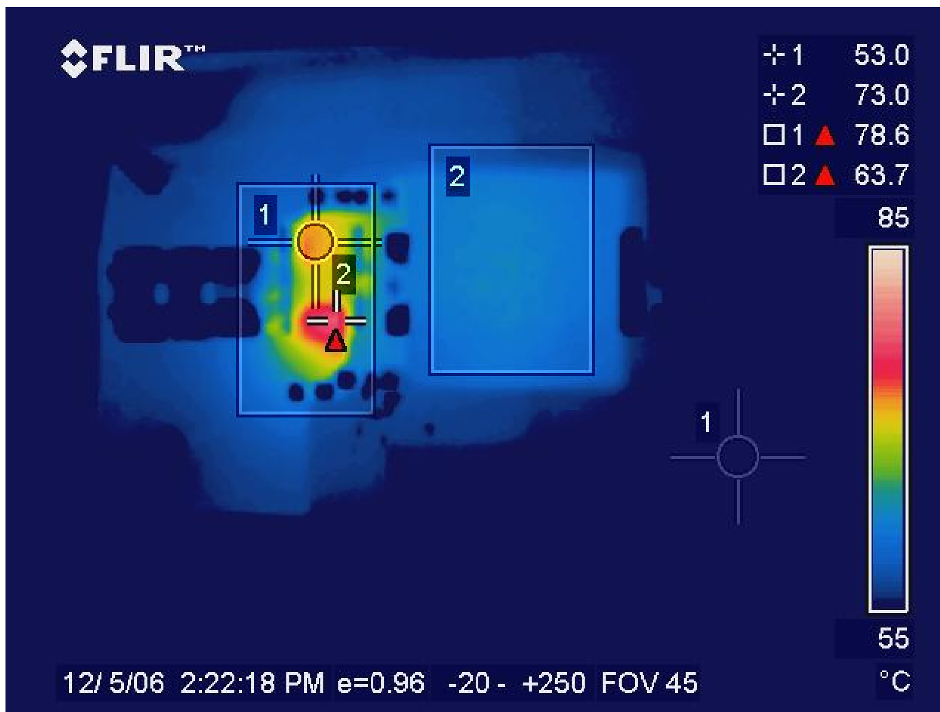

Image 6 – Vin: 12V Iout: 10Amps Ambient Temp: 25˚C Airflow: 100lfm Pdiss: 2.84W

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Results: PCB C – Double Sided, 4 Layer, Maximum vias 7655 Evaluation PCB

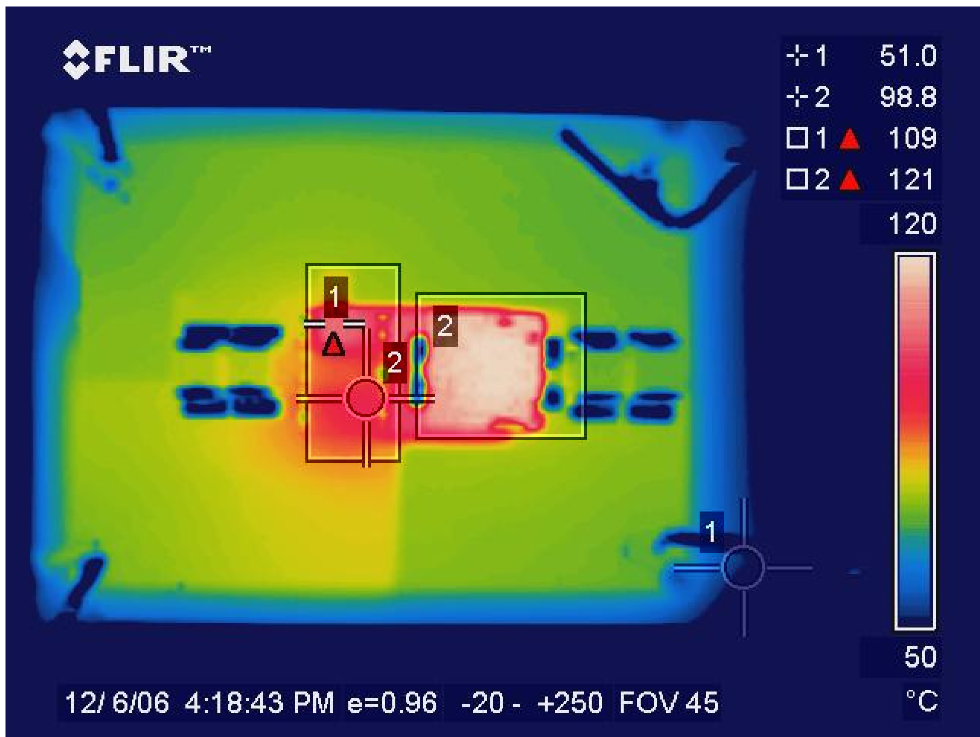


Image 7 – Vin: 12V Iout: 8Amps Ambient Temp: 25˚C Airflow: 0lfm Pdiss: 3.73W

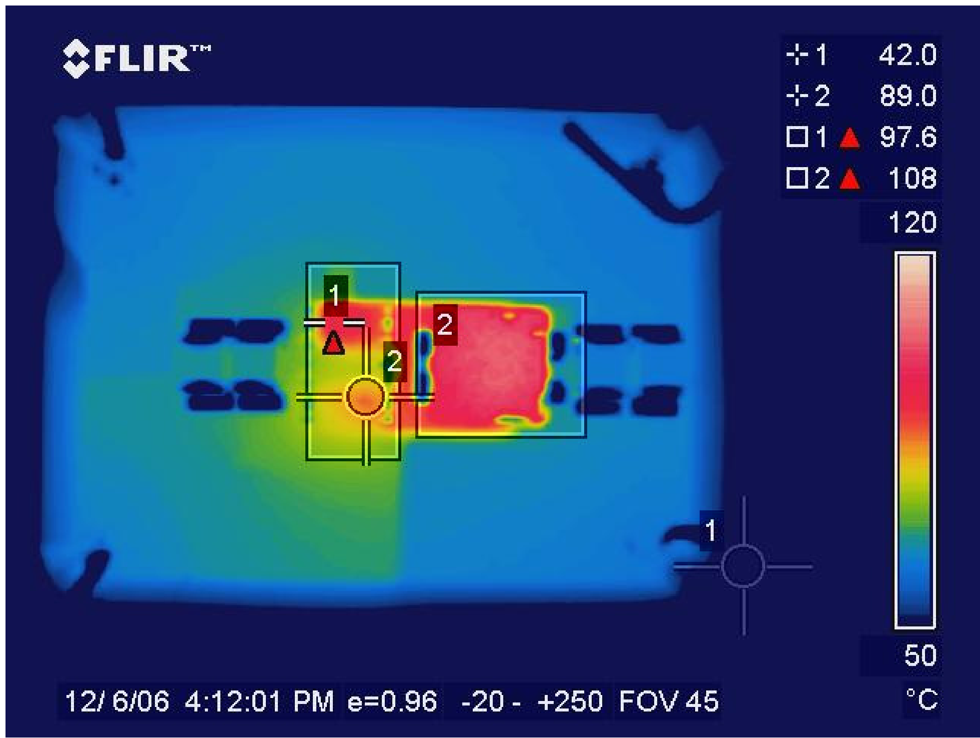
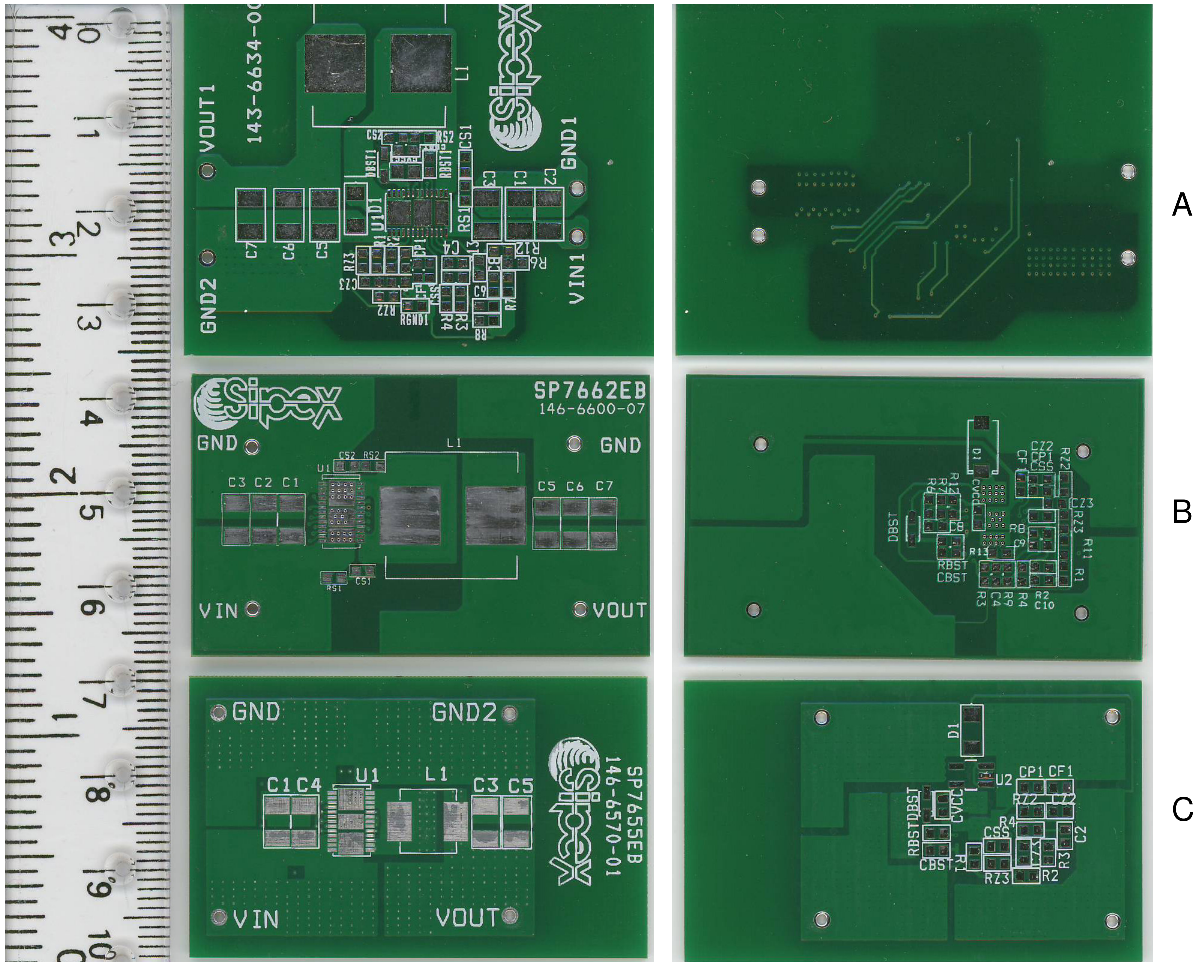


Image 8 – Vin: 12V Iout: 8Amps   Ambient Temp: 25˚C Airflow: 100lfm Pdiss: 3.8W

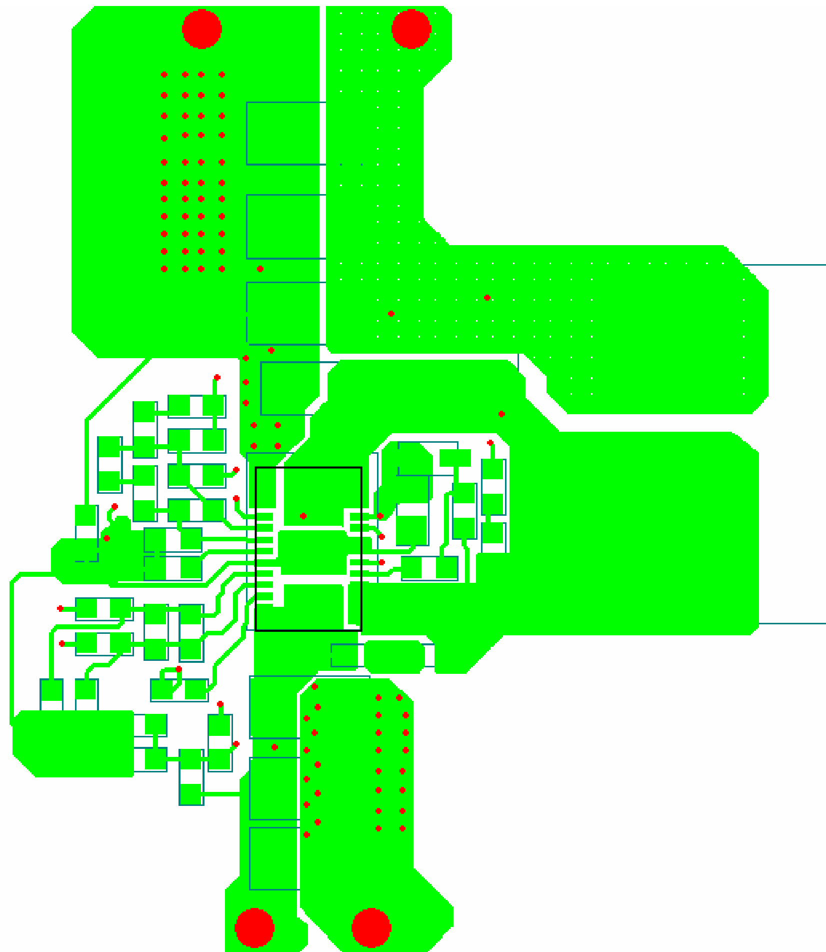
PCB Plots

PCB Image Comparison

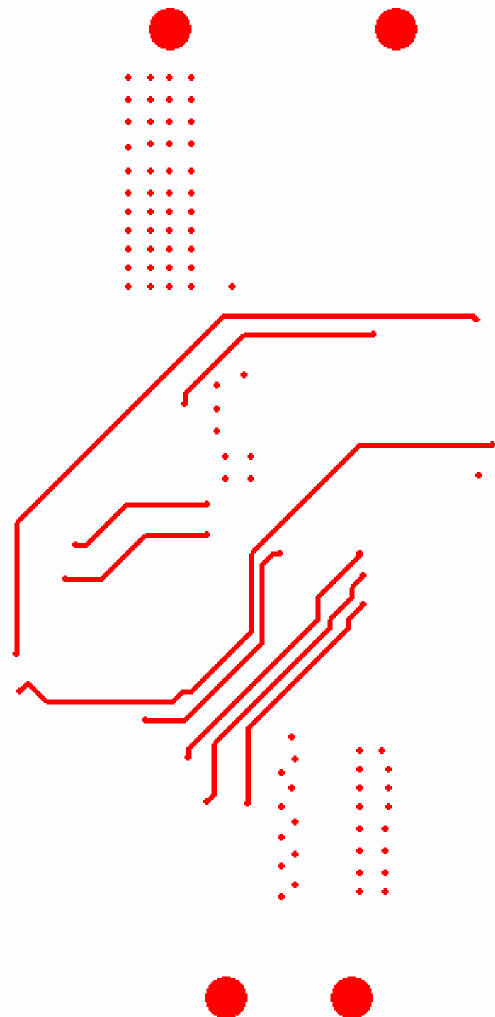
Top Side **Bottom Side**



PCB A – Single Sided Components PCB – 4 Layers



Top side traces and copper areas. Red circles are board vias



Back side

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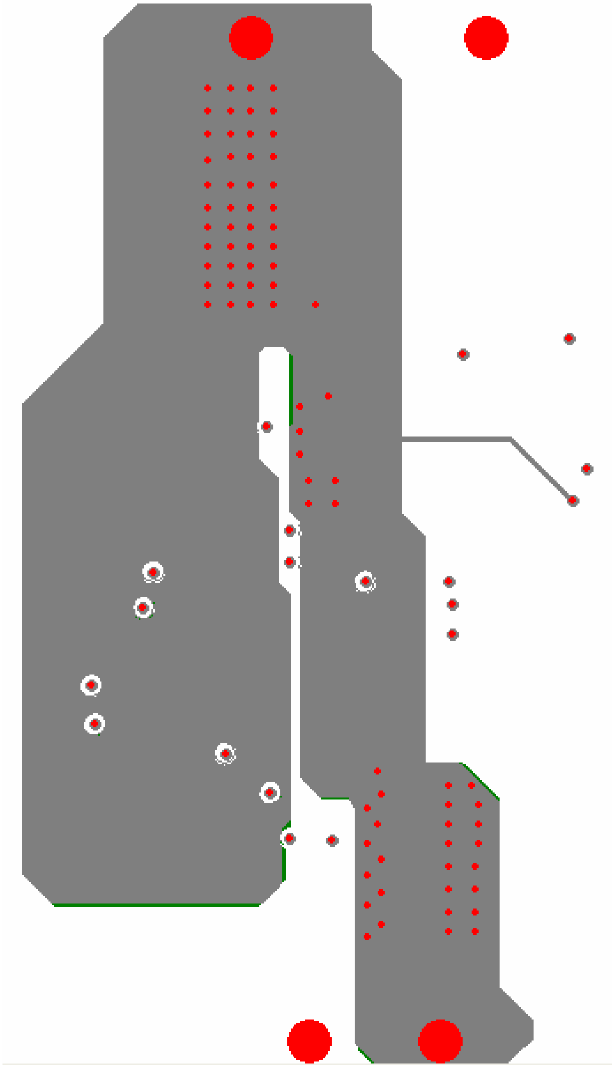
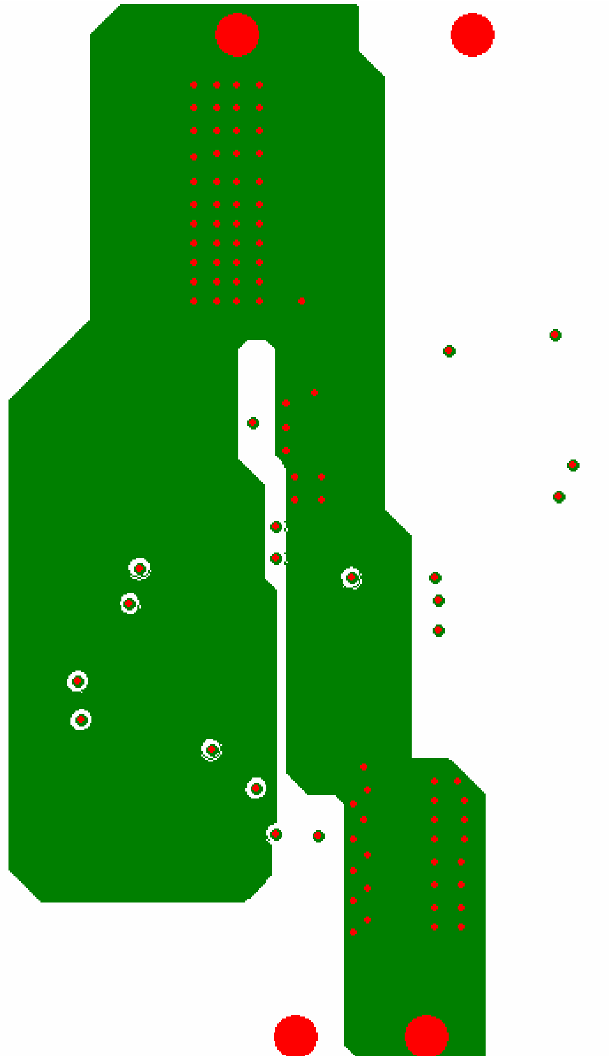
PCB A – Single Sided Components PCB – 4 Layers

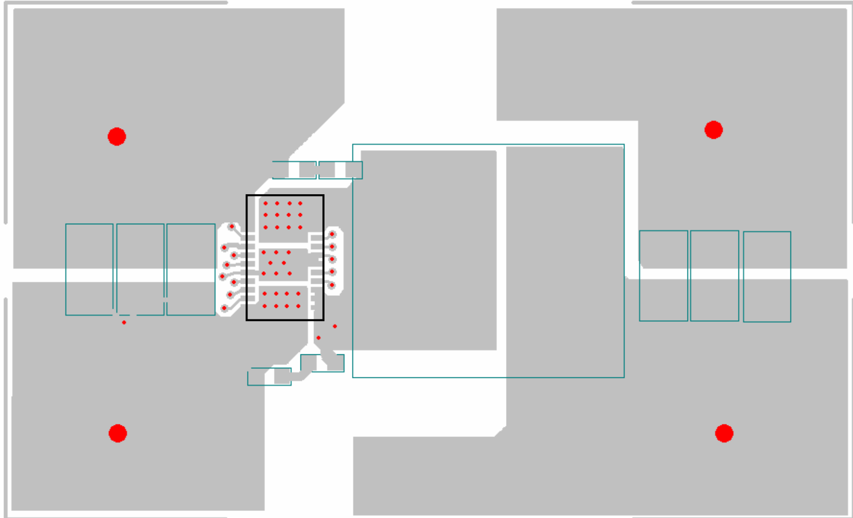


Internal Layer 2

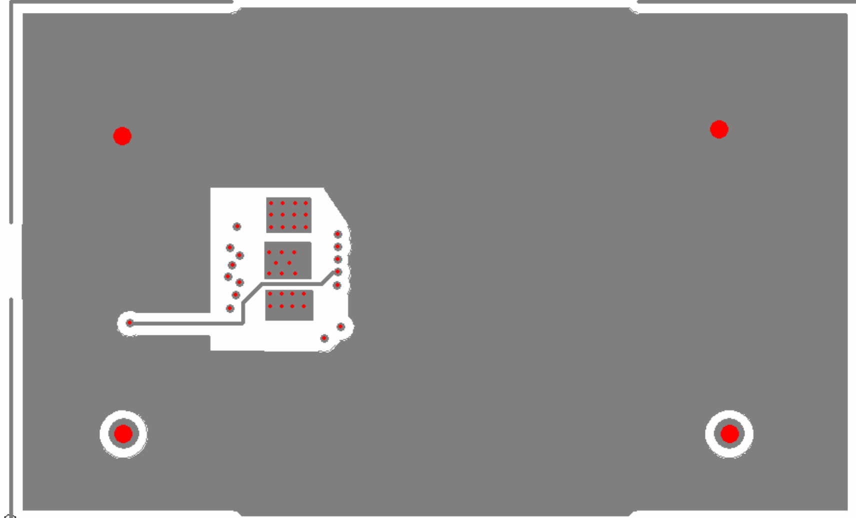


Internal Layer 3

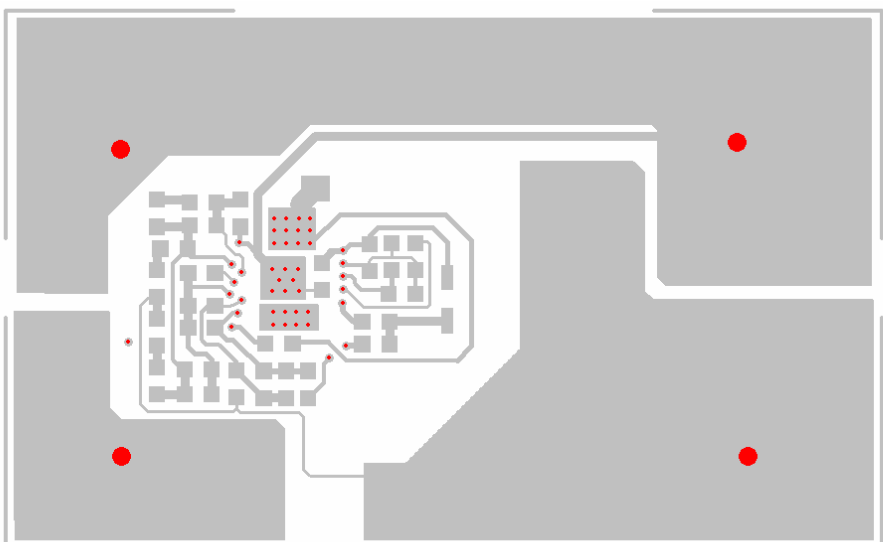
PCB B – Double Sided Components PCB – 4 Layers



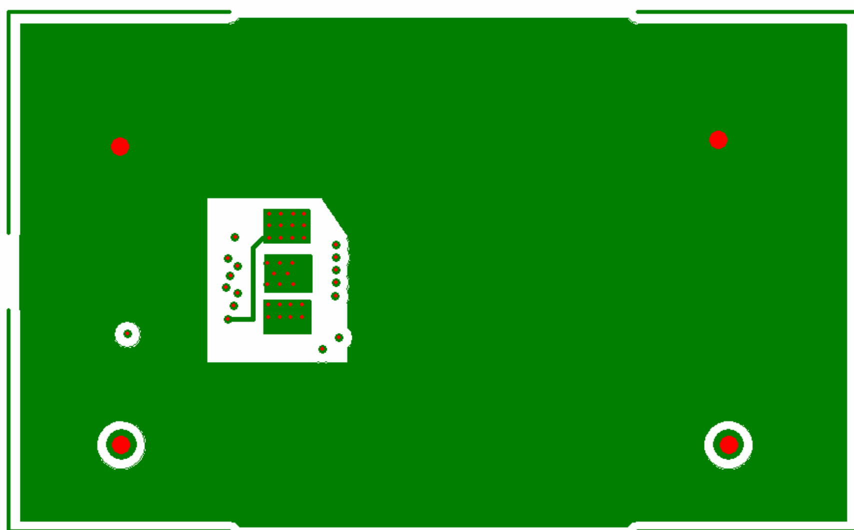
Top Layer



Inner Layer 2



Bottom Layer



Inner Layer 3

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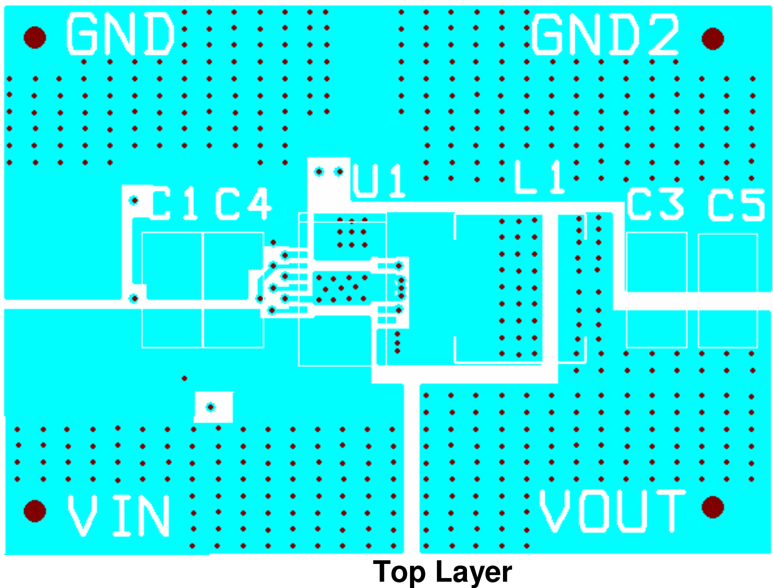
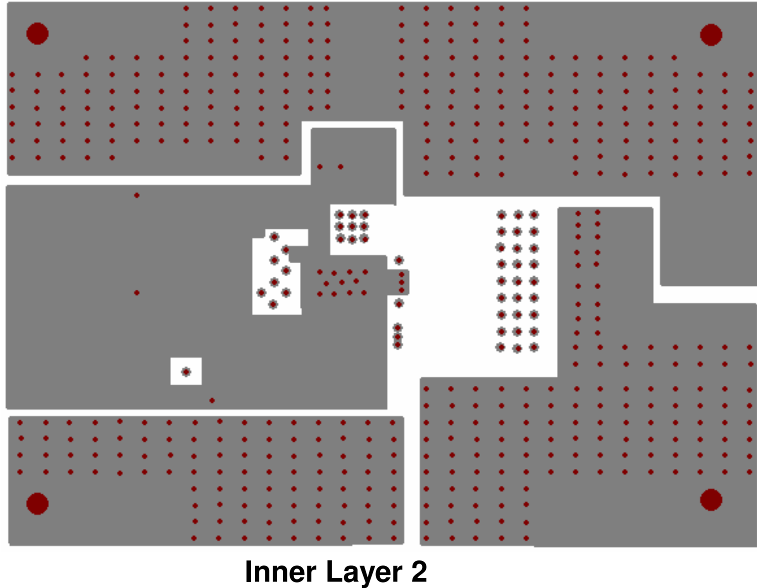
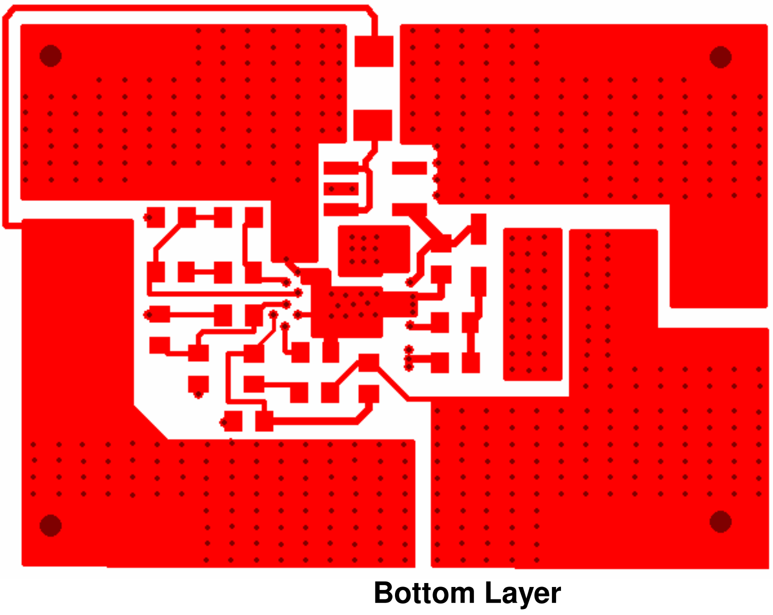
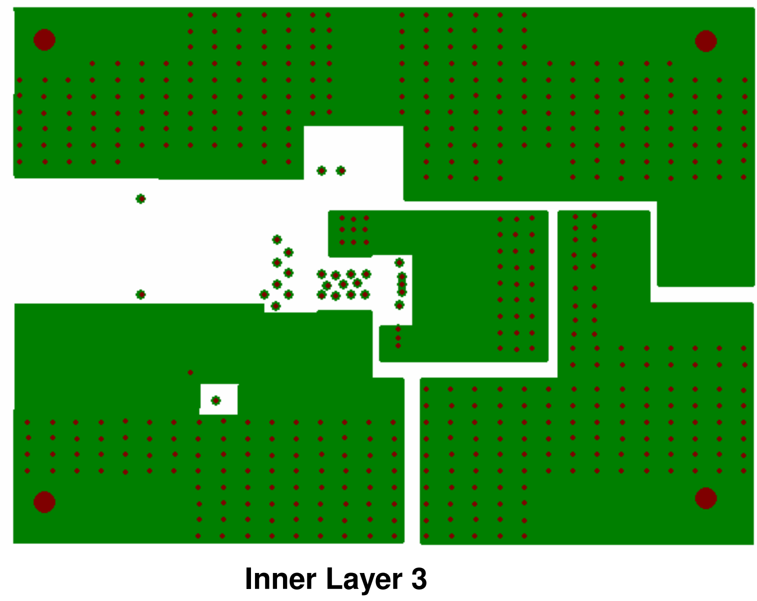
PCB C – Double Sided Components PCB – 4 Layers w/ Multiple Vias – 7655 Evaluation Board



Top Layer


Inner Layer 2


Bottom Layer


Inner Layer 3

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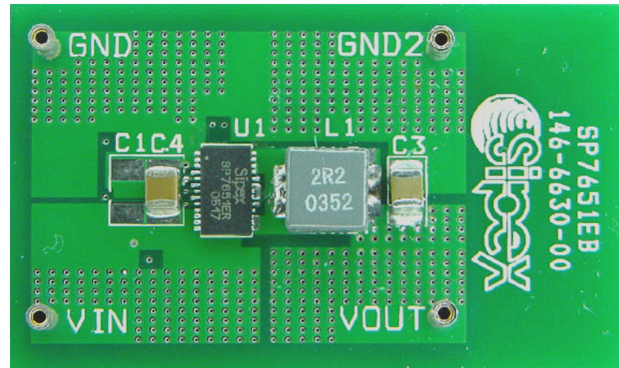
Solved by Sipex

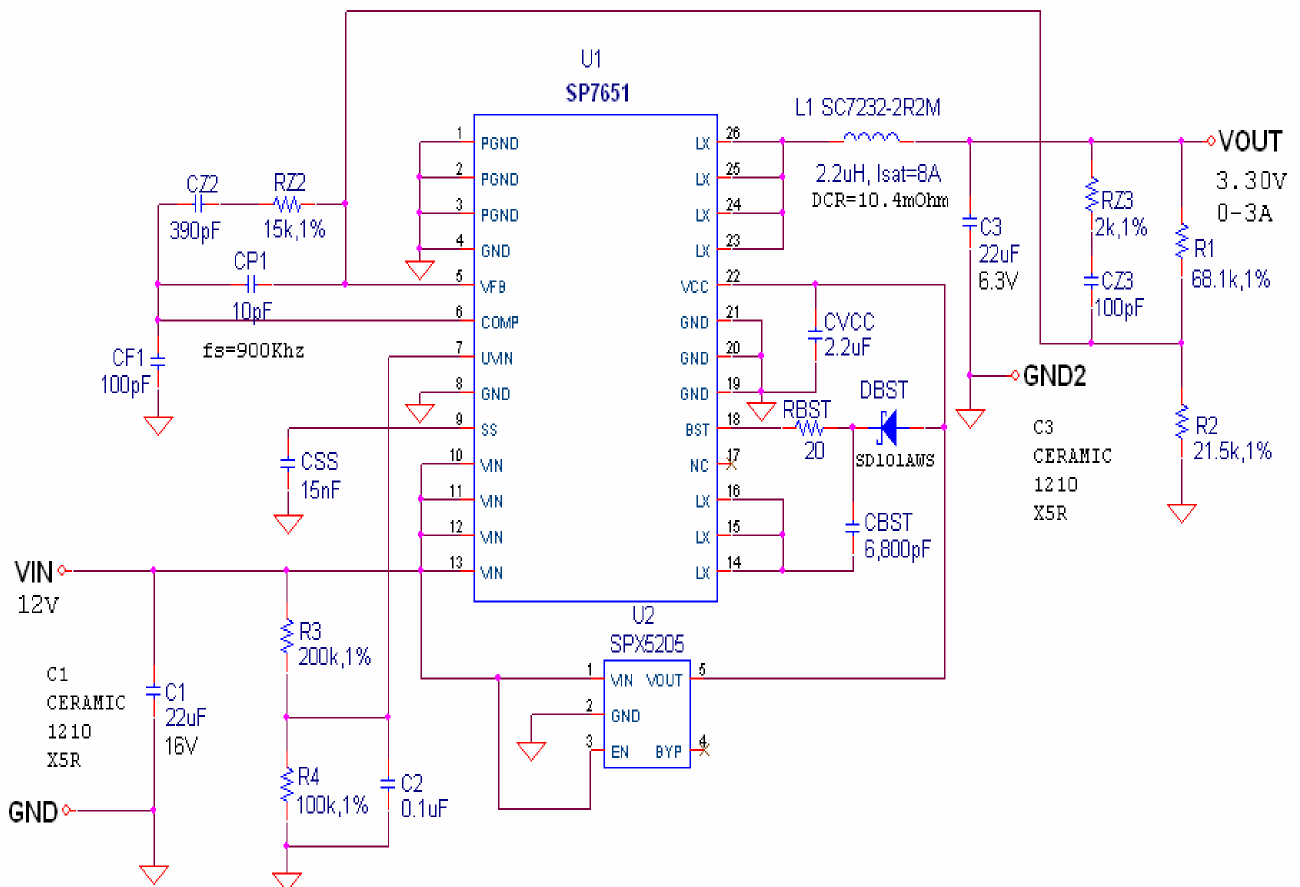
SP7651

Evaluation Board Manual

- Easy Evaluation for the SP7651ER 12V Input, 0 to 3A Output Synchronous Buck Converter
- Built in Low RDS(ON) Power FETs
- UVLO Detects Both Vcc and VIN
- Highly Integrated Design, Minimal Components
- High Efficiency: 88%
- Feature Rich: UVIN, Programmable Softstart, External Vcc Supply and Output Dead Short Circuit Shutdown Protection



SP7651EB SCHEMATIC



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USING THE EVALUATION BOARD

1) Powering Up the SP7651EB Circuit

Connect the SP7651 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the "VIN" and "GND" posts. Connect a Load between the VOUT and GND2 posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

V_{OUT} ripple can best be seen touching the probe tip to the pad for C3 and the scope GND collar touching the GND side of C3 using short wrapped wire around the collar – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP7651 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP7651 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin V_{FB}, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$V_{OUT} = 0.80V (R1 / R2 + 1) \Rightarrow R2 = R1 / [(Vout / 0.80V) – 1]$$

Where R1 = 68.1KΩ and for V_{OUT} = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of the R1 & R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that $50K\Omega \le R1 \le 100K\Omega$ for overall system loop stability.

Note that since the SP7651 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section. In addition, the SP7651ER provides short circuit protection by sensing V_{OUT} at GND.

POWER SUPPLY DATA

The SP7651ER is designed with a very accurate 1.0% reference over line, load and temperature. Figure 1 data shows a typical SP7655 Evaluation Board Efficiency plot, with efficiencies to 87% (including generation of 5V Vcc) and output currents to 3A. SP7651ER Load Regulation is shown in Figure 2 to have only 0.5% change in output voltage from 0.5A load to 3A load. Figures 3 and 4 illustrate a 1.5A to 3A and 0A to 3A Load Step. Start-up Responses in Figures 5, 6 and 7 show a controlled start-up with different output load behavior when power is applied where the input current rises smoothly as the Softstart ramp increases. In Figure 8 the SP7651ER is configured for hiccup mode in response to an output dead short circuit condition and will Soft-start until the over-load is removed. Figure 9 and 10 show output voltage ripple less than 25mV at no load to 3A load.

While data on individual power supply boards may vary, the capability of the SP7651ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

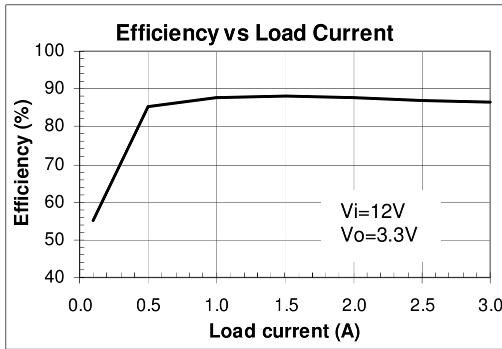


Figure 1. Efficiency vs Load

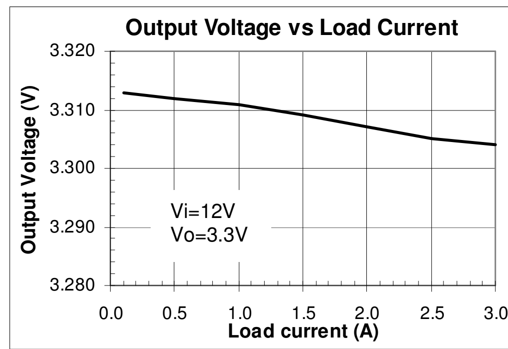


Figure 2. Load Regulation

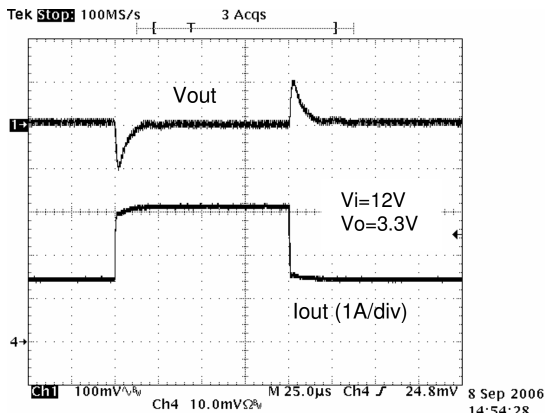


Figure 3. Load Step Response: 1.5->3A

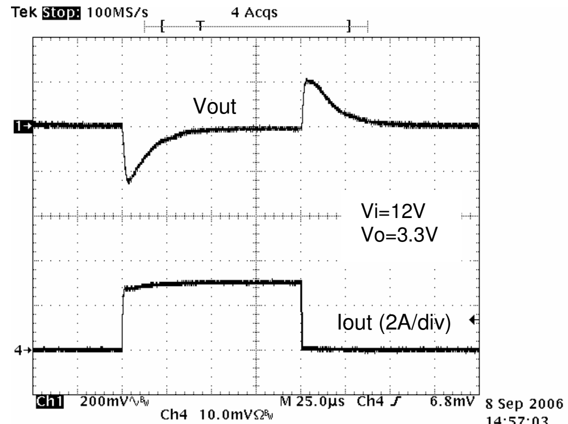


Figure 4. Load Step Response: 0->3A

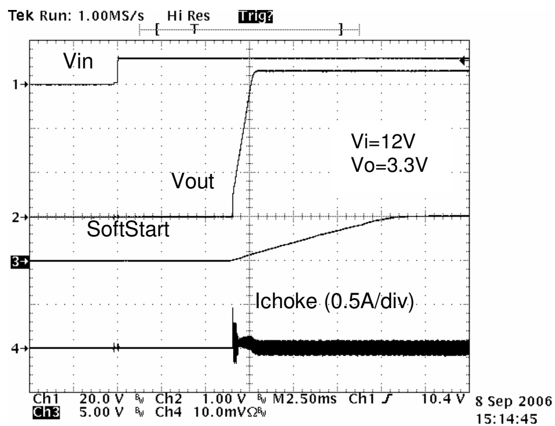


Figure 5. Start-Up Response: No Load

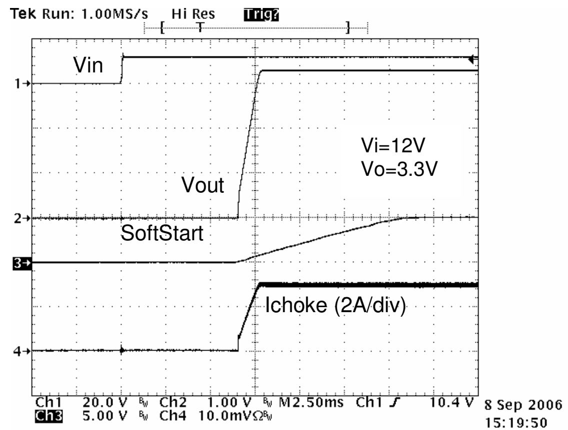


Figure 6. Start-Up Response: 3A Load

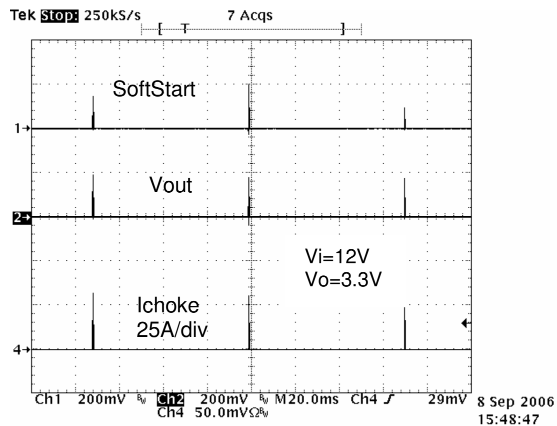


Figure 7. Output Load Short Circuit

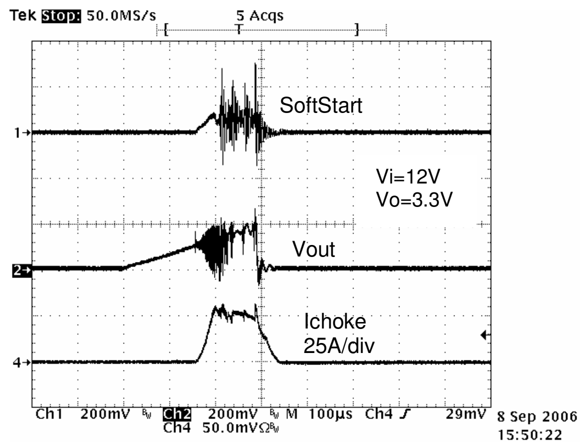


Figure 8. Output Load Short Circuit (Zoom-in)

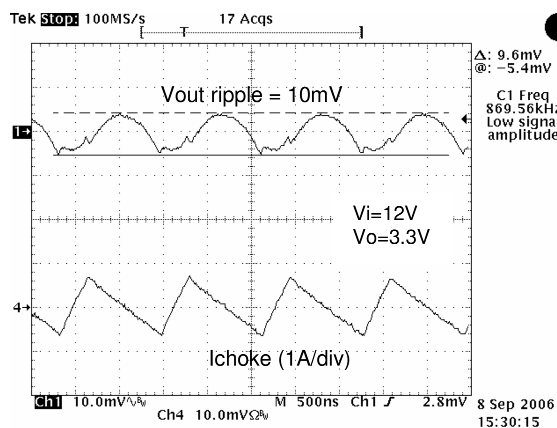


Figure 9. Output Ripple: No Load

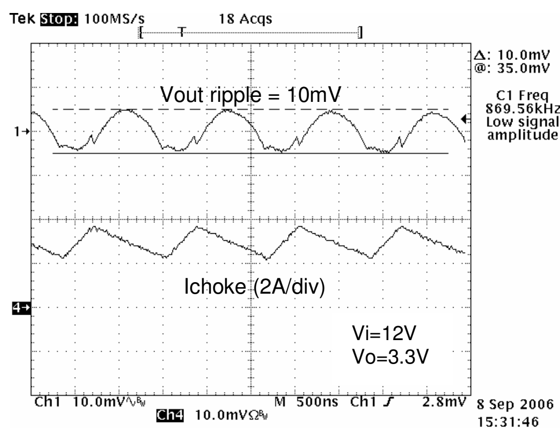
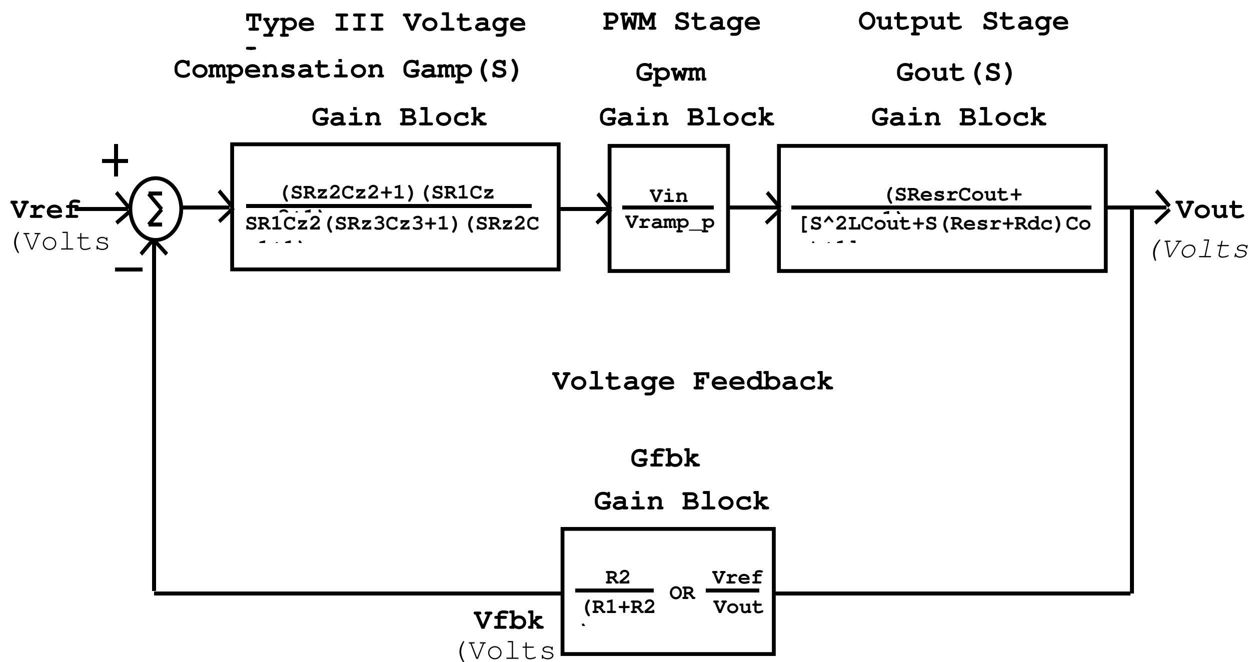


Figure 10. Output Ripple:3A Load

TYPE III LOOP COMPENSATION DESIGN

The open loop gain of the SP7651EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to cross over at the selecting frequency **fco**, the gain of the error amplifier must compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec. The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 to 1/10 of the switching frequency **fs** to insure proper operation. Since the SP7651EB is designed with Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** underdamped resonance double pole frequency.



Definition

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP7651 Internal RAMP Amplitude Peak to Peak Voltage

Condition

Cz2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> Resr and Rdc

Figure 11. Voltage Mode Control Loop with Loop Dynamic for Type III Compensation

The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows:

a. Choose **fco** = fs / 5

b. Calculate **fp_LC**
$fp_LC = 1 / [2\pi (L \bullet C)^{1/2}]$

c. Calculate **fz_ESR**
$fz_ESR = 1 / 2\pi (R_{ESR}) \bullet (C_{OUT})$

d. Select **R1** component value such that $50k\Omega \leq R1 \leq 100k\Omega$

e. Calculate **R2** base on the desired V_{OUT}
$R2 = R1 / [(V_{OUT} / 0.80V) - 1]$

f. Select the ratio of **Rz2** / **R1** gain for the desired gain bandwidth
$Rz2 = R1 (V_{RAMP_PP} / V_{IN_MAX}) (fco / fp_LC)$

g. Calculate **Cz2** by placing the zero at ½ of the output filter pole frequency
$Cz2 = 1 / [\pi (Rz2) \bullet (fp_LC)]$

h. Calculate **Cp1** by placing the first pole at ESR zero frequency
$Cp1 = 1 / [2\pi (Rz2) \bullet (fz_ESR)]$

i. Calculate **Rz3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency
$Rz3 = 2 (R1) (fp_LC) / fs$

j. Calculate **Cz3** from **Rz3** component value above
$Cz3 = 1 / \pi (Rz3) \bullet (fs)$

k. Choose $100pF \leq$ **Cf1** $\leq 220pF$ to stabilize the SP7651ER internal Error Amplifier

Note: Loop Compensation component calculations discussed in this section are further elaborated in the application note #ANP16, "**Loop Compensation of Voltage-Mode Buck Converters".**

These calculations shown here can be quickly iterated with the Type III Loop Compensation Calculator on the web at:
www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

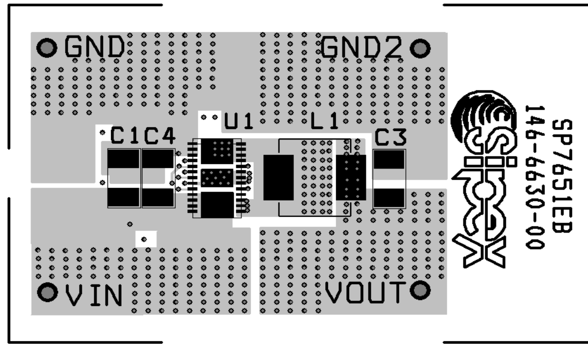


Figure 12. SP7651EB Layout Top Side & Component Placement

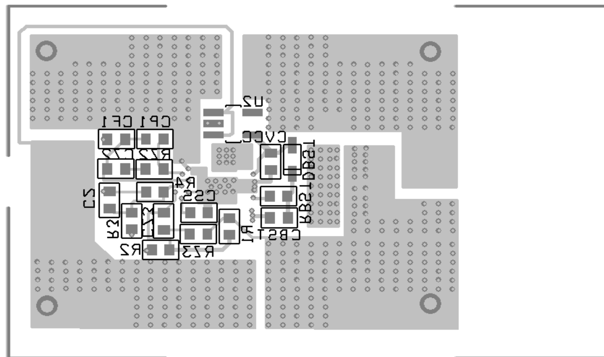


Figure 13. SP7651EB PC Layout Bottom Side & Component Placement

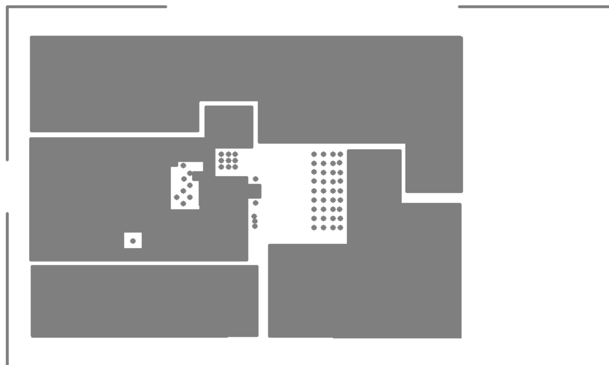


Figure 14. SP7651EB PC Layout Inner Layer 1

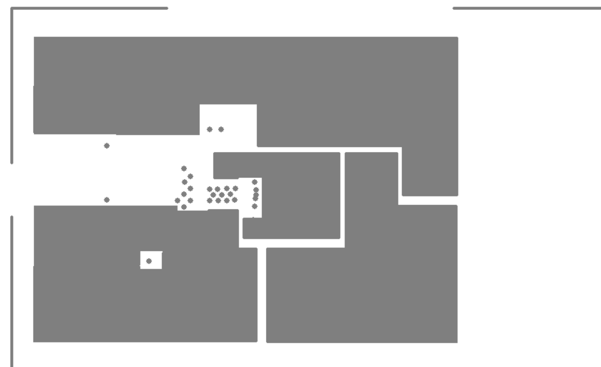


Figure 15. SP7651EB PC Layout Inner Layer 2

Table 1: SP7651EB List of Materials

REF. DES.	QTY	MANUFACTURER NAME	Manufacturer Part Number	SIZE	DESCRIPTION
U1	1	SIPEX	SP7651ER	DFN-26	2-FETs Buck Ctrl
U2	1	Sipex	SPX5205M5-5.0	SOT-23-5	150mA LDO Voltage Regulator
DBST	1	Diodes Inc.	SD101AWS-7	SOD-323	Schottky Diode, 15mA
L1	1	Intertechnical	SC7232-2R2M	7 X 7mm	Inductor, 2.2uH, 8A, 10.4mohm
C3	1	TDK CORPORATION	C3225X5R0J226M	1210	Capacitor, Ceramic, 22uF, 6.3V, X5R, 20%
C4	1	TDK CORPORATION	C3225X5R1C226M	1210	Capacitor, Ceramic, 22uF, 16V, X5R, 20%
CVCC	1	TDK CORPORATION	C1608X5R1A225K	0603	Capacitor, Ceramic, 2.2uF, 10V, X5R, 10%
C2	1	TDK CORPORATION	C1608X7R1H104K	0603	Capacitor, Ceramic, 0.1uF, 50V, X7R, 10%
CBST	1	AVX CORPORATION	06035C682KAT2A	0603	Capacitor, Ceramic, 6.8nF, 50V, X7R, 10%
CSS	1	ROHM	MCH185CN153KK	0603	Capacitor, Ceramic, 15nF, 50V, X7R, 10%
CP1	1	AVX CORPORATION	06035A100JAT2A	0603	Capacitor, Ceramic, 10pF, 50V, C0G, 5%
CZ2	1	AVX CORPORATION	06035A391JAT2A	0603	Capacitor, Ceramic, 390pF, 50V, C0G, 5%
CZ3	1	AVX CORPORATION	06035A101JAT2A	0603	Capacitor, Ceramic, 100pF, 50V, C0G, 5%
CF1	1	ROHM	MCH185A101JK	0603	Capacitor, Ceramic, 100pF, 50V, C0G, 5%
RZ2	1	VISHAY DALE	CRCW0603-1502FRT1	0603	Resistor, 15K, 1/16W, 1%
R2	1	SEI ELECTRONICS	RMC-1/16W-21.5K-1%-TR	0603	Resistor, 21.5K, 1/16W, 1%
RZ3	1	VISHAY DALE	CRCW0603-2001FRT1	0603	Resistor, 2K, 1/16W, 1%
R1	1	VISHAY DALE	CRCW0603-6812FRT1	0603	Resistor, 68.1K, 1/16W, 1%
R3	1	VISHAY DALE	CRCW0603-2003FRT1	0603	Resistor, 200K, 1/16W, 1%
R4	1	VISHAY DALE	CRCW0603-1003FRT1	0603	Resistor, 100K, 1/16W, 1%
RBST	1	ROHM	MCR03EZPEFX20R0	0603	Resistor, 20, 1/16W, 1%
VIN,VOUT, GND,GND2	4	Vector Electronic	K24C/M	.042 Dia	Input/Output Terminal Posts

ORDERING INFORMATION

Model **Temperature Range** **Package Type**

SP7651EB……............................-40°C to +85°C.................…SP7651 Evaluation Board

SP7651ER...............................…. -40°C to +85°C.....................................……26-pin DFN