

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

### 524,288-WORD BY 8-BIT STATIC RAM

#### DESCRIPTION

The TC554001AF/AFT/ATR is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 5.5 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10 mA/MHz (typ) and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 2  $\mu$ A standby current (typ) when chip enable ( $\overline{CE}$ ) is asserted high. There are two control inputs.  $\overline{CE}$  is used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC554001AF/AFT/ATR is available in a standard plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

#### FEATURES

- Low-power dissipation  
Operating: 55 mW/MHz (typical)
- Standby current of 5  $\mu$ A (maximum) at Ta = 25°C
- Single power supply voltage of 2.7 to 5.5 V
- Power down features using  $\overline{CE}$ .
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs

- Access Times (maximum):

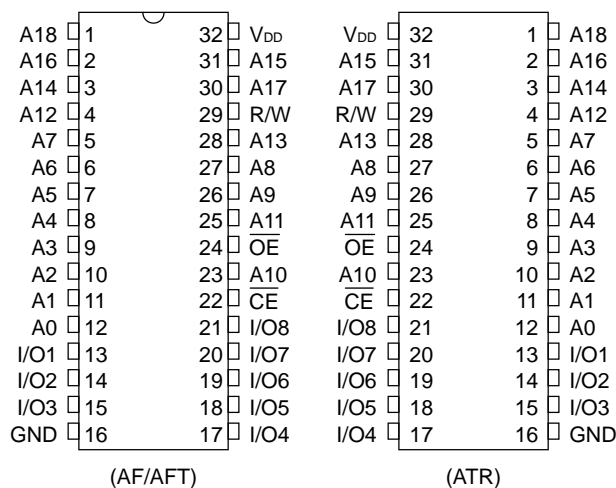
	5 V $\pm$ 10%			2.7 V-5.5 V	
	-70V	-85V	-10V	-70V	-85V/-10V
Access Time	70 ns	85 ns	100 ns	120 ns	150 ns
$\overline{CE}$ Access Time	70 ns	85 ns	100 ns	120 ns	150 ns
$\overline{OE}$ Access Time	35 ns	45 ns	50 ns	70 ns	75 ns

- Package:

SOP32-P-525-1.27 (AF)	(Weight: 1.14 g typ)
TSOP II32-P-400-1.27 (AFT)	(Weight: 0.53 g typ)
TSOP II32-P-400-1.27A (ATR)	(Weight: 0.53 g typ)

#### PIN ASSIGNMENT (TOP VIEW)

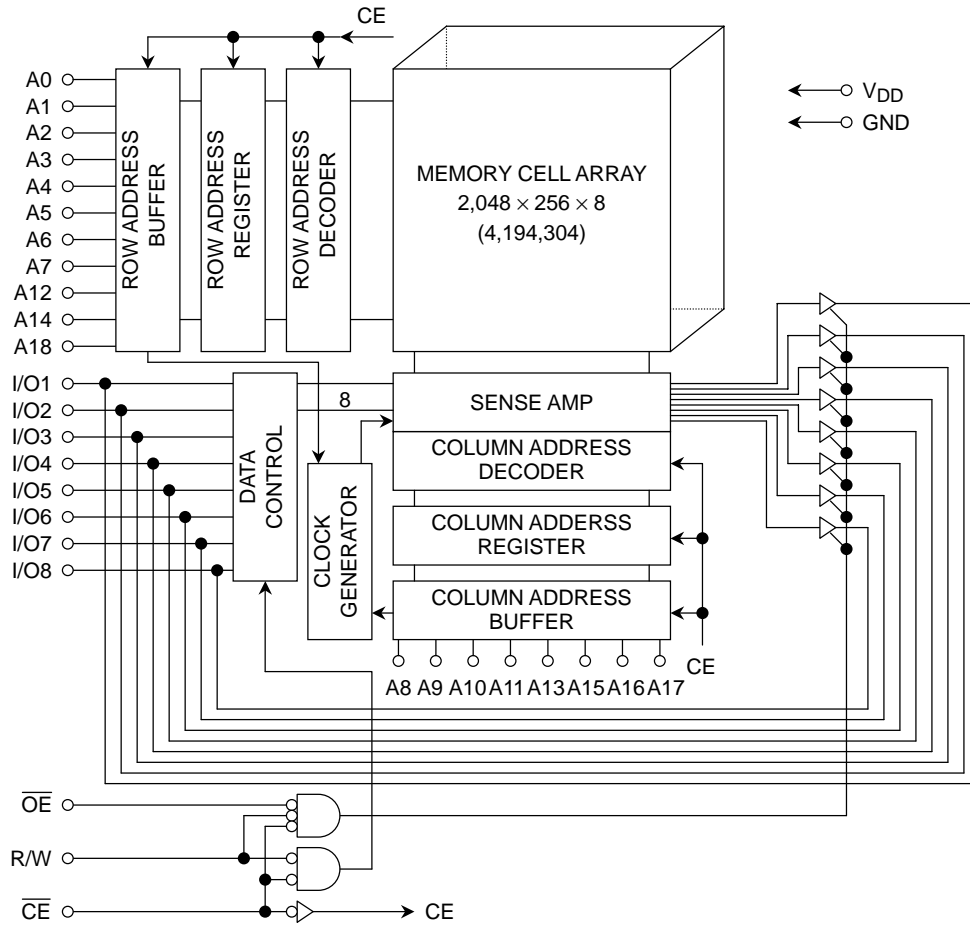
##### 32 PIN SOP & TSOP



#### PIN NAMES

A0~A18	Address Inputs
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1~I/O8	Data Inputs/Outputs
V <sub>DD</sub>	Power (+5 V)
GND	Ground

## BLOCK DIAGRAM



## OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	Output	$I_{DDO}$
Write	L	*	L	Input	$I_{DDO}$
Output Deselect	L	H	H	High-Z	$I_{DDO}$
Standby	H	*	*	High-Z	$I_{DDS}$

\* = don't care  
H = logic high  
L = logic low

## MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
$V_{DD}$	Power Supply Voltage	-0.3~7.0	V
$V_{IN}$	Input Voltage	-0.3*~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5- $V_{DD}$ + 0.5	V
$P_D$	Power Dissipation	0.6	W
$T_{solder}$	Soldering Temperature (10s)	260	°C
$T_{stg}$	Storage Temperature	-55~150	°C
$T_{opr}$	Operating Temperature	0~70	°C

\*: -3.0 V when measured at a pulse width of 50ns

## DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	5 V ± 10%			2.7 V~5.5 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	2.7	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> + 0.3	V <sub>DD</sub> - 0.2	—	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3*	—	0.8	-0.3*	—	0.2	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	2.0	—	5.5	V

\*: -3.0V when measured at a pulse width of 50 ns

## DC CHARACTERISTICS (Ta = 0° to 70°C, V<sub>DD</sub> = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT		
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V~V <sub>DD</sub>	—	—	±1.0	μA		
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ , V <sub>OUT</sub> = 0 V~V <sub>DD</sub>	—	—	±1.0	μA		
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V	-1.0	—	—	mA		
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	2.1	—	—	mA		
I <sub>DDO1</sub>	Operating Current	$\overline{CE} = V_{IL}$ and R/W = V <sub>IH</sub> , I <sub>OUT</sub> = 0 mA, Other Input = V <sub>IH</sub> /V <sub>IL</sub>	t <sub>cycle</sub> = MIN	—	—	70	mA	
			t <sub>cycle</sub> = 1 μs	—	15	—		
I <sub>DDO2</sub>	Operating Current	$\overline{CE} = 0.2$ V and R/W = V <sub>DD</sub> - 0.2 V, I <sub>OUT</sub> = 0 mA, Other Input = V <sub>DD</sub> - 0.2 V/0.2 V	t <sub>cycle</sub> = MIN	—	—	60	mA	
			t <sub>cycle</sub> = 1 μs	—	10	—		
I <sub>DDS1</sub>	Standby Current	$\overline{CE} = V_{IH}$	—	—	3	mA		
I <sub>DDS2</sub>		$\overline{CE} = V_{DD} - 0.2$ V,	V <sub>DD</sub> = 2.0 V~5.5 V	Ta = 25°C	—	2	5	μA
				Ta = 0~70°C	—	—	50	
		V <sub>DD</sub> = 3.0 V	Ta = 25°C	—	2	—	5	
	Ta = 0~40°C		—	—	5			
		Ta = 0~70°C	—	—	25			

## DC CHARACTERISTICS (Ta = 0° to 70°C, VDD = 3.0 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V~V <sub>DD</sub>		—	—	±1.0	μA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ , V <sub>OUT</sub> = 0 V~V <sub>DD</sub>		—	—	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.2 V		-1.0	—	—	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.2 V		0.1	—	—	mA	
I <sub>DDO2</sub>	Operating Current	$\overline{CE} = 0.2$ V and R/W = V <sub>DD</sub> - 0.2 V, I <sub>OUT</sub> = 0 mA, Other Input = V <sub>DD</sub> - 0.2 V/0.2 V	t <sub>cycle</sub> = MIN	—	—	30	mA	
			t <sub>cycle</sub> = 1 μs	—	5	—		
I <sub>DDS2</sub>	Standby Current	$\overline{CE} = V_{DD} - 0.2$ V,	V <sub>DD</sub> = 3.0 ± 0.3 V	Ta = 25°C	—	2	3	μA
				Ta = 0~70°C	—	—	28	
			V <sub>DD</sub> = 3.0 V	Ta = 25°C	—	2	—	
				Ta = 0~40°C	—	—	5	
Ta = 0~70°C	—	—	25	—				

## CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

## AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = 0° to 70°C, VDD = 5 V ± 10%)

### READ CYCLE

SYMBOL	PARAMETER	TC554001AF/AFT/ATR						UNIT
		-70V		-85V		-10V		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	70	—	85	—	100	—	ns
t <sub>ACC</sub>	Address Access Time	—	70	—	85	—	100	
t <sub>CO</sub>	Chip Enable Access Time	—	70	—	85	—	100	
t <sub>OE</sub>	Output Enable Access Time	—	35	—	45	—	50	
t <sub>COE</sub>	Chip Enable Low to Output Active	10	—	10	—	10	—	
t <sub>OEE</sub>	Output Enable Low to Output Active	5	—	5	—	5	—	
t <sub>OD</sub>	Chip Enable High to Output High-Z	—	25	—	30	—	35	
t <sub>ODO</sub>	Output Enable High to Output High-Z	—	25	—	30	—	35	
t <sub>OH</sub>	Output Data Hold Time	10	—	10	—	10	—	

### WRITE CYCLE

SYMBOL	PARAMETER	TC554001AF/AFT/ATR						UNIT
		-70V		-85V		-10V		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	70	—	85	—	100	—	ns
t <sub>WP</sub>	Write Pulse Width	50	—	55	—	60	—	
t <sub>CW</sub>	Chip Enable to End of Write	60	—	70	—	80	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	
t <sub>ODW</sub>	R/W Low to Output High-Z	—	25	—	30	—	35	
t <sub>OEW</sub>	R/W High to Output Active	5	—	5	—	5	—	
t <sub>DS</sub>	Data Setup Time	30	—	35	—	40	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	

### AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Output load	100 pF + 1 TTL Gate
Input pulse level	0.6 V, 2.4 V
Timing measurements	1.5 V
Reference level	1.5 V
t <sub>R</sub> , t <sub>F</sub>	5 ns

## AC CHARACTERISTICS AND OPERATING CONDITIONS

( $T_a = 0^\circ$  to  $70^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$  to  $5.5\text{ V}$ )

### READ CYCLE

SYMBOL	PARAMETER	TC554001AF/AFT/ATR				UNIT
		-70V		-85V/-10V		
		MIN	MAX	MIN	MAX	
$t_{RC}$	Read Cycle Time	120	—	150	—	ns
$t_{ACC}$	Address Access Time	—	120	—	150	
$t_{CO}$	Chip Enable Access Time	—	120	—	150	
$t_{OE}$	Output Enable Access Time	—	70	—	75	
$t_{COE}$	Chip Enable Low to Output Active	10	—	10	—	
$t_{OEE}$	Output Enable Low to Output Active	5	—	5	—	
$t_{OD}$	Chip Enable High to Output High-Z	—	50	—	50	
$t_{ODO}$	Output Enable High to Output High-Z	—	50	—	50	
$t_{OH}$	Output Data Hold Time	10	—	10	—	

### WRITE CYCLE

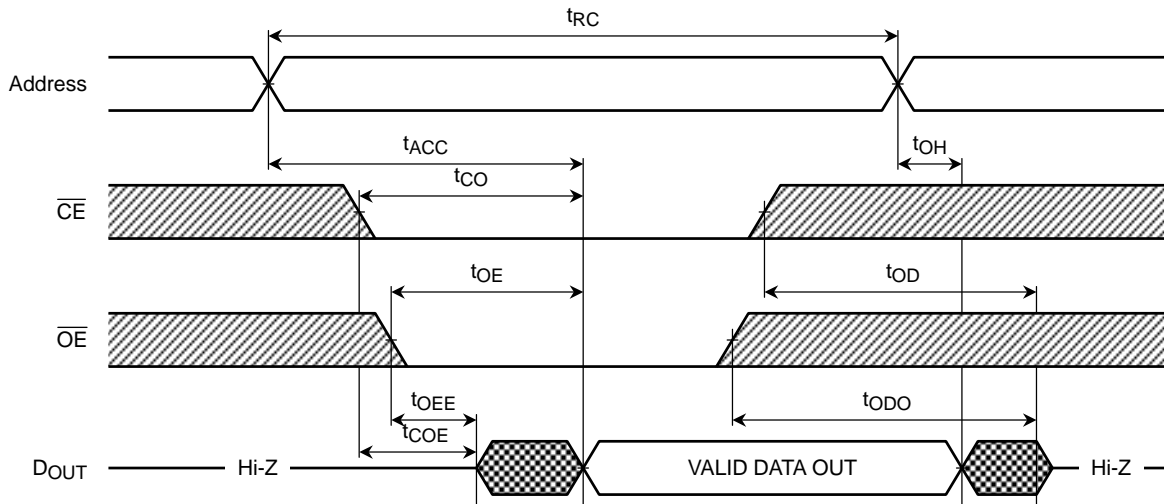
SYMBOL	PARAMETER	TC554001AF/AFT/ATR				UNIT
		-70V		-85V/-10V		
		MIN	MAX	MIN	MAX	
$t_{WC}$	Write Cycle Time	120	—	150	—	ns
$t_{WP}$	Write Pulse Width	80	—	100	—	
$t_{CW}$	Chip Enable to End of Write	100	—	120	—	
$t_{AS}$	Address Setup Time	0	—	0	—	
$t_{WR}$	Write Recovery Time	0	—	0	—	
$t_{ODW}$	R/W Low to Output High-Z	—	50	—	50	
$t_{OEW}$	R/W High to Output Active	5	—	5	—	
$t_{DS}$	Data Setup Time	50	—	60	—	
$t_{DH}$	Data Hold Time	0	—	0	—	

## AC TEST CONDITIONS

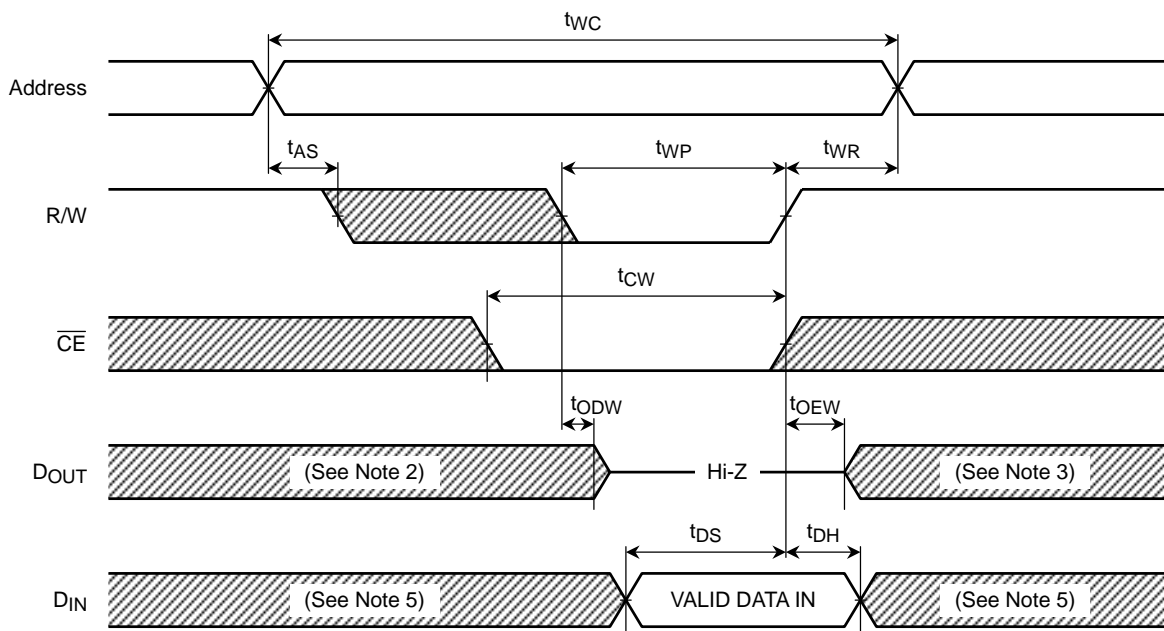
PARAMETER	TEST CONDITION
Output load	100 pF (Include Jig)
Input pulse level	$V_{DD} - 0.2\text{ V}$ , $0.2\text{ V}$
Timing measurements	1.5 V
Reference level	1.5 V
$t_R$ , $t_F$	5 ns

## TIMING DIAGRAMS

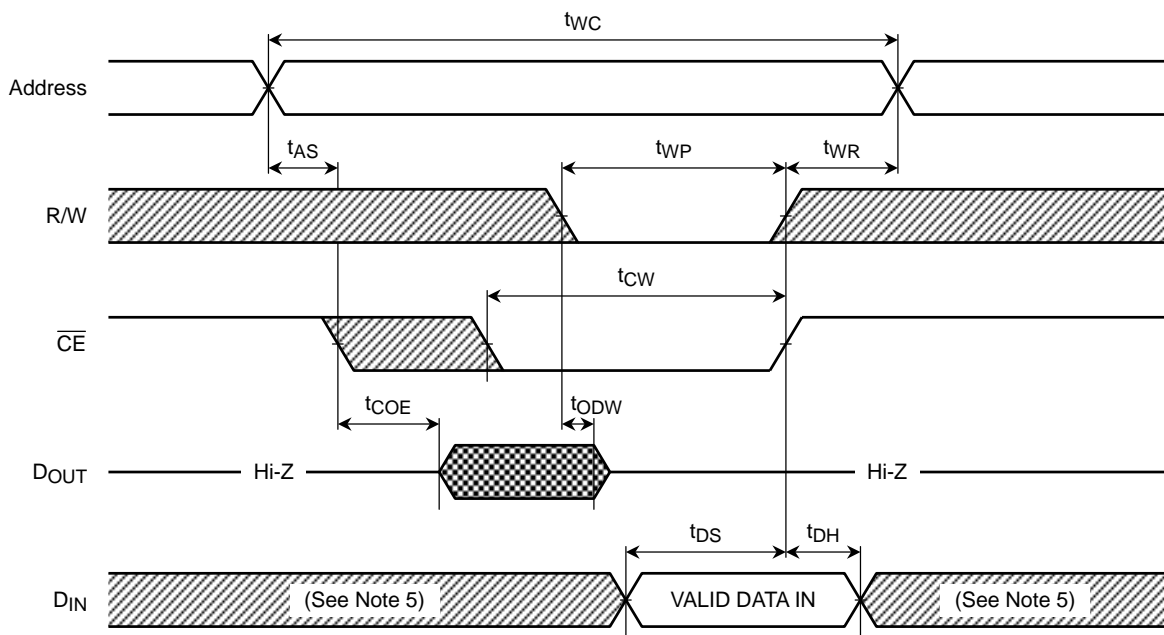
### READ CYCLE (See Note 1)



### WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



## WRITE CYCLE 2 ( $\overline{CE}$ CONTROLLED) (See Note 4)



### Note:

- (1) R/W remains HIGH for the read cycle.
- (2) If  $\overline{CE}$  goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If  $\overline{CE}$  goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

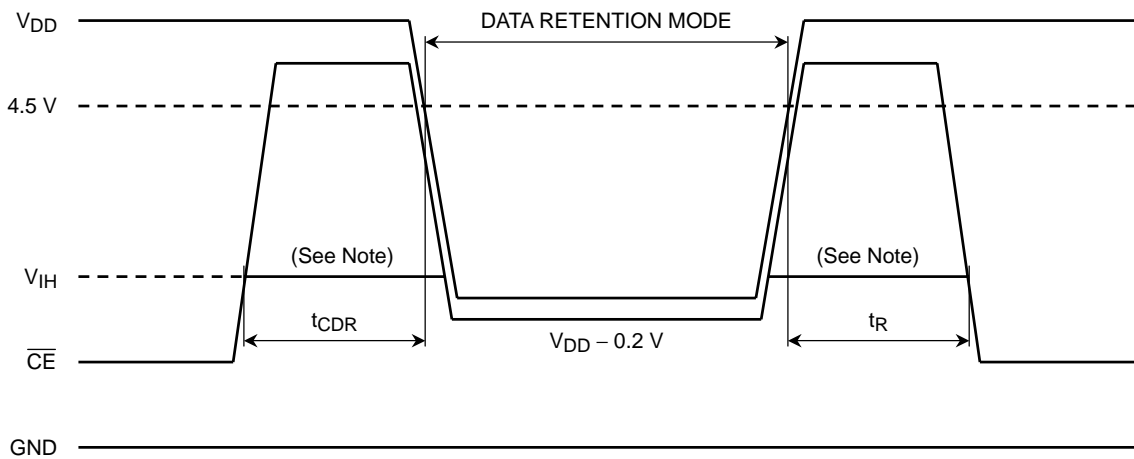


**DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.0 V	—	25*	μA
		V <sub>DH</sub> = 5.5 V	—	50	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time	0	—	—	ns
t <sub>R</sub>	Recovery Time	5	—	—	ms

\*: 5 μA (max) at Ta = 0° to 40°C

**CE CONTROLLED DATA RETENTION MODE**

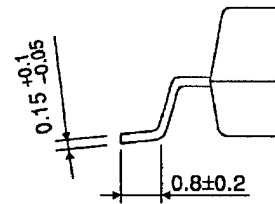
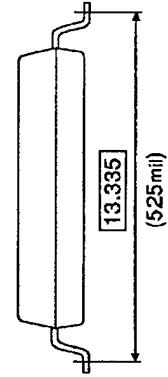
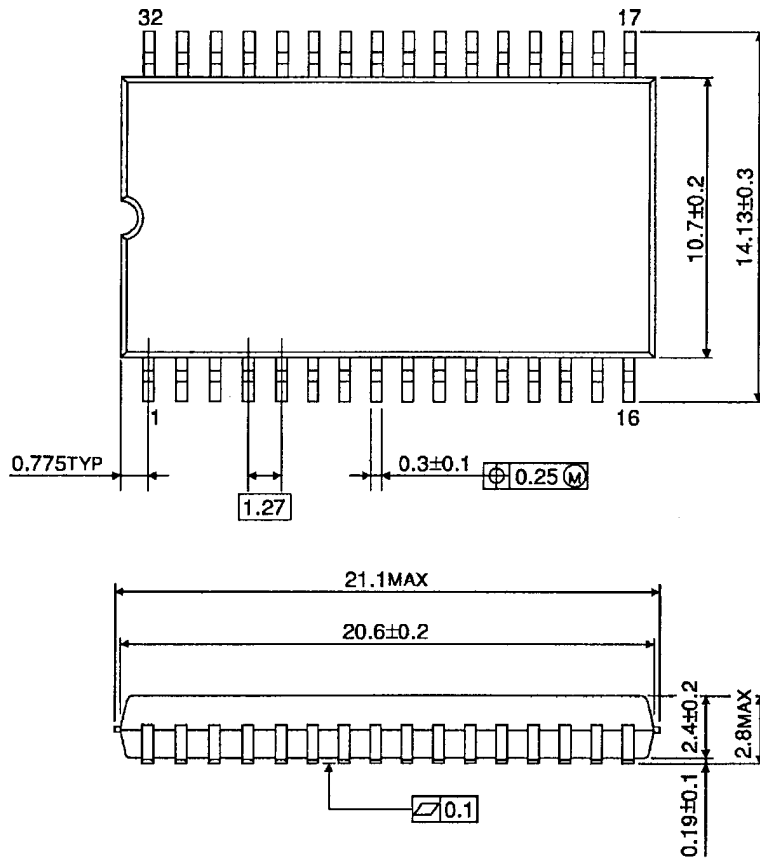


Note: When  $\overline{CE}$  is operating at the V<sub>IH</sub> level (2.2V), the standby current is given by I<sub>DDS1</sub> during the transition of V<sub>DD</sub> from 4.5 to 2.4V.

## PACKAGE DIMENSIONS

SOP32-P-525-1.27

Unit : mm

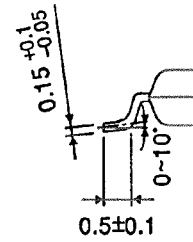
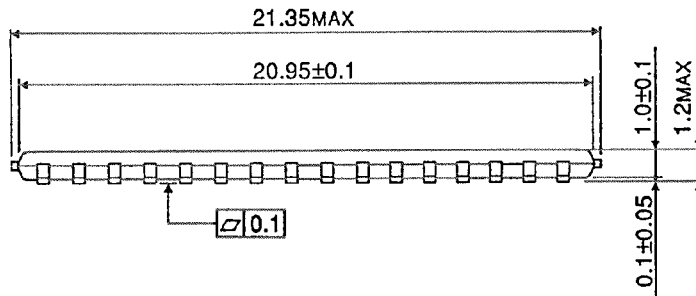
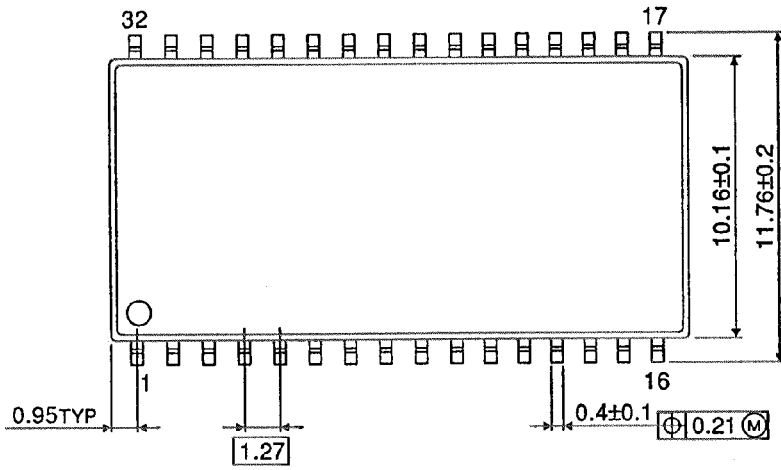


Weight: 1.14 g (typ)

## PACKAGE DIMENSIONS

TSOPII32-P-400-1.27

Unit: mm

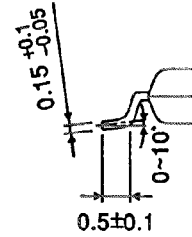
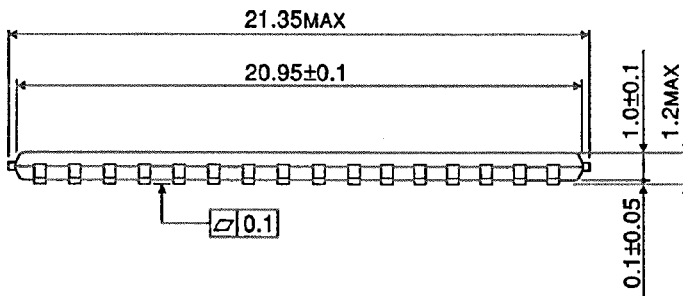
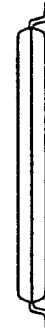
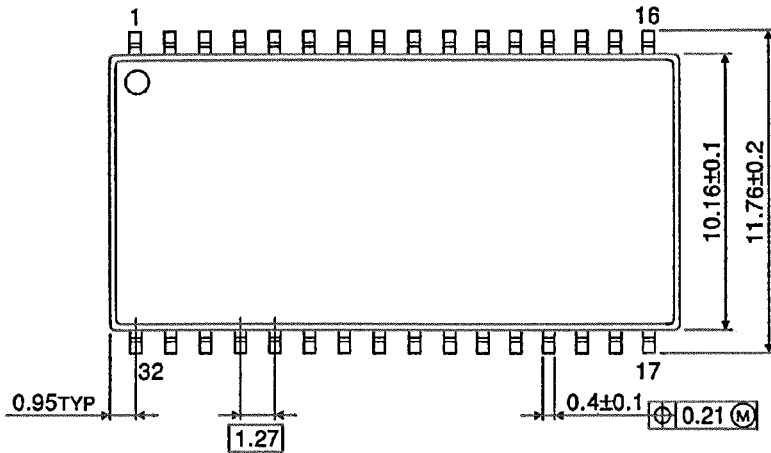


Weight: 0.53 g (typ)

## PACKAGE DIMENSIONS

TSOPII32-P-400-1.27A

Unit: mm



Weight: 0.53 g (typ)

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