Monolithic Video A/D Converter

7-Bit, 20Msps

The TRW TDC1047 is a 20Msps (MegaSample Per Second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7MHz into 7-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are TTL compatible.

The TDC1047 consists of 127 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

The TDC1047 is pin and function compatible with TRW's TDC1027, and offers increased performance with lower power dissipation.

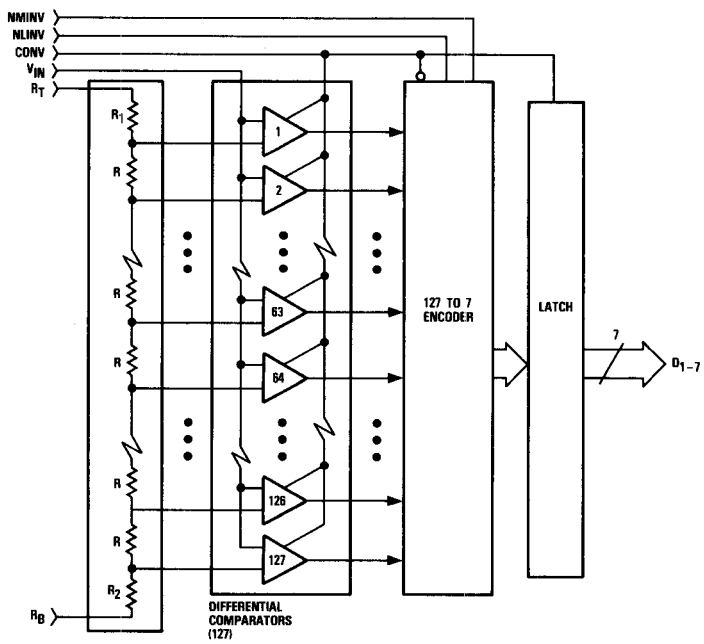
Features

- 7-Bit Resolution
- 1/2 LSB Linearity
- Sample-And-Hold Circuit Not Required
- 20Msps Conversion Rate
- Selectable Output Format
- Available In 24 Pin CERDIP

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- TV Special Effects
- Video Simulators
- Radar Data Conversion

Functional Block Diagram



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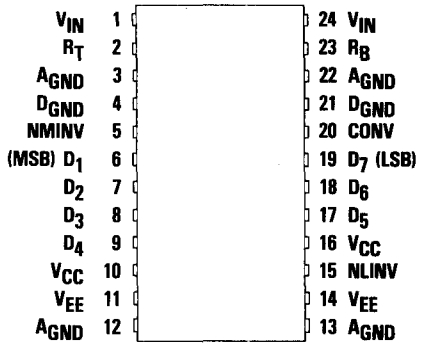
Pin Assignments



24 Pin CERDIP – B7 Package

Functional Description

General Information

The TDC1047 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 127 reference voltages to produce an N-of-127 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-127 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1047 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1047 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.8V and 1.2V. The nominal voltages are V_{RT} = 0.00V and V_{RB} = −1.00V. These voltages may be varied dynamically up to 7MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically as in an Automatic Gain Control (AGC) circuit, a low-impedance reference source is recommended.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1047 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within the Sampling Time Offset (t_{STO}) of a rising edge on the CONV pin. The 127 to 7 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e., data for sample N is acquired by the external circuitry while the TDC1047 is taking input sample N+2.

Analog Input

The TDC1047 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, both V_{IN} pins must be used and the source impedance of the driving circuit must be less than 30 Ohms. The input signal will not damage the TDC1047 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 127 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1047 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal.

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	10, 16
	V_{EE}	Negative Supply Voltage	−5.2V	11, 14
	D_{GND}	Digital Ground	0.0V	4, 21
	A_{GND}	Analog Ground	0.0V	3, 12, 13, 22
Reference	R_T	Reference Resistor (Top)	0.00V	2
	R_B	Reference Resistor (Bottom)	−1.00V	23
Controls	NMINV	Not Most Significant Bit INVert	TTL	5
	NLINV	Not Least Significant Bit INVert	TTL	15
Convert	CONV	Convert	TTL	20
Analog Input	V_{IN}	Analog Signal Input	0V to −1V	1, 24
Outputs	D_1	MSB Output	TTL	6
	D_2		TTL	7
	D_3		TTL	8
	D_4		TTL	9
	D_5		TTL	17
	D_6		TTL	18
	D_7	LSB Output	TTL	19

Figure 1. Timing Diagram

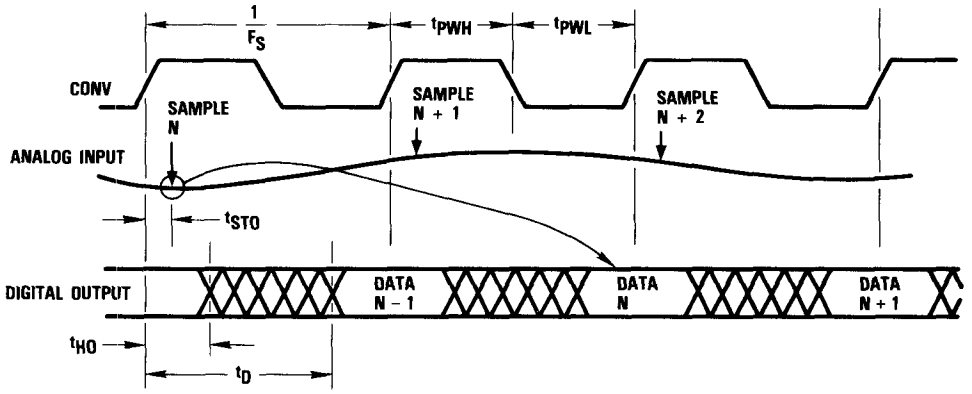


Figure 2. Simplified Analog Input Equivalent Circuit

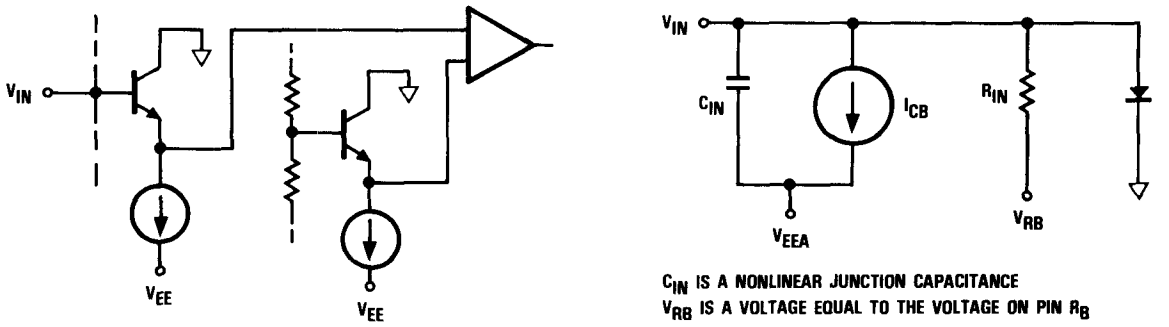


Figure 3. Digital Input Equivalent Circuit

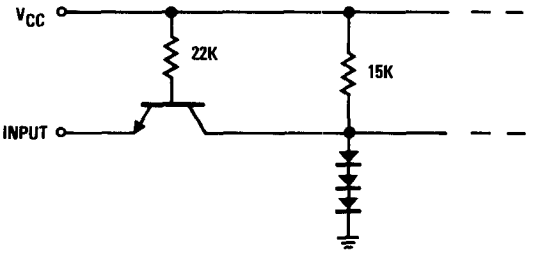
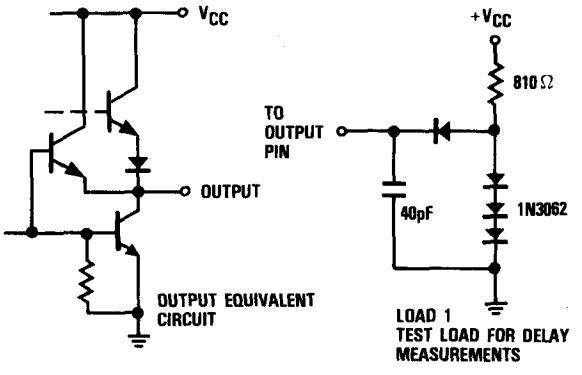


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged)[1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... −0.5 to +7.0V
V_{EE} (measured to A_{GND}) ..... +0.5 to −7.0V
A_{GND} (measured to D_{GND}) ..... −0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... +0.5 to V_{EE}
V_{RT} (measured to V_{RB}) ..... +2.2 to −2.2V

Output

Applied voltage (measured to D_{GND}) ..... −0.5 to 5.5V[2]
Applied current, externally forced ..... −1.0 to 6.0mA[3,4]
Short circuit duration (single output in high state to ground) ..... 1 sec

Temperature

Operating, case ..... −55 to + 125°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter	Test Conditions	Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	14			14			ns
t_{PWH}	CONV Pulse Width, HIGH	16			16			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4			−0.4	mA
V_{RT}	Most Positive Reference Input[1]	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input[1]	−0.9	−1.0	−1.1	−0.9	−1.0	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8	1.0	1.2	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max, static[1]		25		30	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, static[1]					
		T_A = 0°C to 70°C		-170			mA
		T_A = 70°C		-135			mA
		T_C = -55°C to 125°C				-220	mA
		T_C = 125°C				-130	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom		35		50	mA
R_{REF}	Total Reference Resistance		28		20		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	100		40		kOhms
C_{IN}	Input Capacitance			60		60	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		150		300	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.5V CONV		-0.4		-0.6	mA
		NMINV, NLINV		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = Max, one pin to ground, one second duration.		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = Min, V_{EE} = Min	20		20		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = Min, V_{EE} = Min		7		10	ns
t_D	Output Delay	V_{CC} = Min, V_{EE} = Min, Load 1		30		35	ns
t_{HO}	Output Hold Time	V_{CC} = Max, V_{EE} = Max, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range				Units
				Standard		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity Error	Integral, Independent	V_{RT}, V_{RB} = Nom		0.4		0.4	%
E_{LD}	Linearity Error	Differential			0.4		0.4	%
CS	Code Size		V_{RT}, V_{RB} = Nom	30	170	30	170	% Nominal
V_{OT}	Offset Voltage	Top	V_{IN} = V_{RT}		+50		+50	mV
V_{OB}	Offset Voltage	Bottom	V_{IN} = V_{RB}		−30		−30	mV
T_{CO}	Temperature Coefficient				±20		±20	μV/°C
BW	Bandwidth, Full Power Input			7		7		MHz
t_{TR}	Transient Response, Full Scale				10		10	ns
SNR	Signal-to-Noise Ratio		7MHz Bandwidth,					
			20MSPS Conversion Rate					
		Peak Signal/RMS Noise	1MHz Input	48		46		dB
			7MHz Input	46		44		dB
		RMS Signal/RMS Noise	1MHz Input	39		37		dB
			7MHz Input	37		35		dB
E_{AP}	Aperture Error				50		50	ps
DP	Differential Phase Error[1]		F_S = 4 x NTSC		1.5		1.5	Degree
DG	Differential Gain Error[1]		F_S = 4 x NTSC		2.5		2.5	%

Note:
1. In excess of quantization.

Output Coding

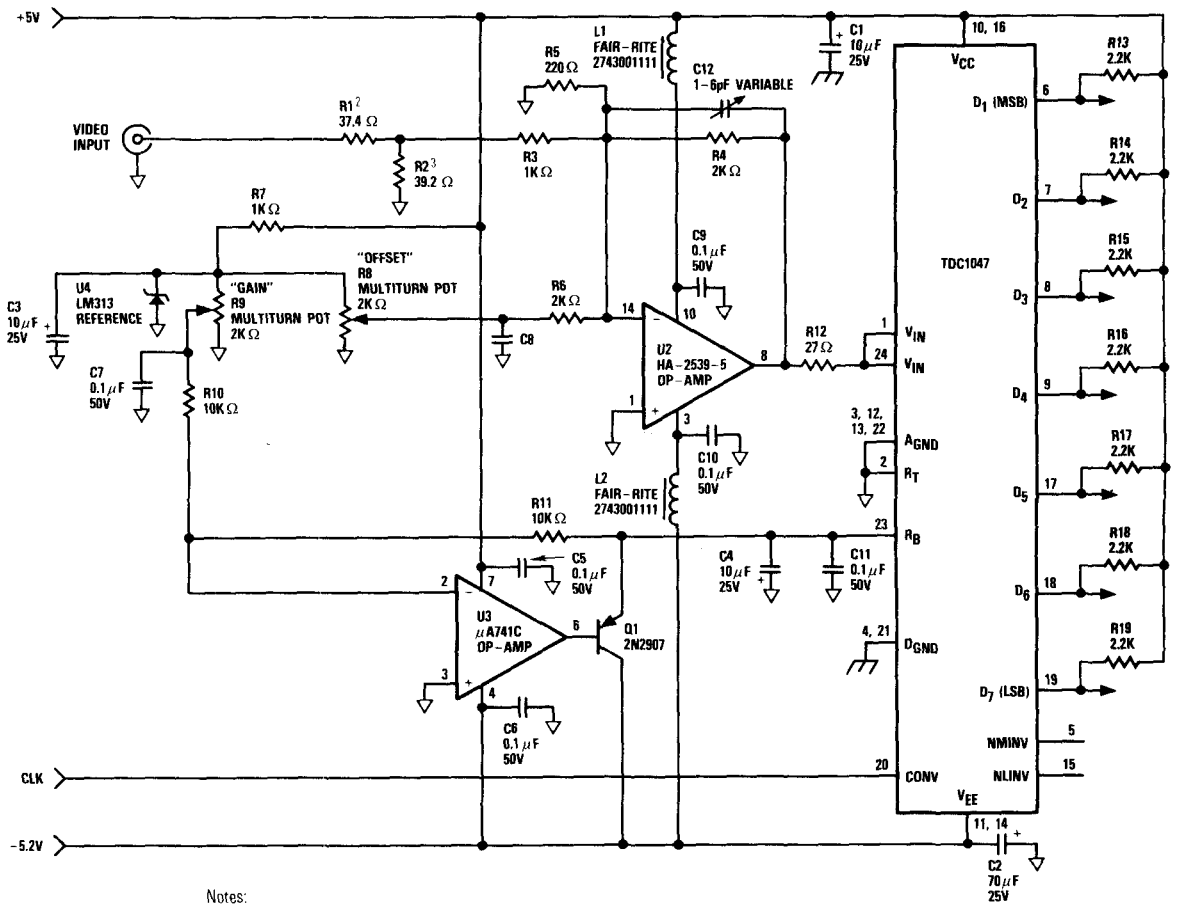
Step		Binary		Offset Two's Complement	
	Range	True	Inverted	True	Inverted
	−1.0000V FS	NMINV = 1	0	0	1
	7.874mV STEP	NLINV = 1	0	1	0
000	0.0000V	0000000	1111111	1000000	0111111
001	−0.0078V	0000001	1111110	1000001	0111110
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
063	−0.4960V	0111111	1000000	1111111	0000000
064	−0.5039V	1000000	0111111	0000000	1111111
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
126	−1.9921V	1111110	0000001	0111110	1000001
127	−1.0000V	1111111	0000000	0111111	1000000

Note:
1. Voltages are code midpoints when calibrated (see Calibration Section).

Calibration

To calibrate the TDC1047, adjust V_{RT} and V_{RB} to set the 1st and 127th thresholds to the desired voltages in the block diagram. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0039V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9961V and adjust V_{RB} for toggling between codes 126 and 127. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

Figure 5. Typical Interface Circuit



Notes:

1. Unless otherwise specified, all resistors are 1/4W, 2%.
2. $R1 = Z_{IN} - \left(\frac{1000\ R2}{1000 + R2}\right)$
3. $R2 = \frac{1}{\left(\frac{2V_{Range}}{V_{REF}\ Z_{IN}}\right) - 0.001}$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1047B7C	STD–T_A=0°C to 70°C	Commercial	24 Pin CERDIP	1047B7C
TDC1047B7V	EXT–T_C=–55°C to 125°C	MIL-STD-883	24 Pin CERDIP	1047B7V

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