THC63DV164

170MHz 12/24Bit COLOR DVI Compliant Transmitter

General Description

The THC63DV164 is transmitter compliant with DVI Rev.1.0. The THC63DV164 converts 24bits of CMOS/ TTL data into differential signaling data which standardized by DDWG (Digital Display Working Group). The THC63DV164 supports display resolution from VGA to UXGA(25-170MHz) with 24bit true color RGB data stream.

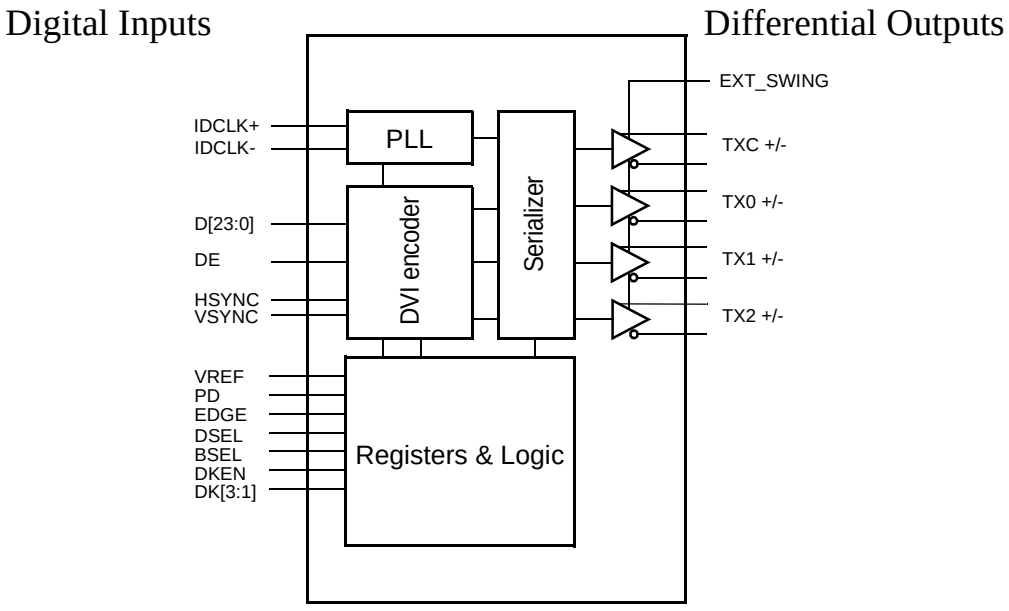
Excellent on-chip jitter specification and high tolerance to clock jitter is achieved by the built-in PLL based on proprietary hi-frequency PLL technologies used in the THine's LVDS products. Newly developed innovative DVI encode and decode technologies accomplished very low power consumption preferable for portable application.

THC63DV164 has 12bit or 24bit mode interface and dual edge/single clock (12bit mode) or single/dual clock edge clocking (24bit mode). THC63DV164 supports Receiver Detection.

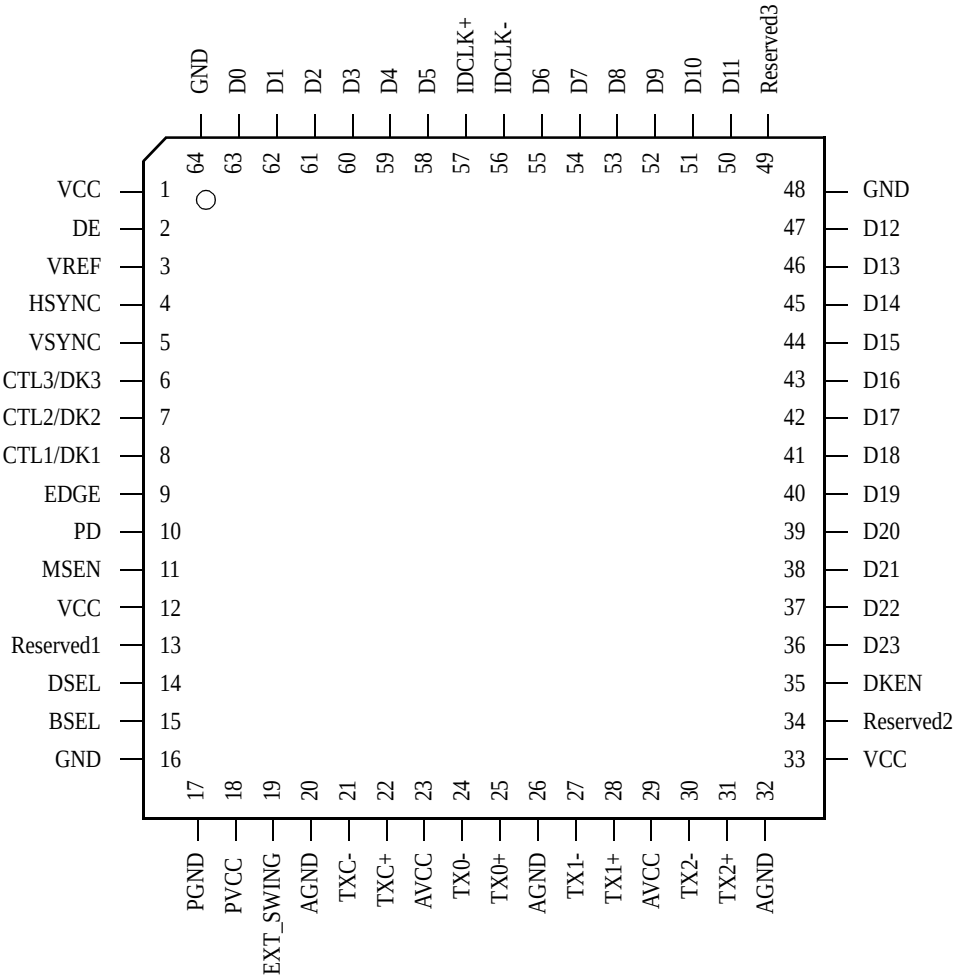
Features

- Compliant with DVI Rev.1.0
- Wide Frequency Range: 25MHz-170MHz
- PLL requires No external components
- Programmable Single/Dual Clocking Mode
- Small Swing with V_{REF} Interface Support
- Power down mode
- Low power single 3.3V CMOS design
- 64pin TQFP
- Pin Compatible with the Silicon Image SiI164

Block Diagram



Pin Out



Pin Description

Pin Name	Pin #	Type	Description
TX0+, TX0-	25, 24	Out	Differential Data output pairs. (DVI v1.0 compliant)
TX1+, TX1-	28, 27	Out	
TX2+, TX2-	31, 30	Out	
TXC+, TXC-	22, 21	Out	Differential Clock output pairs. (DVI v1.0 compliant)
D23 ~ D12	36-47	In	Top half of 24bit pixel bus.
D11 ~ D0	50-55,58-63	In	Bottom half of 24bit pixel bus / 12bit pixel input. When **BSEL = High**, this bus inputs the bottom half of the 24bit pixel bus. When **BSEL = Low**, this bus inputs 1/2 pixel (12-bit) at both rising and falling edge of the clock.
IDCLK+	57	In	Input Data Clock +.
IDCLK-	56	In	Input Data Clock -. This clock **ONLY** used in 12bit mode when **DSEL = Low**, dual edge clocking is turned off. It is used to provide ODD pixel data latch timing with dual clock single edge. If **BSEL = High** or **DSEL = High**, this pin should be tied to GND.

Pin Name	Pin #	Type	Description
DE	2	In	Data enable. This signal is high when input pixel data is valid to the transmitter and low otherwise. It is critical that this signal have the same setup/hold timings as the data bus.
HSYNC VSYNC	4 5	In	Horizontal Sync input control signal. Vertical Sync input control signal.
CTL1/DK1 CTL2/DK2 CTL3/DK3	8 7 6	In In In	The use of multi-function inputs depends in setting of ISEL and DKEN. These inputs are regular 3.3V CMOS level inputs. These inputs pins contain weak pull down resistors so that if left unconnected, they will be Low. **DKEN=LOW** General purpose input CTL[3:1] are active, for backward compatibility. These pins must be used to send DC signal only during blanking time. **DKEN=High** DK[3:1] are active, these inputs are used to select deskewing setting for the pixel data latching.
MSEN	11	Out	Monitor Sense. This pin is an open source output. An external 5K pull-up resistor is required on this pin for systems, there is no internal pull-up resistor. **High** level indicates a powered on receiver is detected at the all of differential outputs.
BSEL	15	In	Input bus select. **BSEL=High** Select 24bit input mode. **BSEL=Low** Select 12bit input mode.
DSEL	14	In	Dual edge clock select. **DSEL=High** Dual edge mode is selected. IDCLK+ latches input pixels data both falling and rising edges. **DSEL=Low** Single edge mode is selected. IDCLK+/- latches input pixel data on only falling or rising edges. IDCLK+ latches 1st half of data and IDCLK- latches 2nd half of data at 12bit mode.
EDGE	9	In	Edge select. **DSEL=High (dual edge mode)** **EDGE=Low** The Primary edge (first/even latch edge after DE asserted) is the falling edge. **EDGE=High** The Primary edge (first/odd latch edge after DE asserted) is the rising edge. Note: the case of BSEL=High and DSEL=high, EDGE is ignored (See Page10). **DSEL=Low (single edge mode)** **EDGE=Low** The falling edge of the clock is used to latch pixel data. **EDGE=High** The rising edge of the clock is used to latch pixel data.

Pin Name	Pin #	Type	Description
DKEN	35	In	Setup/hold trim select. **DKEN=High** DK[3:1] is used as the setup/hold trim (de-skewing) setting. The trimming step is 200psec in typical. **DKEN=Low** Default trimming setting is used.
VREF	3	Analog	Input reference voltage. Select the swing range of the digital pixel data and control inputs (D[23:0],DE,VSYNC,HSYNC and IDCLK+/-).
EXT_SWING	19	Analog	Voltage swing adjust. A resistor should tie this pin to AVCC. This resistance determines the amplitude of the differential output swing. For remote display applications, 400Ω is recommended. For notebook computers, 680Ω is recommended.
PD	10	In	Power Down **PD=High** Normal operation. **PD=Low** All Input Pins are desabled and all differential outputs are HiZ. MSEN is to Low forced.
Reserved1	13	In	If Low, the serial interface is inactive. If you want to use it, see the application note THAN-00-004.
Reserved2	34	In	Must be tied to GND.
Reserved3	49	In	Must be tied to VCC.
VCC	1,12,33	Power	Digital VCC.
GND	16,48,64	Ground	Digital GND.
AVCC	23,29	Power	Analog VCC.
AGND	20,26,32	Ground	Analog GND.
PVCC	18	Power	PLL Analog VCC.
PGND	17	Ground	PLL Analog GND.

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
TMDS Receiver Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
DC Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Lead Temperature (Soldering, 4sec)	+260°C
Maximum Power Dissipation @+25°C	1.0W

1. “Absolute Maximum Ratings” are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

Electrical Characteristics

DC Digital I/O Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage	$V_{REF} = V_{CC}$	2.0			V
V_{IL}	Low Level Input Voltage	$V_{REF} = V_{CC}$			0.8	V
V_{DDQ}[1]	Small Swing Voltage		1		1.8	V
V_{REF}	Input Reference Voltage	Small Swing	0.5	$V_{DDQ}/2$	1	V
		CMOS		V_{CC}		V
V_{SH}[2]	Small Swing High Level Input Voltage	$V_{REF} = V_{DDQ}/2$	$V_{DDQ}/2$ + 300mV			V
V_{SL}[2]	Small Swing Low Level Input Voltage	$V_{REF} = V_{DDQ}/2$			$V_{DDQ}/2$ - 100mV	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$	-10		+10	µA

Notes: [1]V_{DDQ} voltage defines max voltage of small swing input. It is not an actual input voltage.
[2] Small swing signal is apllied to D[23:0], DE,VSYNC,HSYNC and IDCLK+/-.

DC Differential Output Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OD}	Differential Voltage	R_{LOAD} = 50Ω				
	Single-ended peak to peak amplitude	R_{EXT_SWING} = 680Ω	300	330	370	mV
		R_{EXT_SWING} = 400Ω	450	510	570	mV
V_{ODH}	Differential High Level Output Voltage[1]			AVCC		V

Notes: [1]Guaranteed by design.

Supply Current

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Condition	Typ.	Max.	Units
I_{OS}	Differential Output Short Circuit Current	V_{OUT} = 0V		5	µA
I_{TCCS}[1]	Power-down Supply Current	PD = 0V		TBD	mA
I_{TCCW}	Transmitter Supply Current	DCLK = 165MHz, 1-pixel/clock mode, R_{EXT_SWING} = 400Ω, Worst Case Pattern[2]	68	77	mA

Notes: [1]Assume all inputs to the transmitter are not toggled and fixed at V_{IH} or V_{IL} level.
[2]Black and white checkerboard pattern, each checker is one pixel wide.

AC Specifications: (CMOS/TTL level I/F)

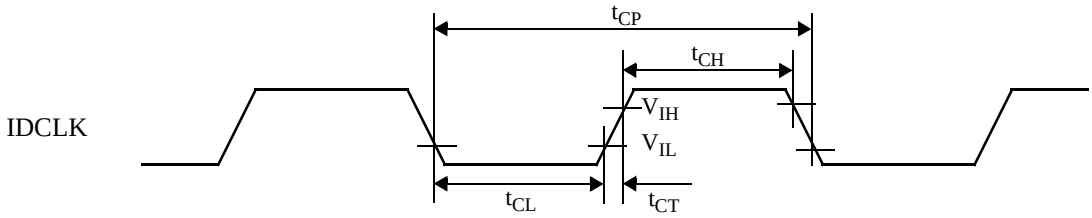
V_{CC} = 3.0V ~ 3.6V, Ta = 0 °C ~ +70 °C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{CP}	IDCLK Period		5.88		40.0	ns
t_{CH}	IDCLK High Time		2.0			ns
t_{CL}	IDCLK Low Time		2.0			ns
t_{CT}	IDCLK Transition time				5.0	ns
t_{JIT}	IDCLK Jitter				2.0	ns
t_{DFS}	Data[1] Setup to IDCLK falling edge	DSEL = 0,DKEN = 0 EDGE = 0	0.6			ns
t_{DFH}	Data[1] Hold from IDCLK falling edge	DSEL = 0,DKEN = 0 EDGE = 0	1.2			ns
t_{DRS}	Data[1] Setup to IDCLK rising edge	DSEL = 0,DKEN = 0 EDGE = 1	0.9			ns
t_{DRH}	Data[1] Hold from IDCLK rising edge	DSEL = 0,DKEN = 0 EDGE = 1	1.2			ns
t_{DS}	Data[1] Setup to IDCLK rising/falling edge	DSEL = 1,DKEN = 0 BSEL = 1,EDGE = 0	0.7			ns
t_{DH}	Data[1] Hold from IDCLK rising/falling edge	DSEL = 1,DKEN = 0 BSEL = 1,EDGE = 0	1.4			ns
t_{DDF}	V/HSYNC Delay from DE falling edge		1			t_{CP}
t_{DDR}	V/HSYNC Delay from DE rising edge		1			t_{CP}
t_{DEH}	DE High Time				8191	t_{CP}
t_{DEL}	DE Low Time[2]		128			t_{CP}
t_{SLH}	Differential Swing Low to High Transition Time[3]	C_{LOAD} = 5pF R_{LOAD} = 50Ω R_{EXT_SWING} = 400Ω	0.3	0.5	0.7	ns
t_{SHL}	Differential Swing High to Low Transition Time[3]	C_{LOAD} = 5pF R_{LOAD} = 50Ω R_{EXT_SWING} = 400Ω	0.3	0.5	0.7	ns
t_{STEP}	De-skew trim increment			200		ps
t_{TPLL}	Phase Lock Loop Setup				10.0	ms

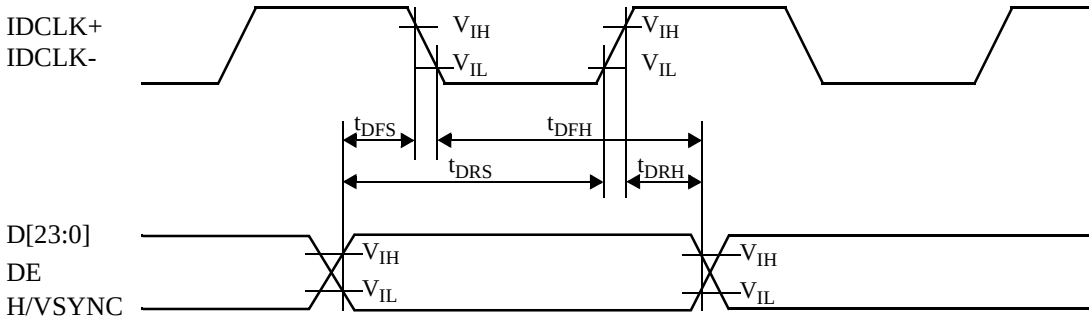
Notes: [1] Data includes D[23:0], DE, VSYNC and HSYNC.
[2] DE low time as defined as per DVI 1.0 Specification, Section 3.4
[3] On the TXC+/- outputs.

Timing Diagrams

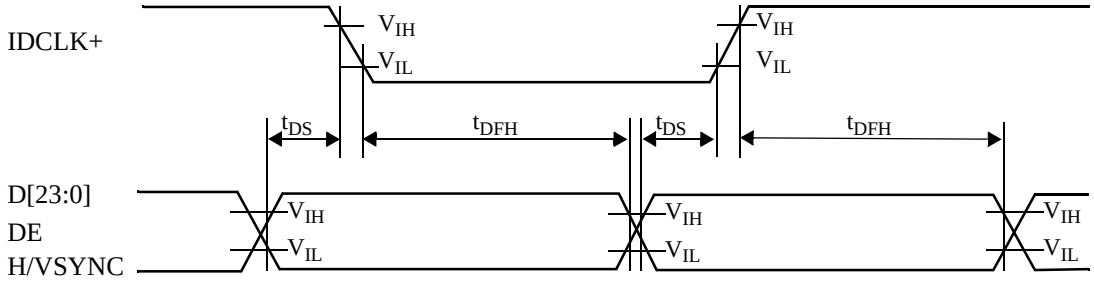
AC Timing Diagrams



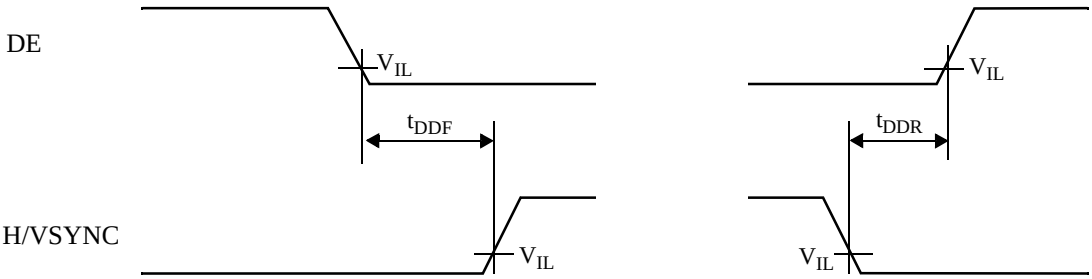
Clock Cycle and High/Low timings



Single-edge Clock to Data Setup/Hold timings

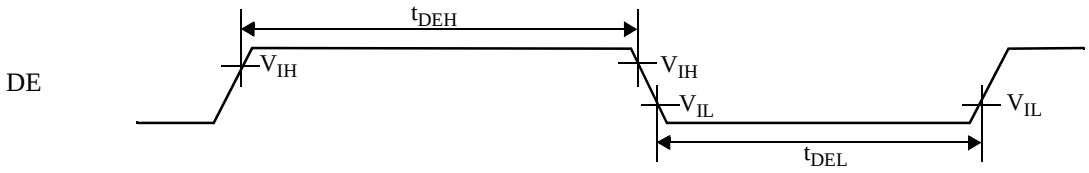


Dual-edge Clock to Data Setup/Hold timings

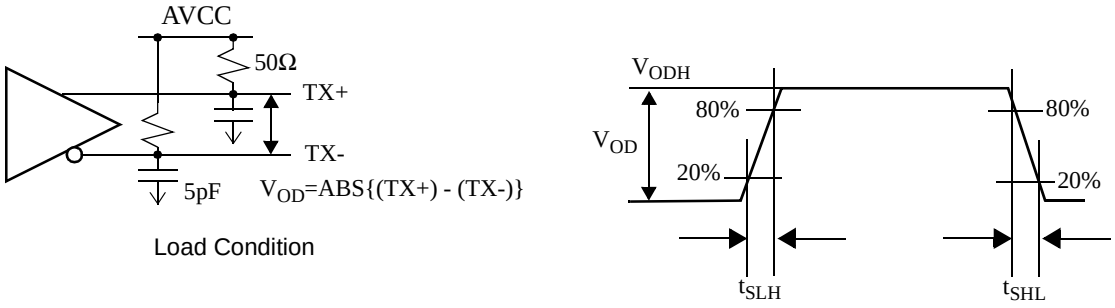


DE to H/VSYNC Delay timings

AC Timing Diagrams



DE High/Low timings



Differential Output Timings

Data Setup/Hold Trim

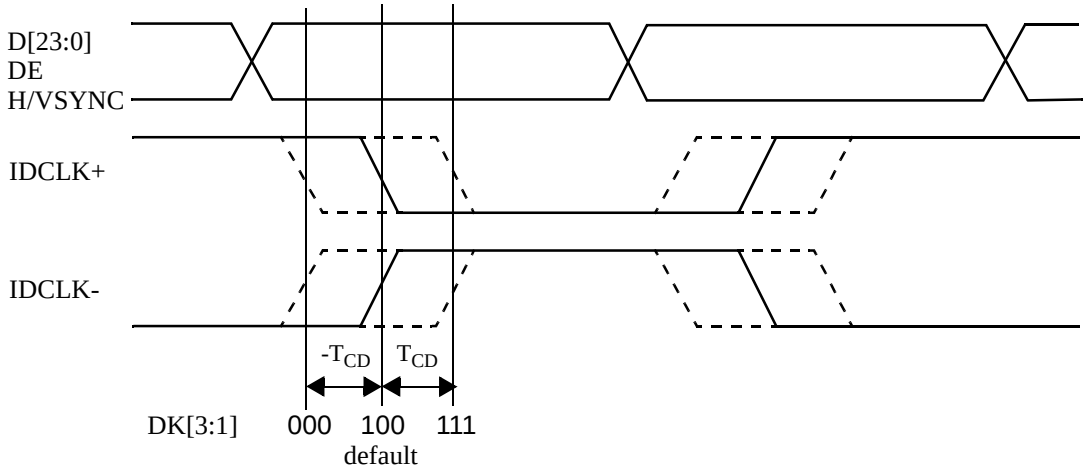
Input clock to data setup hold time can be adjusted through the use of the trim (de-skew) feature. When DKEN=High, the configuration pins DK[3:1] can be used to vary the input setup/hold time by amount T_{CD} given by the following formula.

T_{CD} = (DK[3:1] - 4) x 200p

Where

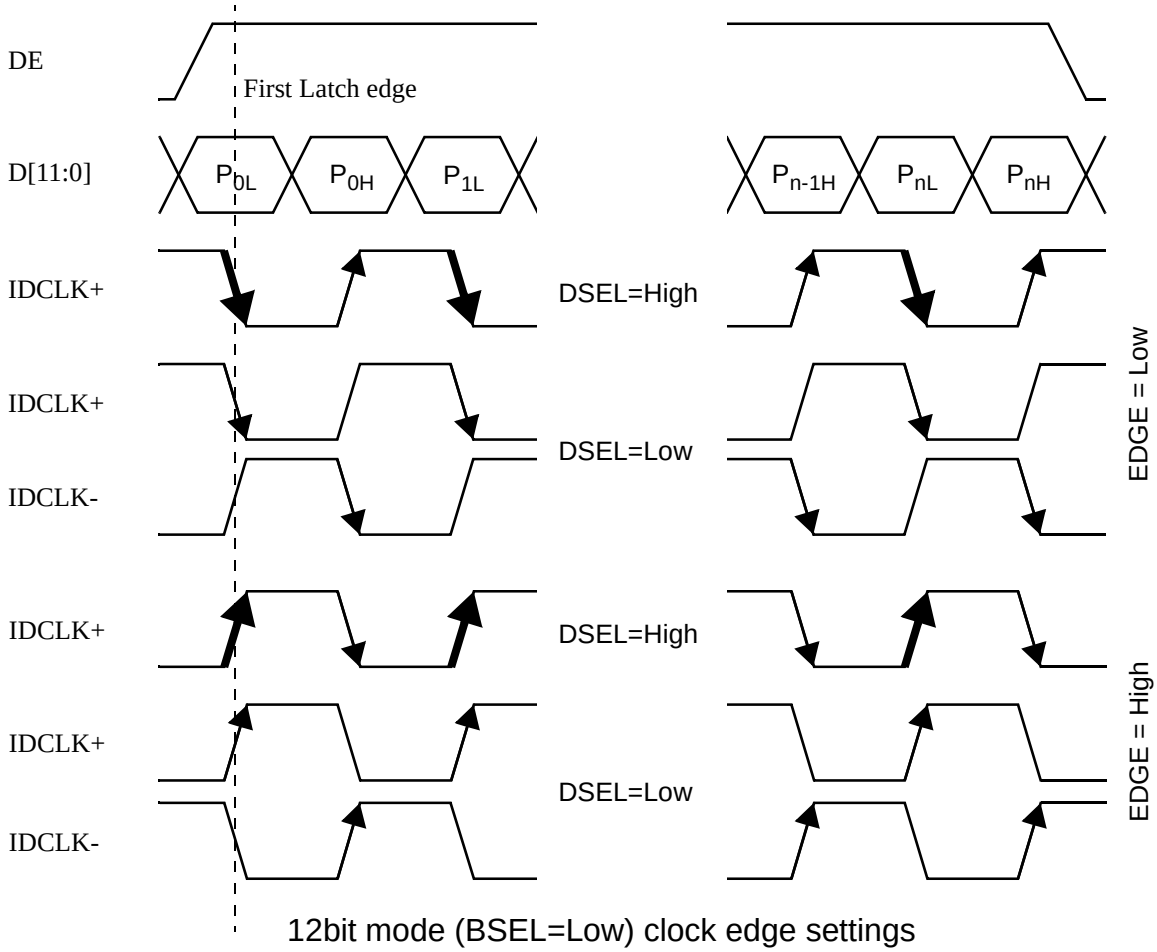
T_{CD} is the amount of setup/hold variation.
DK[3:1] is the setting of the configuration pins.

This feature can be used in both 12 and 24 bit mode.
If DKEN=LOW, the DK[3:1] input are ignored and default setting of T_{CD} = 0 is used.



Data setup/hold trimming

Data Mapping

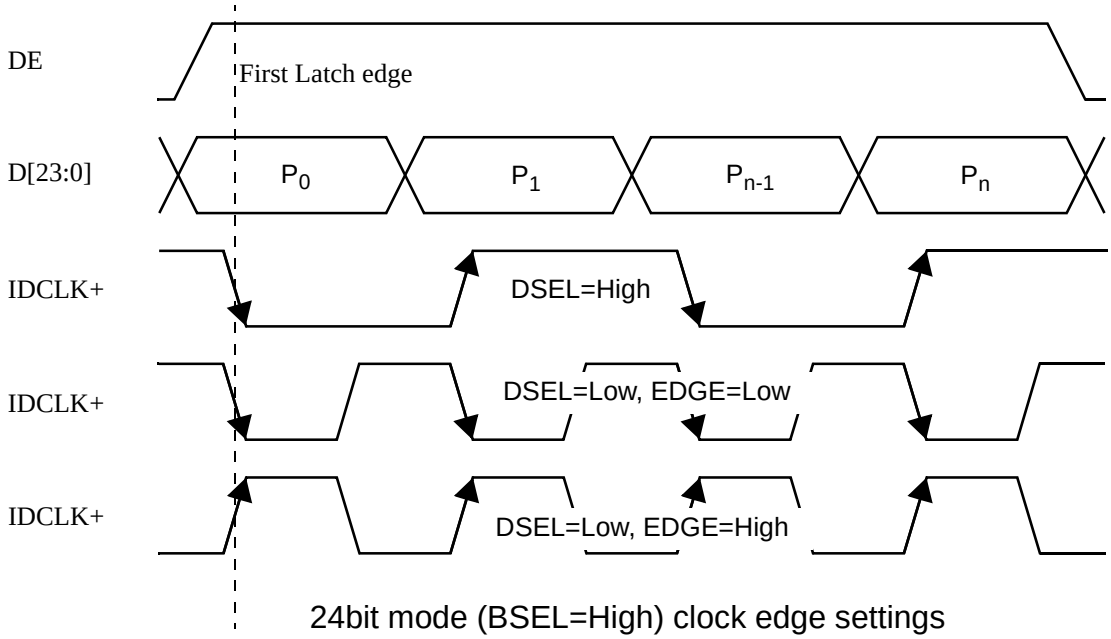


12bit mode (BSEL=Low) clock edge settings

12bit Mode Data Mapping Table

	P0		P1			Pn	
	P_{0L}	P_{0H}	P_{1L}	P_{1H}		P_{nL}	P_{0H}
	Low	High	Low	High		Low	High
D11	G0[3]	R0[7]	G1[3]	R1[7]		Gn[3]	Rn[7]
D10	G0[2]	R0[6]	G1[2]	R1[6]		Gn[2]	Rn[6]
D9	G0[1]	R0[5]	G1[1]	R1[5]		Gn[1]	Rn[5]
D8	G0[0]	R0[4]	G1[0]	R1[4]		Gn[0]	Rn[4]
D7	B0[7]	R0[3]	B1[7]	R1[3]		Bn[7]	Rn[3]
D6	B0[6]	R0[2]	B1[6]	R1[2]		Bn[6]	Rn[2]
D5	B0[5]	R0[1]	B1[5]	R1[1]		Bn[5]	Rn[1]
D4	B0[4]	R0[0]	B1[4]	R1[0]		Bn[4]	Rn[0]
D3	B0[3]	G0[7]	B1[3]	G1[7]		Bn[3]	Gn[7]
D2	B0[2]	G0[6]	B1[2]	G1[6]		Bn[2]	Gn[6]
D1	B0[1]	G0[5]	B1[1]	G1[5]		Bn[1]	Gn[5]
D0	B0[0]	G0[4]	B1[0]	G1[4]		Bn[0]	Gn[4]

Notes: [1]In this figure, clock edges represented by arrows signify latching edge. Primary latch edge is indicated by bold arrow, which latches the lower half of pixel (L) data.
[2]Color pixel components are represented as R:Red, G:Green and B:Blue.
[3]Bit significance with in a color: [7:0] = [MSB:LSB]



24bit mode (BSEL=High) clock edge settings

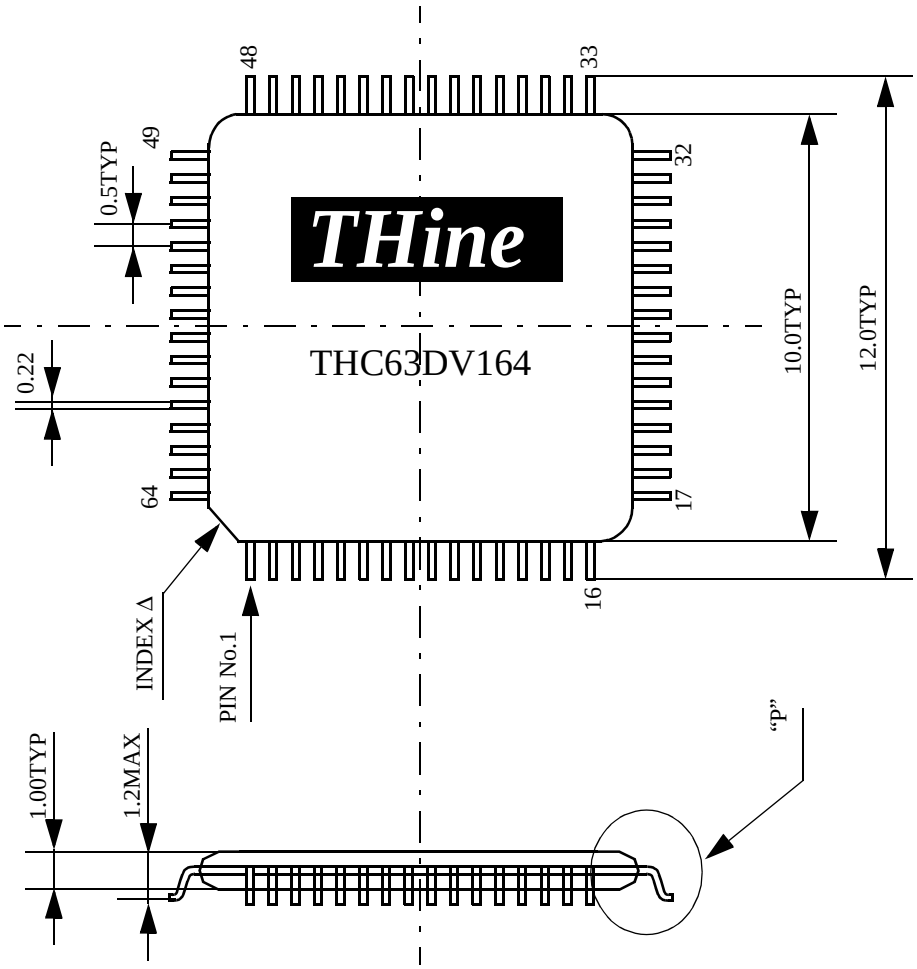
Notes: In 24 bit Single Clock Dual Edge mode, the THC63DV164 will look at the first clock edge (either falling or rising) after DE goes high to determine the first pixel data. EDGE pin has no affect in 24 bit Single Clock Dual Edge mode.

24bit Mode Data Mapping Table

	P0	P1		Pn
D23	R0[7]	R1[7]		Rn[7]
D22	R0[6]	R1[6]		Rn[6]
D21	R0[5]	R1[5]		Rn[5]
D20	R0[4]	R1[4]		Rn[4]
D19	R0[3]	R1[3]		Rn[3]
D18	R0[2]	R1[2]		Rn[2]
D17	R0[1]	R1[1]		Rn[1]
D16	R0[0]	R1[0]		Rn[0]
D15	G0[7]	G1[7]		Gn[7]
D14	G0[6]	G1[6]		Gn[6]
D13	G0[5]	G1[5]		Gn[5]
D12	G0[4]	G1[4]		Gn[4]
D11	G0[3]	G1[3]		Gn[3]
D10	G0[2]	G1[2]		Gn[2]
D9	G0[1]	G1[1]		Gn[1]
D8	G0[0]	G1[0]		Gn[0]
D7	B0[7]	B1[7]		Bn[7]
D6	B0[6]	B1[6]		Bn[6]
D5	B0[5]	B1[5]		Bn[5]
D4	B0[4]	B1[4]		Bn[4]
D3	B0[3]	B1[3]		Bn[3]
D2	B0[2]	B1[2]		Bn[2]
D1	B0[1]	B1[1]		Bn[1]
D0	B0[0]	B1[0]		Bn[0]

Notes: [1]In this figure, clock edges represented by arrows signify latching edge.
[2]Color pixel components are represented as R:Red, G:Green and B:Blue.
[3]Bit significance with in a color: [7:0] = [MSB:LSB]

Package



UNITS: mm

Notes to Users:

1. The contents of this data sheet are subject to change without prior notice.
2. Circuit diagrams shown in this data sheet are examples of application. Therefore, please pay sufficient attention when designing circuits. Even if there are incorrect descriptions, we are not responsible for any problem due to them. Please note that incorrect descriptions sometimes cannot be corrected immediately if found.
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4. We are not responsible for any problems of industrial proprietorship occurring during THC63DV164 use, except for those directly related to THC63DV164's structure, manufacture or functions. THC63DV164 is designed on the premise that it should be used for ordinary electronic devices. Therefore, it shall not be used for applications that require extremely high-reliability (space equipment, nuclear control equipment, medical equipment that affects people's lives, etc.). In addition, when using THC63DV164 for traffic signals, safety devices and control/safety units in transportation equipment, etc., appropriate measures should be taken.
5. We are making the utmost effort to improve the quality and reliability of our products. However, there is a very slight possibility of failure in semiconductor devices. To avoid damage to social or official organizations, much care should be taken to provide sufficient redundancy and fail-safe design.
6. No radiation-hardened design is incorporated in THC63DV164.
7. Judgment on whether THC63DV164 comes under strategic products prescribed by the Foreign Exchange and Foreign Trade Control Law is the user's responsibility.
8. This technical document was provisionally created during development of THC63DV164, so there is a possibility of differences between it and the product's final specifications. When designing circuits using THC63DV164, be sure to refer to the final technical documents.
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THine Electronics, Inc.
1-10-7, 6F, Hatchobori,
Chuo-ku, Tokyo, 104-0032 Japan
Tel: 81-3-3555-0666
Fax: 81-3-3555-0677

