



**P-Channel Enhancement-Mode  
Vertical DMOS FETs**

**Ordering Information**

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package			
				TO-39	TO-92	TO-243AA*	Die†
-20V	4.0Ω	-2.4V	-0.85A	—	TP0102N3	—	TP0102ND
-40V	4.0Ω	-2.4V	-0.85A	TP0104N2	TP0104N3	TP0104N8	TP0104ND

\* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

† MIL visual screening available

**Features**

- Low threshold — 2.4V max.
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

**Low Threshold DMOS Technology**

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

**Applications**

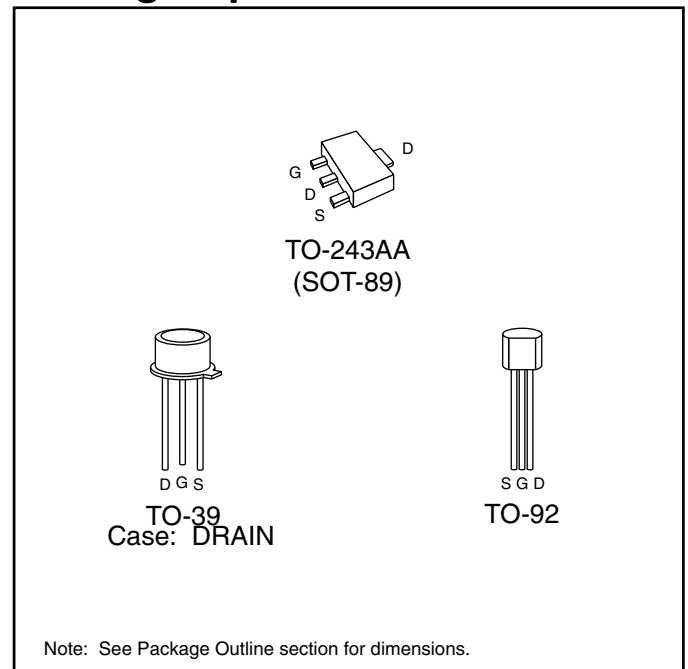
- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

**Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* For TO-39 and TO-92, distance of 1.6 mm from case for 10 seconds.

**Package Options**



# Thermal Characteristics

Package	I <sub>D</sub> (continuous)*	I <sub>D</sub> (pulsed)	Power Dissipation @ T <sub>C</sub> = 25°C	θ <sub>jc</sub> °C/W	θ <sub>ja</sub> °C/W	I <sub>DR</sub> *	I <sub>DRM</sub>
TO-39	-0.9A	-2.0A	3.5W	35	125	-0.90A	-2.0A
TO-92	-0.5A	-2.0A	1.0W	125	170	-0.50A	-2.0A
TO-243AA	-0.26A	-2.0A	1.6W	15	78†	-0.26A	-2.0A

\* I<sub>D</sub> (continuous) is limited by max rated T<sub>j</sub>.

† T<sub>A</sub> = 25°C. Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P<sub>D</sub> increase possible on ceramic substrate.

**TP0104  
OBSOLETE -**

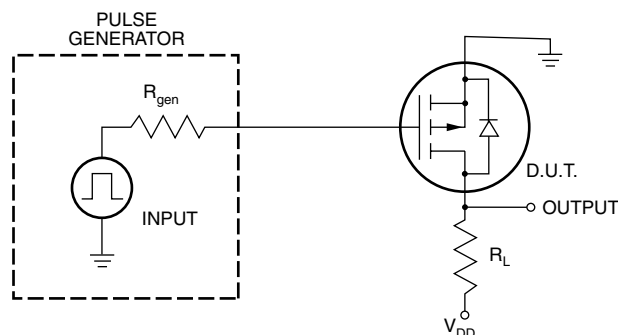
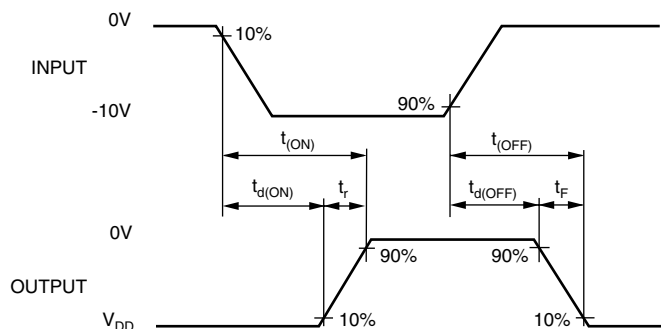
# Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	TP0104	-40			V <sub>GS</sub> = 0V, I <sub>D</sub> = -1.0mA
		TP0102	-20			
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0		-2.4	V	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1.0mA
ΔV <sub>GS(th)</sub>	Change in V <sub>GS(th)</sub> with Temperature		-5.8	-6.5	mV/°C	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1.0mA
I <sub>GSS</sub>	Gate Body Leakage		-1.0	-100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current			-10	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = Max Rating
				-1	mA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0.8 Max Rating T <sub>A</sub> = 125°C
I <sub>D(ON)</sub>	ON-State Drain Current		-0.08		A	V <sub>GS</sub> = -3V, V <sub>DS</sub> = -20V
		-0.25	-0.50	V <sub>GS</sub> = -5V, V <sub>DS</sub> = -20V		
		-0.85	-1.70	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -20V		
R <sub>DS(ON)</sub>	Static Drain-to-Source ON-State Resistance		15		Ω	V <sub>GS</sub> = -3V, I <sub>D</sub> = -25mA
			4.7	7.5		V <sub>GS</sub> = -5V, I <sub>D</sub> = -0.1A
			2.5	4.0		V <sub>GS</sub> = -10V, I <sub>D</sub> = -0.5A
ΔR <sub>DS(ON)</sub>	Change in R <sub>DS(ON)</sub> with Temperature		0.55	1.0	%/°C	V <sub>GS</sub> = -10V, I <sub>D</sub> = -0.5A
G <sub>FS</sub>	Forward Transconductance	225	250		mS	V <sub>DS</sub> = -20V, I <sub>D</sub> = -0.5A
C <sub>ISS</sub>	Input Capacitance			60	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -20V f = 1 MHz
C <sub>OSS</sub>	Common Source Output Capacitance			50		
C <sub>RSS</sub>	Reverse Transfer Capacitance			25		
t <sub>d(ON)</sub>	Turn-ON Delay Time		4.0	6.0	ns	V <sub>DD</sub> = -20V, I <sub>D</sub> = -0.85A R <sub>GEN</sub> = 25Ω
t <sub>r</sub>	Rise Time		7.0	10		
t <sub>d(OFF)</sub>	Turn-OFF Delay Time		3.0	9.0		
t <sub>f</sub>	Fall Time		4.0	13		
V <sub>SD</sub>	Diode Forward Voltage Drop		-1.2	-2.0	V	I <sub>SD</sub> = -0.25A, V <sub>GS</sub> = 0V
t <sub>rr</sub>	Reverse Recovery Time		300		ns	I <sub>SD</sub> = -0.25A, V <sub>GS</sub> = 0V

**Notes:**

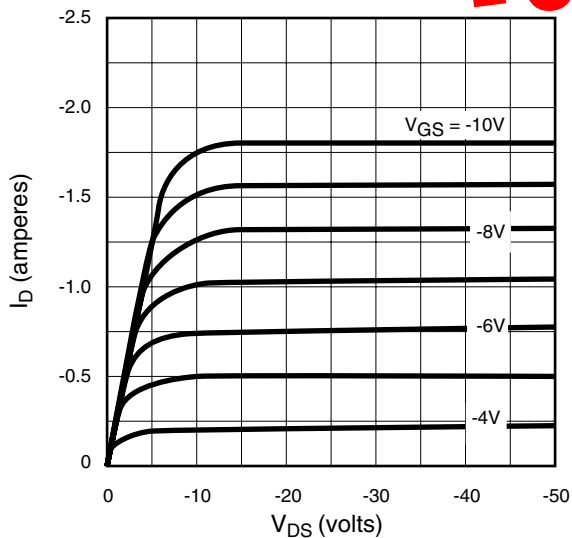
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

# Switching Waveforms and Test Circuit

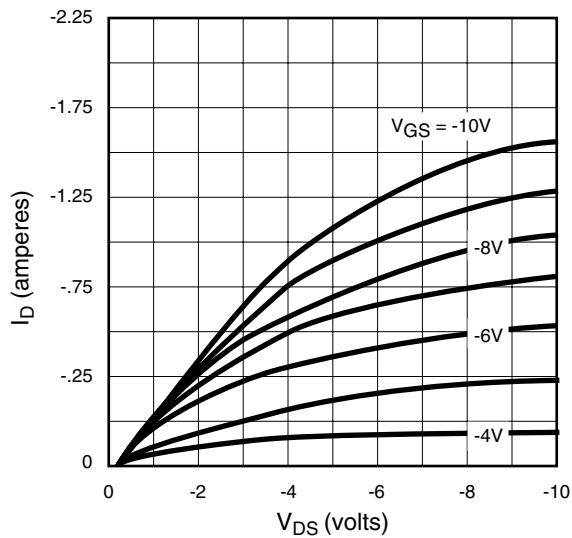


# Typical Performance Curves **TP0104** **- OBSOLETE -**

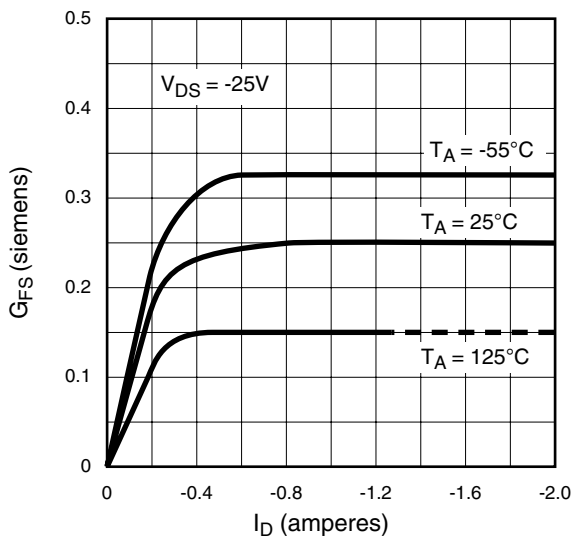
Output Characteristics



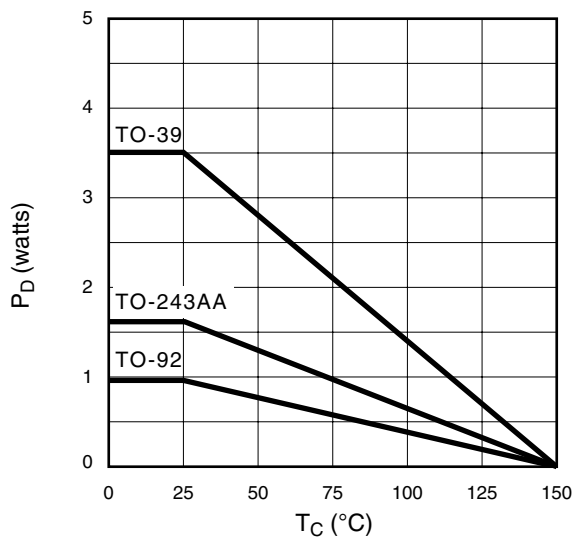
Saturation Characteristics



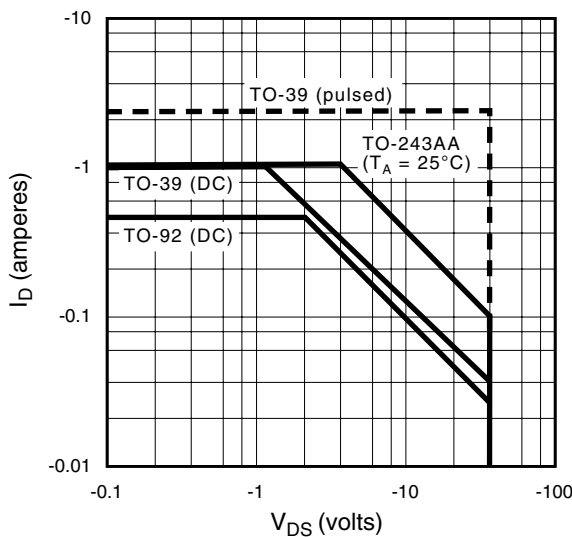
Transconductance vs. Drain Current



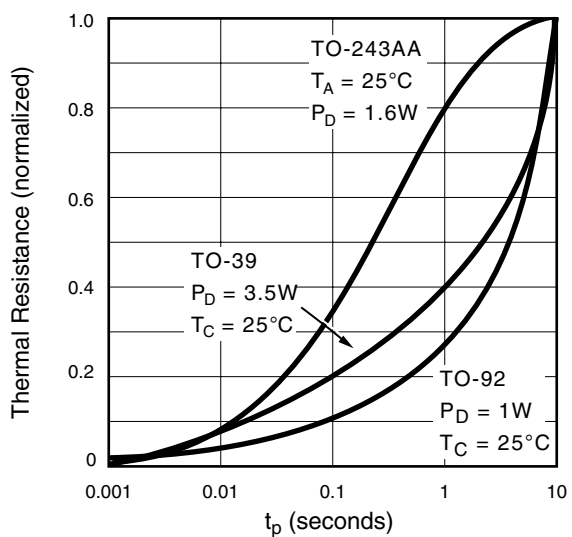
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



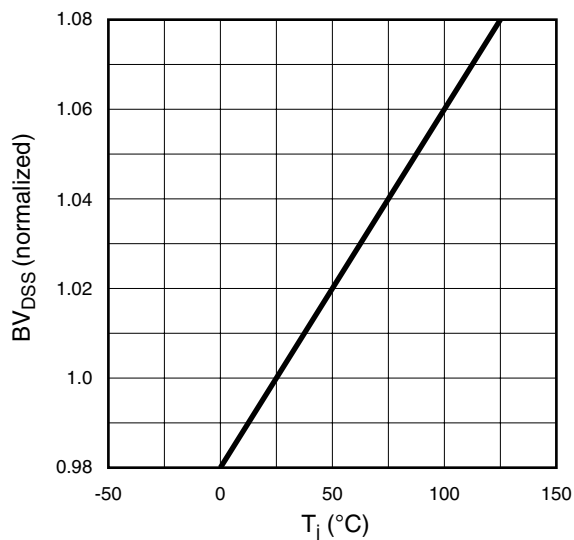
Thermal Response Characteristics



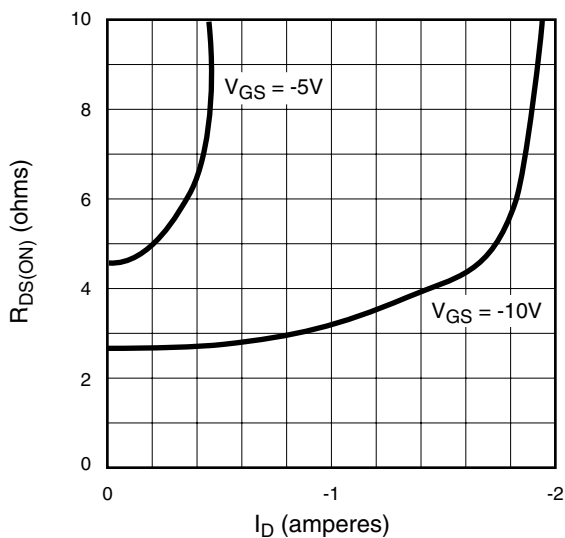
# Typical Performance Curves

**TP0104  
OBSOLETE -**

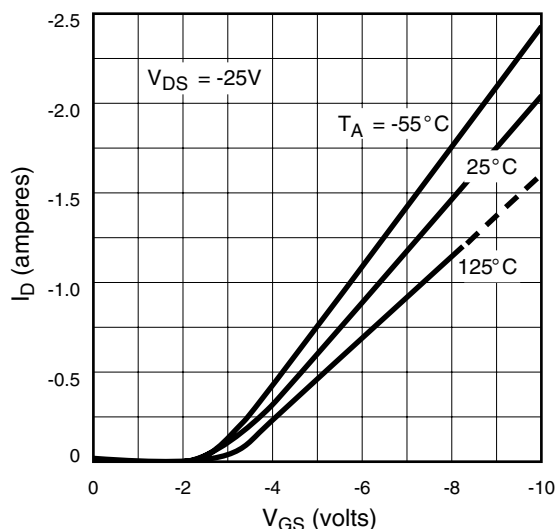
BV<sub>DSS</sub> Variation with Temperature



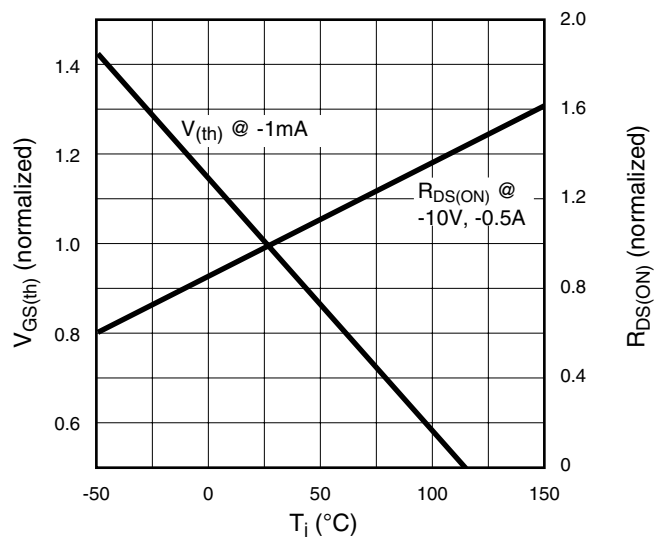
On-Resistance vs. Drain Current



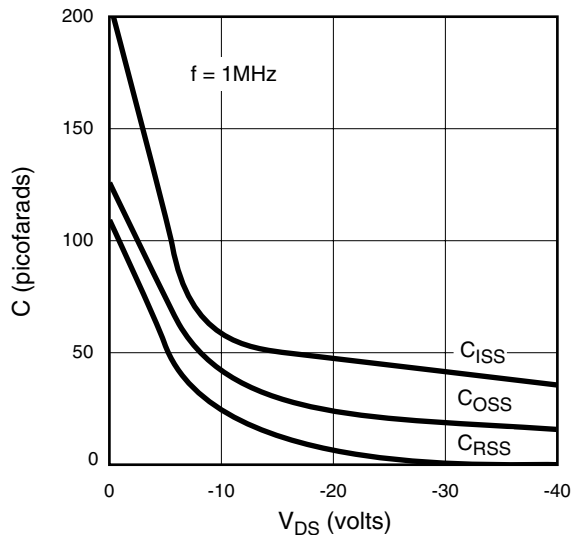
Transfer Characteristics



V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

