TPS7H1x01 1.5-V to 7-V, Ultra-Low Dropout (LDO) Regulator

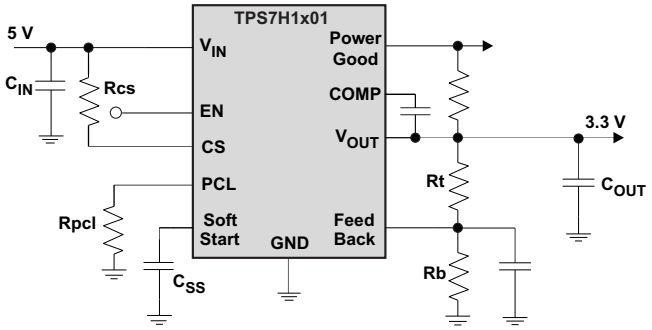
1 Features

- Wide V_{IN} Range: 1.5 to 7 V
- Current Share/Parallel Operation to Provide Higher Output Current
- 5962R13202:
  - Radiation Hardness Assurance (RHA) up to TID 100 krad (Si)
  - Total Ionizing Dose 100 krad (Si)
  - ELDRS-Free 100 krad (Si)
  - Dose Rate 10 mRAD(si)/s
  - Single Event Latchup (SEL) Immune to LET = 85 MeV-cm^2/mg
  - SEB and SEGR Immune to LET = 85 MeV-cm^2/mg
  - SET/SEFI Onset Threshold is 40 MeV-cm^2/mg, See *Radiation Report* for Details
  - SET/SEFI Cross-Section Plot, See *Radiation Report* for Details
- Stable With Ceramic Output Capacitor
- ±2.0% Accuracy over Line, Load, and Temperature (TPS7H1101-SP)
- ±4.2% Accuracy over Line, Load, and Temperature (TPS7H1201-HT)
- Programmable Soft-Start
- PowerGood Output
- LDO Voltage **TPS7H1201-HT**: 100 mV (MAX) at 0.5 A (210°C), V_{OUT} = 6.8 V
- LDO Voltage **TPS7H1101-SP**: 62 mV at 1 A (25°C), V_{OUT} = 1.8 V
- Low Noise **TPS7H1201-HT**: 20.26 µVRMS V_{IN} = 2.1 V, V_{OUT} = 1.8 V at 0.5 A
- Low Noise **TPS7H1101-SP**: 20.33 µVRMS V_{IN} = 2 V, V_{OUT} = 1.8 V at 3 A
- PSRR: Over 45 dB at 1 kHz
- Load/Line Transient Response
- Fold-Back Current Limit (TPS7H1101-SP)

2 Applications

- TPS7H1101-SP: Rad-Tolerant Applications
- RF 5-V Components VCOs, Receivers, ADCs, Amplifiers
- Clock Distribution
- Clean Analog Supply Requirements
- Supports Harsh Environment Applications
- TPS7H1201-HT Available in Extreme (–55°C to 210°C) Temperature Range
  TPS7H1101-SP Available in Military (–55°C to 125°C) Temperature Range (1)
- TPS7H1201-HT: TI's High Temperature Products Use Highly-Optimized Silicon (Die) Solutions With Design and Process Enhancements to Maximize Performance over Extended Temperatures.
- Engineering Evaluation (/EM) Samples are Available (2)

Typical Application Circuit



3 Description

The TPS7H1x01 is a LDO linear regulator that uses a PMOS pass element configuration. It operates under a wide range of input voltage, from 1.5 to 7 V while offering excellent PSRR. The TPS7H1x01 features a precise and programmable fold back current limit implementation with a very-wide adjustment range. To support the complex power requirements of FPGAs, DSPs, or microcontrollers, the TPS7H1x01 provides enable on/off functionality, programmable SoftStart, current sharing capability, and a PowerGood open-drain output. The TPS7H1x01 is available in a thermally-enhanced 16-pin ceramic flatpack package (CFP) and KGD (bare die) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7H1201-HT	HKS (16)	11.00 mm × 9.60 mm
TPS7H1101-SP	HKR (16)	11.00 mm × 9.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(1) Custom temperature ranges are available
(2) These units are intended for engineering evaluation only. They are processed to a noncompliant flow (that is, no burn-in, and so forth) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2014) to Revision H **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision F (October 2013) to Revision G **Page**

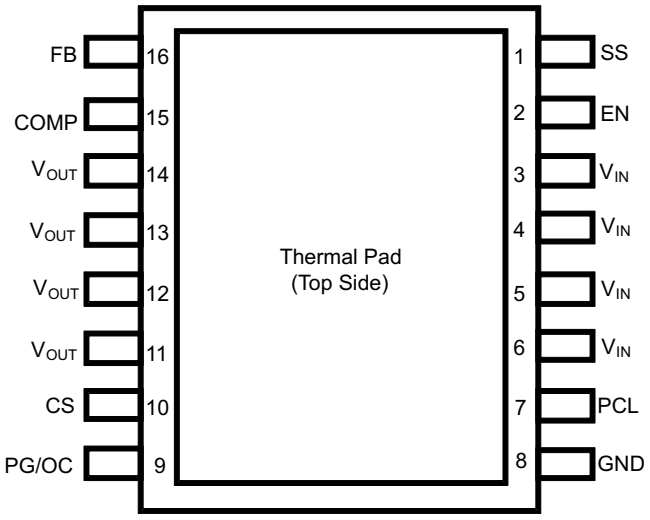
- Added Bare Die Information ... 5

5 Device Comparison Table

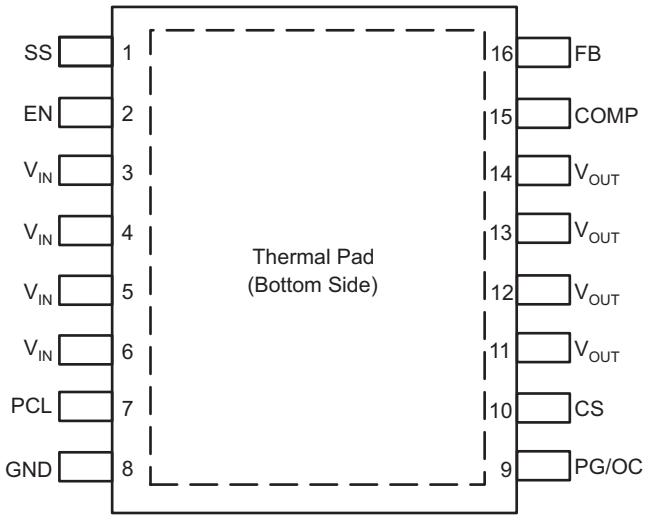
PART NUMBER	LDO VOLTAGE	LOW-NOISE
TPS7H1201-HT	• 100 mV (MAX) at 0.5 A (210°C) , V_{OUT} = 6.8 V	• 20.26 µVRMS (V_{IN} = 2.1 V, V_{OUT} = 1.8 V at 0.5 A) • 31.0 µVRMS (V_{IN} = 7 V, V_{OUT} = 6.7 V at 0.5 A)
TPS7H1101-SP	• 62 mV at 1 A (25°C), V_{OUT} = 1.8 V • 125 mV at 2 A (25°C), V_{OUT} = 1.8 V • 196 mV at 3 A (25°C), V_{OUT} = 1.8 V • 210 mV at 3 A (25°C), V_{OUT} = 1.3 V • 335 mV (MAX) at 3 A (125°C) , V_{OUT} = 1.3 V	• 20.33 µVRMS (V_{IN} = 2 V, V_{OUT} = 1.8 V at 3 A) • 31.68 µVRMS (V_{IN} = 7 V, V_{OUT} = 6.7 V at 3 A)

6 Pin Configuration and Functions

HKS Package
(Top View)



HKR Package
(Top View)



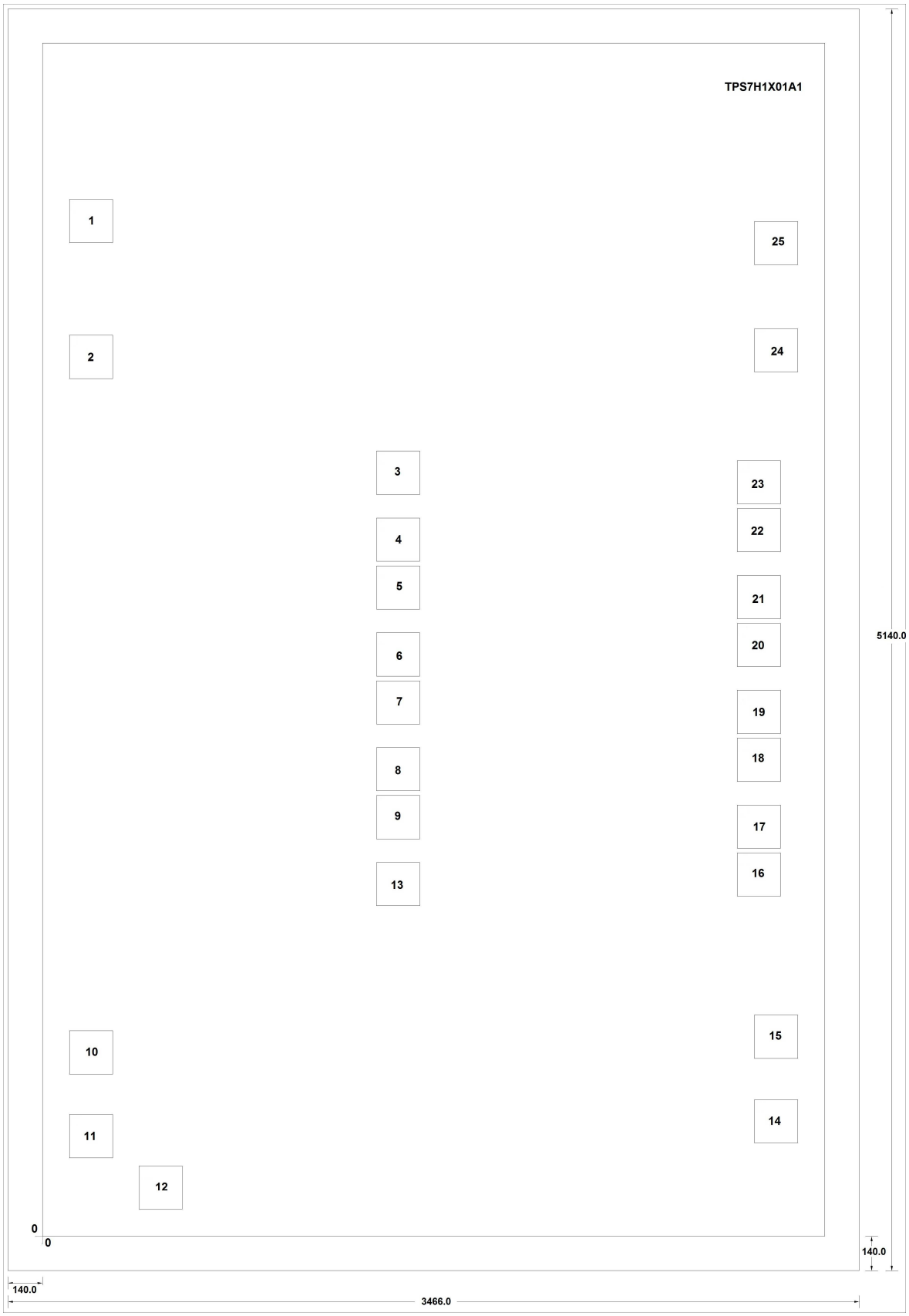
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SS	1		Soft-Start terminal. Connecting an external capacitor slows down the output voltage ramp rate after enable event. The Soft-Start terminal can be used to disable the device as described in *Soft-Start*.
EN	2		Enable terminal. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device; V_{IN} voltage must be greater than 3.5 V. For V_{IN} < 3.5 V, enable terminal cannot be used to disable the device. TI recommends to connect the enable terminal to V_{IN}.
V_{IN}	3		Unregulated supply voltage. TI recommends to connect an input capacitor as a good analog circuit practice.
	4		
	5		
	6		
PCL	7		Programmable current limit. A resistor to GND sets the overcurrent limit activation point. The range of resistor that can be used on the PCL terminal to GND is 47 to 160 kΩ (TPS7H1201-HT). The range of resistor that can be used on the PCL terminal to GND is 8.2 to 160 kΩ (TPS7H1101-SP).
GND	8	—	Ground/thermal pad(1)
PG/OC	9		PowerGood terminal. PG is an open-drain output to indicate the output voltage reaches 90% of target. PG terminal is also used as indicator when an overcurrent condition is activated.
CS	10		Current sense terminal. Resistor connected from CS to V_{IN}. CS terminal indicates voltage proportional to output current. CS terminal low: Foldback current limit disabled (applies for TPS7H1101-SP only) CS terminal high: Foldback current limit enabled (applies for TPS7H1101-SP only)
V_{OUT}	11		Regulated output
	12		
	13		
	14		
COMP	15		Output of error amplifier
FB	16		The output voltage feedback input through voltage dividers. See *Adjustable Output Voltage (Feedback Circuit)*.

(1) Thermal Pad must be connected to GND

Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Ground	AlCu	30 kA



NOTE: All dimensions are in microns.

Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
SS	1	109.89	4046.805	287.19	4224.105
EN	2	109.89	3493.35	287.19	3670.65
VIN	3	1359.99	3021.345	1537.29	3198.645
VIN	4	1359.99	2749.005	1537.29	2926.305
VIN	5	1359.99	2553.705	1537.29	2731.005
VIN	6	1359.99	2281.365	1537.29	2458.665
VIN	7	1359.99	2086.065	1537.29	2263.365
VIN	8	1359.99	1813.725	1537.29	1991.025
VIN	9	1359.99	1618.425	1537.29	1795.725
PCL	10	109.89	660.285	287.19	837.585
GND	11	109.89	319.455	287.19	496.755
N/C	12	392.58	109.935	569.88	287.235
VIN	13	1359.99	1346.085	1537.29	1523.385
PG/OC	14	2898.945	379.62	3076.245	556.92
CS	15	2898.945	724.32	3076.245	901.62
VOUT	16	2829.105	1384.695	3006.405	1561.995
VOUT	17	2829.105	1579.815	3006.405	1757.115
VOUT	18	2829.105	1852.335	3006.405	2029.635
VOUT	19	2829.105	2047.455	3006.405	2224.755
VOUT	20	2829.105	2319.975	3006.405	2497.275
VOUT	21	2829.105	2515.095	3006.405	2692.395
VOUT	22	2829.105	2787.615	3006.405	2964.915
VOUT	23	2829.105	2982.735	3006.405	3160.035
COMP	24	2898.945	3519.72	3076.245	3697.02
FB	25	2898.945	3956.535	3076.245	4133.835

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	V_{IN}, PG	–0.3	7.5	V
	FB, COMP, PCL, CS, EN	–0.3	V_{IN} + 0.3	V
Output voltage	V_{OUT} , SS	–0.3	V_{IN}	V
Peak output current		Internally limited		A
PG terminal sink current		0.001	5	mA
Maximum operating junction temperature, T_J	TPS7H1201	–55	220	°C
	TPS7H1101	–55	150	
Storage temperature, T_{stg}	TPS7H1201	–55	220	°C
	TPS7H1101	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	TPS7H1201-HT	–55		210	°C
		TPS7H1101-SP	–55		125	

7.4 Thermal Information (1)(2)(3)

THERMAL METRIC (4)		HKS (HeatSlug_up_no Underfill) (5)	HKR (HeatSlug_down Underfill) (6)(7)	HKR (HeatSlug_down_no Underfill)	UNIT
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (8)	75.4	30.7	86.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (9)	0.4	N/A	N/A	
$R_{\theta JB}$	Junction-to-board thermal resistance (10)	4.8	69	59.3	
ψ_{JT}	Junction-to-top characterization parameter (11)	1.1	2.4	5	
ψ_{JB}	Junction-to-board characterization parameter (12)	53.5	12.3	63.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (13)	N/A	0.6	0.6	

(1) Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.
(2) Maximum power dissipation may be limited by overcurrent protection.
(3) Test board conditions:
  (a) 2.5 inches × 2.5 inches, 4 layers, thickness: 0.062 inch
  (b) 2-oz. copper traces located on the top of the PCB
  (c) 2-oz. copper ground planes on the 2 internal layers and bottom layer
  (d) 48 (0.010-inch) thermal vias located under the device package
(4) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(5) Power rating at a specific ambient temperature T_A should be determined with a junction temperature below 220°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 220°C for best performance and long-term reliability.
(6) Power rating at a specific ambient temperature T_A should be determined with a junction temperature below 135°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 230°C for best performance and long-term reliability.
(7) Values listed in the underfill column were derived using properties from a composite, generic silver filled epoxy underfill. They are not product specific.
(8) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(9) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(10) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(11) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(12) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(13) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics for TPS7H1201

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.3 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 210°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			1.5		7	V
V_{FB}	Feedback terminal voltage	1.5 V ≤ V_{IN} ≤ 7 V	T_J = 125°C	0.593	0.605	0.617	V
			T_J = 210°C	0.580	0.605	0.630	V
V_{OUT}	Output voltage range			0.8		V_{IN} – 0.2	V
	Output voltage accuracy	I_{OUT} ≤ 0.5 A, 1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 6.8 V(1)	T_J = 125°C	–2%		2%	
			T_J = 210°C	–4.2%		4.2%	
ΔV_{OUT}%/ ΔV_{IN}	Line regulation	1.5 V ≤ V_{IN} ≤ 7 V		-0.07	0.01	0.07	%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation	0.8 V ≤ V_{OUT} ≤ 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A			0.0125		%/A
ΔV_O	DC input line regulation	1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = -55°C(2)			0.5	3	mV
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 25°C(2)			0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 125°C(2)			0.2	1	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 210°C(2)			0.84	3	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = -55°C(2)			0.5	3	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 25°C(2)			0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 125°C(2)			0.2	1	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 210°C(2)			0.84	3	
ΔV_O	DC output load regulation	V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = -55°C(2)			0.05		mV
		V_{OUT} = 0.8 V, 0 ≤I_{Load} ≤ 0.5 A, T_J = 25°C(2)			0.05		
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 125°C(2)			0.07		
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 210°C(2)			0.51		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = -55°C(2)			0.10		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 25°C(2)			0.04		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 125°C(2)			0.05		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 210°C(2)			0.47		
V_{DO}	Dropout voltage	I_{OUT} = 0.5 A, V_{OUT} = 6.8 V, V_{IN} = V_{OUT} + 0.1 V			55.5	100	mV
I_{CL}	Programmable output current limit range	V_{IN} = 1.5 V, V_{OUT} = 1.2 V, PCL resistance = 47 kΩ		500		700	mA
		V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance varies		200		700	mA
V_{CS}	Operating voltage range at CS			0.3		V_{IN}	V
CSR	Current sense ratio	I_{LOAD} / I_{CS}, V_{IN} = 2.3 V, V_{OUT} = 1.9 V			47394		
I_{GND}	GND terminal current	V_{IN} = 1.5V, V_{OUT} = 1.2 V, I_{OUT} = 0.5 A			13	20	mA
I_Q	Quiescent current (no load)	V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 0 A			12	17	mA
I_{SHDN}	Shutdown current	V_{EN} < 0.5 V, 0.8 V ≤ V_{IN} ≤ 7 V			15	4500	µA
I_{SNS}, I_{FB}	FB/SNS terminal current	V_{IN} = 7 V, V_{OUT} = 6.8 V			1	10	nA
I_{EN}	EN terminal input current	V_{IN} = 7 V, V_{EN} = 7 V			6.75	610	nA
V_{ILEN}	EN terminal input low (disable)				0.30 × V_{IN}		V
V_{IHEN}	EN terminal input high (enable)				0.75 × V_{IN}		V

(1) Based upon using 0.1% resistors.
(2) Line and load regulations done under pulse condition for T < 10 ms.

Electrical Characteristics for TPS7H1201 (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.3 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 210°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Eprop Dly	Enable terminal propagation delay	V_{IN} = 2.2 V, EN rise to I_{OUT} rise			650	1000	µs
T_{EN}	Enable terminal turn-on delay	V_{IN} = 2.2 V, V_{OUT} = 1.8 V, I_{LOAD} = 0.5 A, C_{OUT} = 220 µF, C_{SS} = 2 nF			1.4	1.6	ms
V_{THPG}	PG threshold on	No load,V_{OUT} = 1.2 V and V_{OUT} = 6.8 V		84%	90%		
$V_{THPGHYS}$	PG hysteresis	1.5 V ≤ V_{IN} ≤ 7 V			2%		
V_{OLPG}	PG terminal output low	I_{PG} = 0 to –1 mA			73	300	mV
I_{LKGPG}	PG terminal leakage current	V_{OUT} > V_{THPG}, V_{PG} = 7 V			0.02	20	µA
I_{SS}	SS terminal current	V_{IN} = 1.5 to 7 V			2.5	6.3	µA
I_{SSdisb}	SS terminal disable current	V_{IN} = 1.5 to 7 V			5	13	µA
V_{SS}	SS terminal voltage (device enabled)(3)	V_{IN} = 1.5 to 7 V				1.2	V
PSRR	Power-supply rejection ratio	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, C_{OUT} = 220 µF	1 kHz		45		dB
			100 kHz		20		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 500 mA, V_{IN} = 2 V, V_{OUT} = 1.8 V			20.26		$µV_{RMS}$
T_J	Operating junction temperature			–55		210	°C

(3) Any external pullup voltage should not exceed 1.188 V.

7.6 Electrical Characteristics for TPS7H1101

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.5		7	V
V_{FB}	Feedback terminal voltage(1)(1)	0 A ≤ I_{OUT} ≤ 3 A, 1.5 V ≤ V_{IN} ≤ 7 V	0.594	0.605	0.616	V
V_{OUT}	Output voltage range		0.8		V_{IN} – 0.35	V
	Output voltage accuracy(1)	0 A ≤ I_{OUT} ≤ 3 A, 1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, 6.65 V(2)	–2%		2%	
ΔV_{OUT}%/ ΔV_{IN}	Line regulation	1.5 V ≤ V_{IN} ≤ 7 V	-0.07	0.01	0.07	%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation	0.8 V ≤ V_{OUT} ≤ 6.65 V, 0 ≤ I_{Load} ≤ 3 A		0.08		%/A
ΔV_I	DC input line regulation	1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = –55°C(3)		0.5	3	mV
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 25°C(3)		0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 125°C(3)		0.2	1.0	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = –55°C(3)		0.5	3.0	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 25°C(3)		0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 125°C(3)		0.2	1.0	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, T_J = –55°C(3)		0.5	3.0	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, T_J = 25°C(3)		0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, T_J = 125°C(3)		0.2	1.0	

(1) The output voltage accuracy of condition at I_{OUT} = 2 A and I_{OUT} = 3 A is specified by characterization, but not production tested.
(2) Based upon using 0.1% resistors.
(3) Line and load regulations done under pulse condition for t < 10 ms.

Electrical Characteristics for TPS7H1101 (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_O	DC output load regulation(4)	V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(3)		0.4	1.0	mV
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(3)		0.6	1.1	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(3)		0.8	1.3	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(3)		0.8	1.8	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(3)		1.3	1.8	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(3)		1.6	2.4	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(3)		1.1	1.9	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(3)		1.9	2.6	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(3)		2.5	3.4	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(3)		0.3	1.2	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(3)		0.5	1.3	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(3)		0.6	1.3	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(3)		0.8	1.6	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(3)		1.1	2.1	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(3)		1.5	2.1	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(3)		1.0	1.7	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(3)		1.1	2.4	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(3)		2.2	3.5	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(3)		0.1	0.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(3)		0.3	0.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(3)		0.4	1.2	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(3)		1.4	2.4	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(3)		0.7	1.4	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(3)		0.6	1.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(3)		2.5	3.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(3)		1.2	2.1	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(3)		1.2	2.5	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = –55°C(3)		1.5	2.9	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(3)		0.4	2.6	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(3)		2.8	3.5	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = –55°C(3)		3.5	5.9	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(3)		1.1	4.7	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(3)		5.8	8.0	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = –55°C(3)		5.6	9.3	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(3)		3.7	8.0	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(3)		13.0	25	
V_{DO}	Worst case dropout voltage(4)	I_{OUT} = 3 A, V_{OUT} = 1.3 V, V_{IN} = V_{OUT} + V_{DO}		210	335	mV
	Dropout voltage(4)	I_{OUT} = 3 A, V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + V_{DO}		196		
I_{CL}	Programmable output current limit range	V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance = 47 kΩ	500		750	mA
		V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance varies	200		3500(5)	mA
V_{CS}	Operating voltage range at CS		0.3		V_{IN}	V

(4) The parameter is specified to the limit in characterization, but not production tested.
(5) The maximum limit of the I_{CL}parameter is specified to the limit in characterization, but not production tested.

Electrical Characteristics for TPS7H1101 (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CSR	Current sense ratio	I_{LOAD} / I_{CS}, V_{IN} = 2.3 V, V_{OUT} = 1.9 V		47500	47394	56000	
I_{GND}	GND terminal current	V_{IN} = 1.5 V, V_{OUT} = 1.2 V, I_{OUT} = 2 A			10	16	mA
I_Q	Quiescent current (no load)	V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 0 A			7	10	mA
I_{SHDN}	Shutdown current	1.5 V ≤ V_{IN} ≤ 7 V			26	230	µA
		1.5 V ≤ V_{IN} ≤ 7 V, Post 100 kRads (si), T_J = 25°C(6)				1400	µA
I_{SNS}, I_{FB}	FB/SNS terminal current	V_{IN} = 7 V, V_{OUT} = 6.65 V			1	5	nA
I_{EN}	EN terminal input current	V_{IN} = 7 V, V_{EN} = 7 V, V_{OUT} = 6.65 V			20	150	nA
V_{ILEN}	EN terminal input low (disable)	3.5 V < V_{IN} < 7 V			0.30 x V_{IN}		V
V_{IHEN}	EN terminal input high (enable)	3.5 V < V_{IN} < 7 V			0.75 × V_{IN}		V
Eprop Dly	Enable terminal propagation delay	V_{IN} = 2.2 V, EN rise to I_{OUT}rise			650	1000	µs
T_{EN}	Enable terminal turn-on delay	V_{IN} = 2.2 V, V_{OUT} = 1.8 V, I_{LOAD} = 1 A, C_{OUT} = 220 µF, C_{SS} = 2 nF			1.4	1.6	ms
V_{THPG}	PG threshold	No load, 0.8 V ≤ V_{OUT} ≤ 6.65 V		86	90%		
$V_{THPGHYS}$	PG hysteresis	1.5 V ≤ V_{IN} ≤ 7 V			2%		
V_{OLPG}	PG terminal output low	I_{PG} = 0 to –1 mA			120	300	mV
I_{LKGPG}	PG terminal leakage current	V_{OUT} > V_{THPG}, V_{PG} = 1.2 V			0.2	1.5	µA
		V_{OUT} > V_{THPG}, V_{PG} = 7 V			0.5	2.5	µA
I_{SS}	SS terminal charge current	V_{IN} = 1.5 to 7 V			2.5	3.5	µA
I_{SSdisb}	SS terminal disable current	V_{IN} = 1.5 to 7 V			5	10	µA
V_{SS}	SS terminal voltage (device enabled)(7)	V_{IN} = 1.5 to 7 V				1.232	V
V_{SSdisb}	SS terminal low-level input voltage to disable device	V_{IN} = 1.5 to 7 V				0.4	V
PSRR	Power-supply rejection ratio	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, C_{OUT} = 220 µF	1 kHz		48		dB
			100 kHz		25		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 3 A, V_{IN} = 2 V, V_{OUT} = 1.8 V			20.33		$µV_{RMS}$
TSD	Thermal shutdown temperature				185		°C
T_J	Operating junction temperature			–55		125	°C

(6) This maximum limit applies to SMD 5962R13202 post 100 kRads (Si) test at 25°C.
(7) Any external pullup voltage should not exceed 1.188 V.

7.7 Typical Characteristics (TPS7H1201-HT)

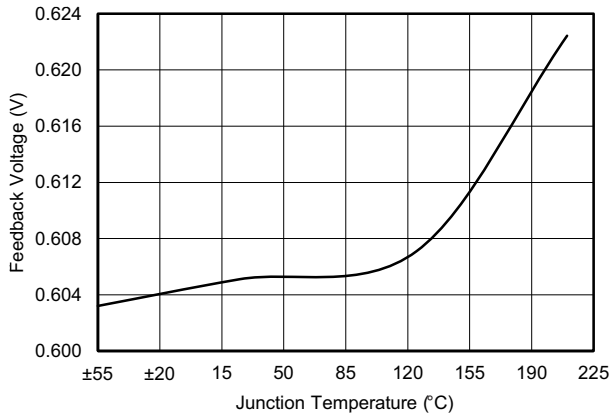


Figure 1. Feedback Voltage vs Temperature

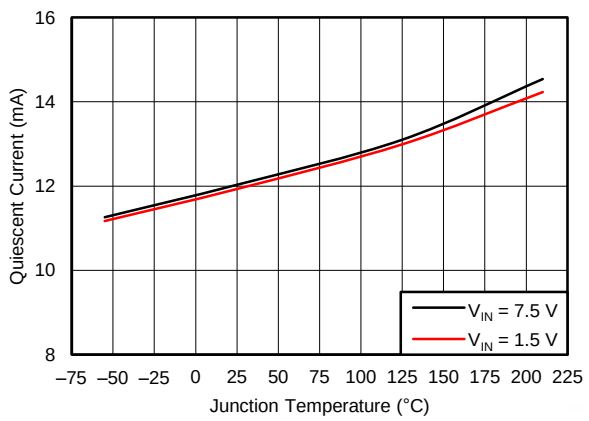


Figure 2. Quiescent Current vs Temperature

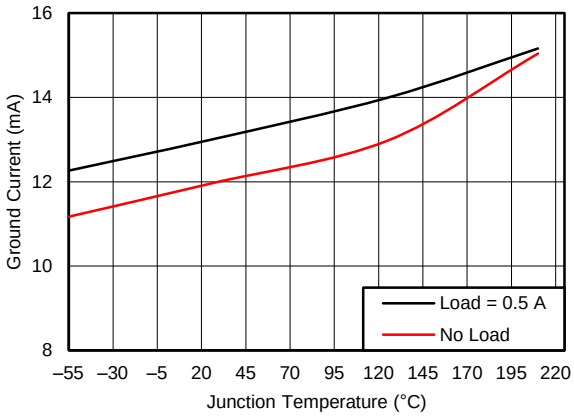


Figure 3. Ground Current vs Temperature

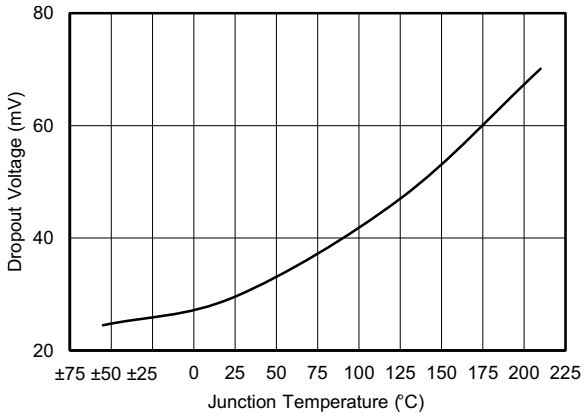


Figure 4. Dropout Voltage vs Temperature

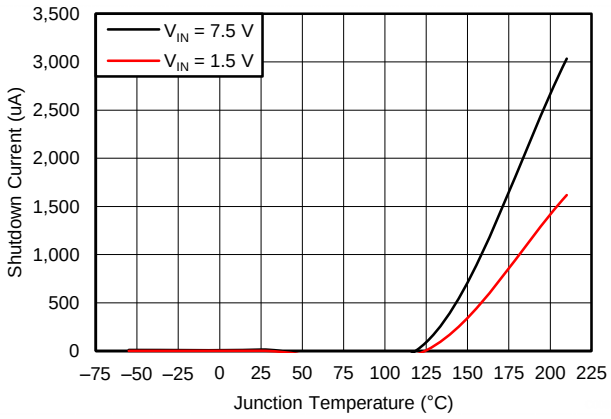


Figure 5. Shutdown Current vs Temperature

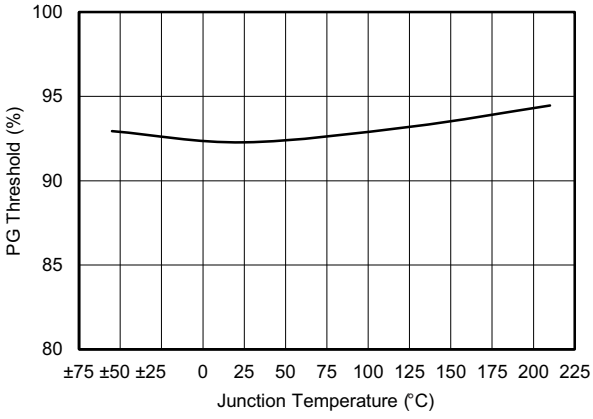


Figure 6. PG Threshold vs Temperature

Typical Characteristics (TPS7H1201-HT) (continued)

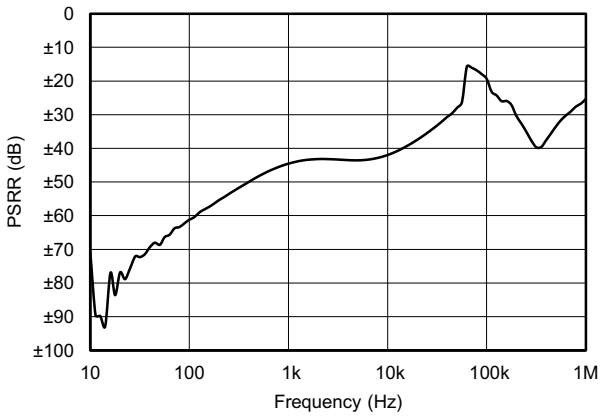


Figure 7. Power Supply Ripple Rejection vs Frequency, I_{OUT} = 250 mA

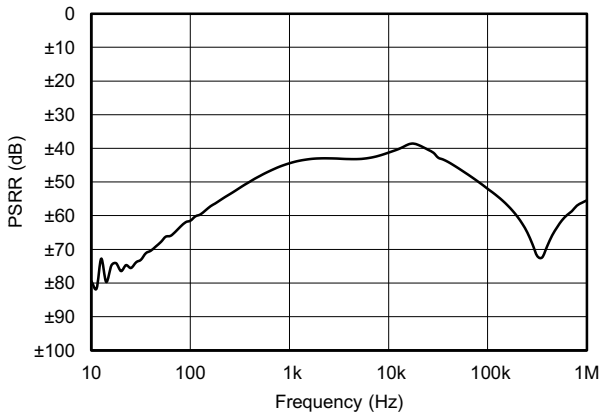


Figure 8. Power Supply Ripple Rejection vs Frequency, I_{OUT} = No Load

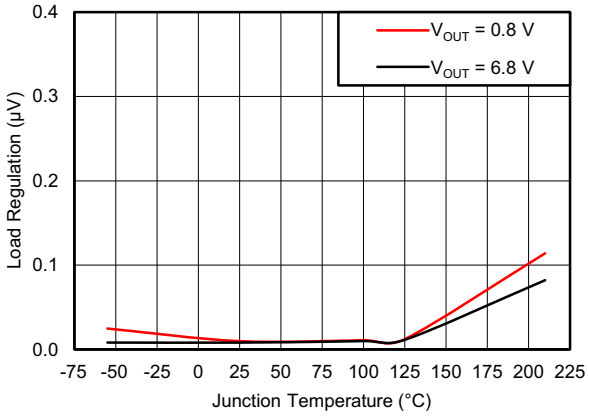


Figure 9. Load Regulation vs Temperature

7.8 Typical Characteristics (TPS7H1101-SP)

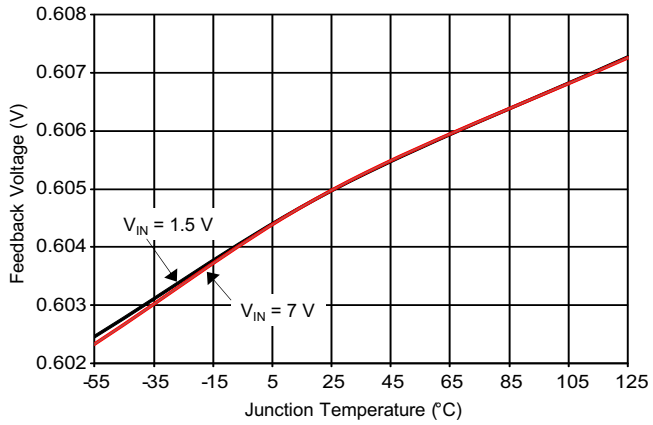


Figure 10. Feedback Voltage vs Temperature

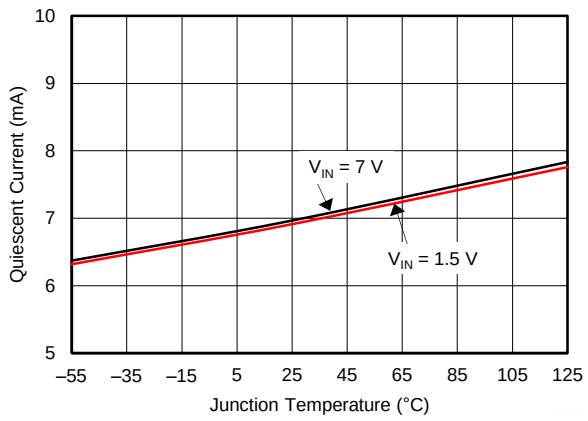


Figure 11. Quiescent Current vs Temperature

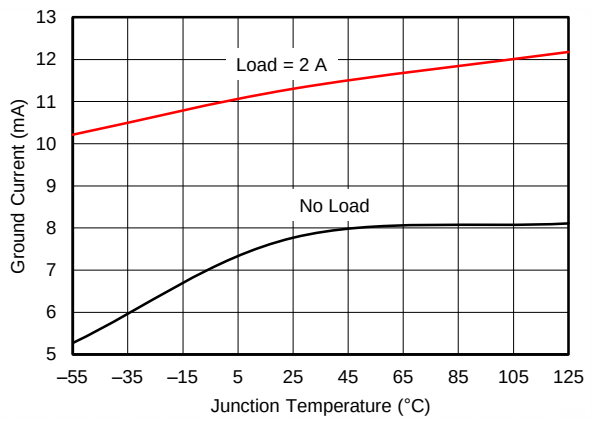


Figure 12. Ground Current vs Temperature

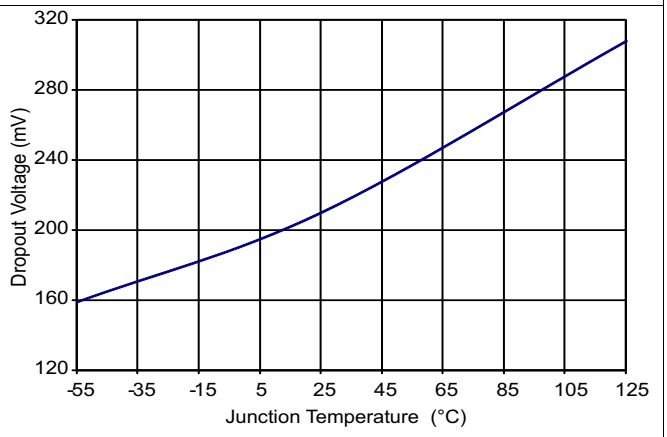


Figure 13. Dropout Voltage vs Temperature

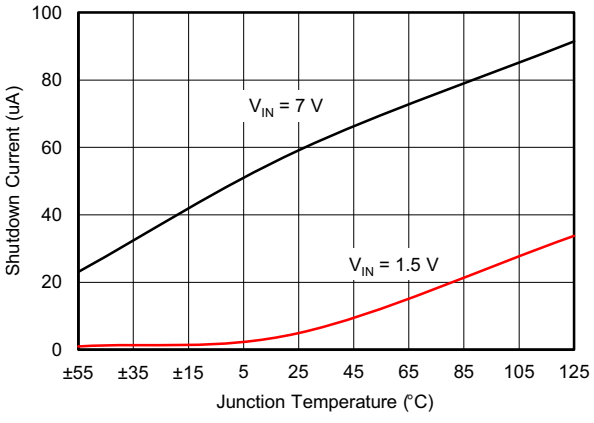


Figure 14. Shutdown Current vs Temperature

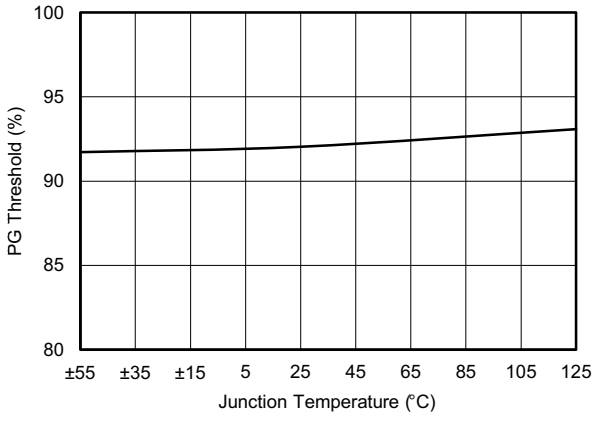


Figure 15. PU Threshold vs Temperature

8 Detailed Description

8.1 Overview

8.1.1 TPS7H1101

The TPS7H1101 is 3-A, 1.5- to 7-V LDO linear regulator that uses PMOS pass element configuration.

It uses TI's proprietary process to achieve low noise, high PSRR combined with high thermal performance in a 16-pin ceramic flatpack package (HKR).

A number of features are incorporated in the design to provide high reliability and system flexibility. Current foldback, overload, current limit, and thermal protection are incorporated in the design to make it viable for harsh environments.

A resistor connected from the current sense (CS) terminal to VIN indicates voltage proportional to the output current. When CS is held high, foldback current limit is enabled. Shorting CS low disables the foldback current limit.

A resistor connected from the programmable current limit (PCL) terminal to ground sets the over current limit activation point. When overcurrent limit activation point is reached, it results in LDO going into current foldback mode. Output current is reduced to approximately 50% of the current limit set point.

TPS7H1101 incorporates thermal protection, which disables the output when the junction temperature rises approximately 185°C, allowing the device to cool. Depending on the power dissipation, thermal resistance, and ambient temperature, the thermal protection turns on. Cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The device also has a current sense monitoring feature. A resistor connected from the CS terminal to VIN indicates voltage proportional to the output load current. *PCL* provides a detailed description of this feature.

To provide system flexibility for demanding current needs, the LDO can be configured in parallel operation as indicated in Figure 17. *Current Sharing* provides detailed parallel operation information.

An enable feature is incorporated in the design allowing the user to enable or disable the LDO. Power Good, an open-drain connection, indicates the status of the output voltage. These provide the customers system flexibility in monitoring and controlling the LDO operation. When using the Enable function, V_{IN} voltage must be >3.5 V. For V_{IN} from 1.5 to 7 V, TPS7H1101 can be disabled using the Soft-Start (SS) terminal as described in *Enable/Disable*.

8.1.2 TPS7H1201

The TPS7H1201 is a 0.5-A, 1.5- to 7-V LDO linear regulator that uses PMOS pass element configuration.

It uses TI's proprietary process to achieve low noise, high PSRR combined with high thermal performance in a 16-terminal ceramic flatpack package (HKS) or KGD (bare die) package.

A number of features are incorporated in the design to provide high reliability and system flexibility. Overload protection is incorporated in the design to make it viable for harsh environments.

A resistor connected from the PCL terminal to ground sets the current limit activation point. When current limit activation point is reached, output voltage drops while output load current is maintained at current limit point.

The device also has a current sense monitoring feature. A resistor connected from the CS terminal to VIN indicates voltage proportional to the output load current. *PCL* provides a detailed description of this feature.

To provide system flexibility for demanding current needs, the LDO can be configured in parallel operation as indicated in Figure 17. *Current Sharing* provides detailed parallel operation information.

An enable feature is incorporated in the design allowing the user to enable or disable the LDO. Power Good, an open-drain connection, indicates the status of the output voltage. These provide the customers' system flexibility in monitoring and controlling the LDO operation. When using the Enable function, V_{IN} voltage must be >3.5 V. For V_{IN} from 1.5 to 7 V, TPS7H1201 can be disabled using the SS terminal as described in *Enable/Disable*.

8.2 Functional Block Diagrams

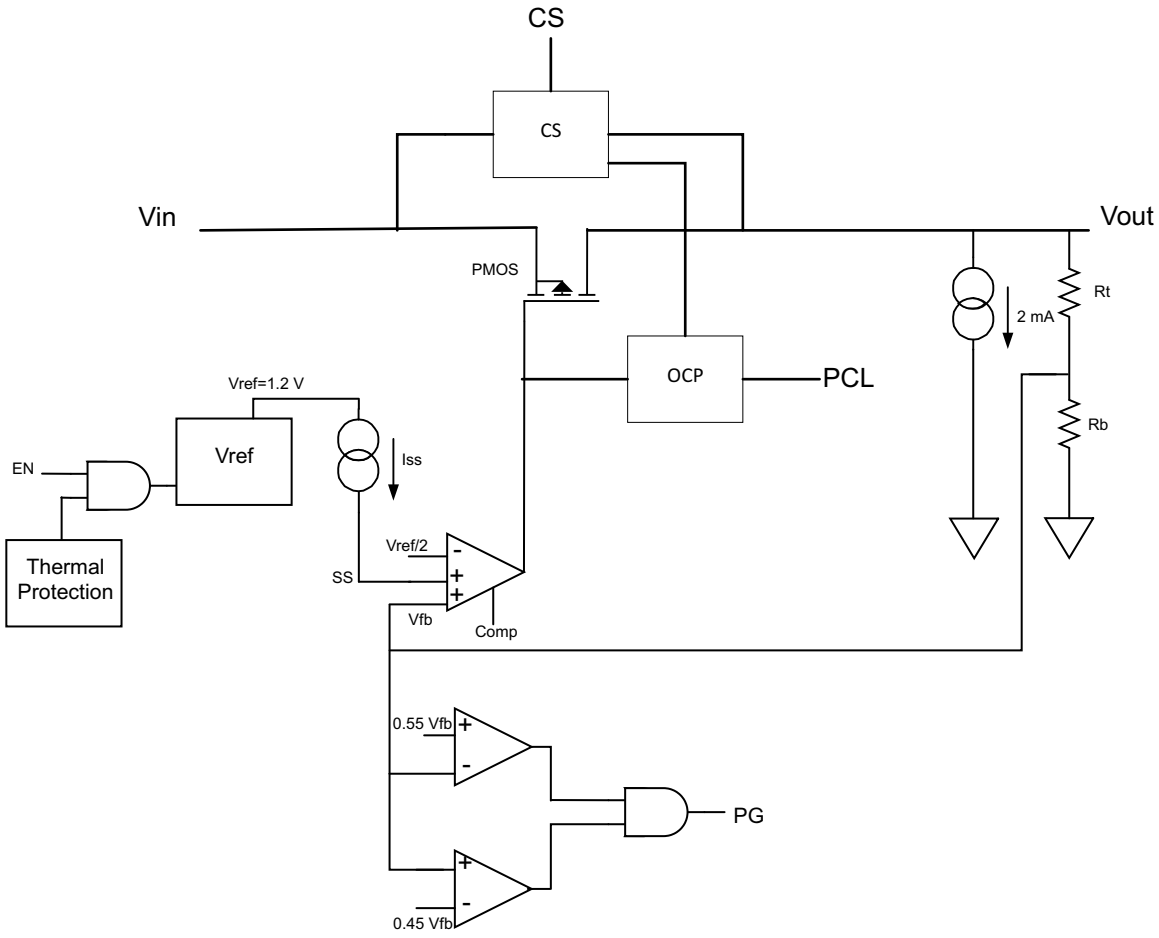


Figure 16. Block Diagram

Functional Block Diagrams (continued)

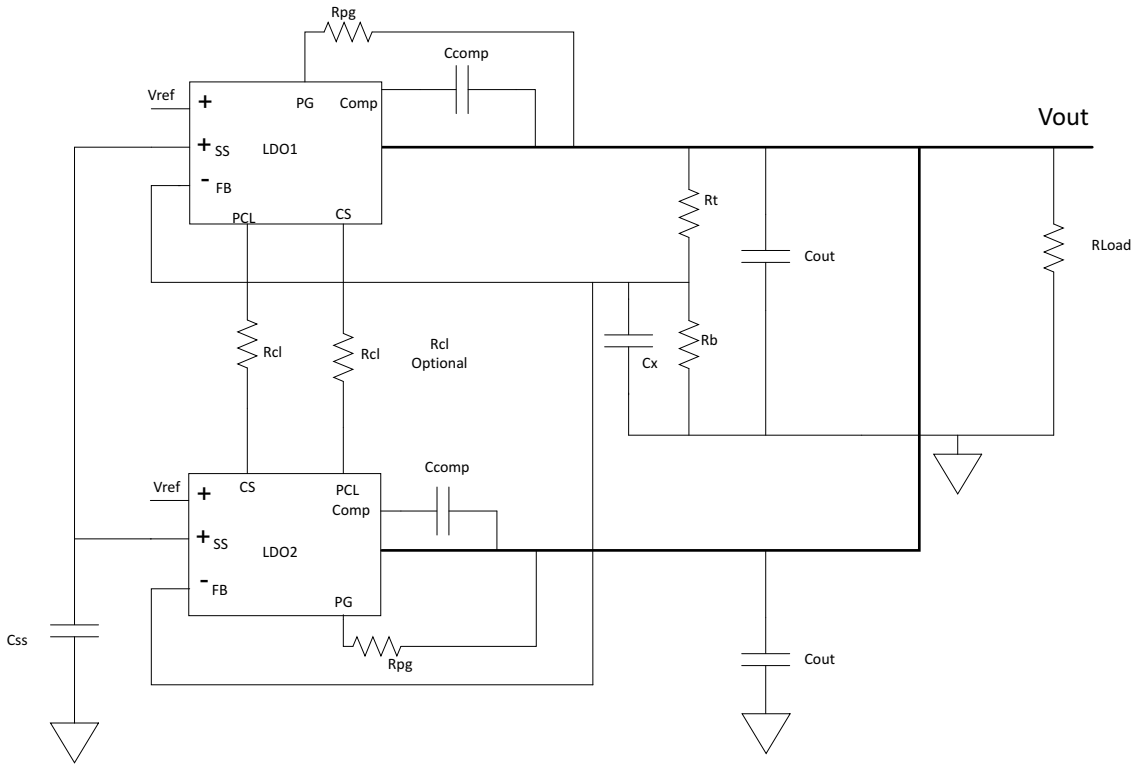


Figure 17. Block Diagram (Parallel Operation)

8.3 Feature Description

8.3.1 Soft-Start

Connecting a capacitor on the CS terminal to GND (C_{SS}) slows down the output voltage ramp rate. The soft-start capacitor charges up to 1.2 V.

$$C_{SS} = \frac{t_{SS} \bullet I_{SS}}{V_{FB}}$$

where

- t_{ss} = Soft-start time
- I_{ss} = 2.5 µA
- $V_{FB} = V_{REF} / 2 = 0.605$ V (1)

8.3.2 Power Good (PG)

Power Good terminal (9) is an open-drain connection and can be used to sequence multiple LDOs. Figure 18 shows typical connection. As shown, maximum voltage at PG terminal must be limited to <1.2 V in order not to forward bias the internal MOSFET diode of PMOS current mirror circuitry.

Feature Description (continued)

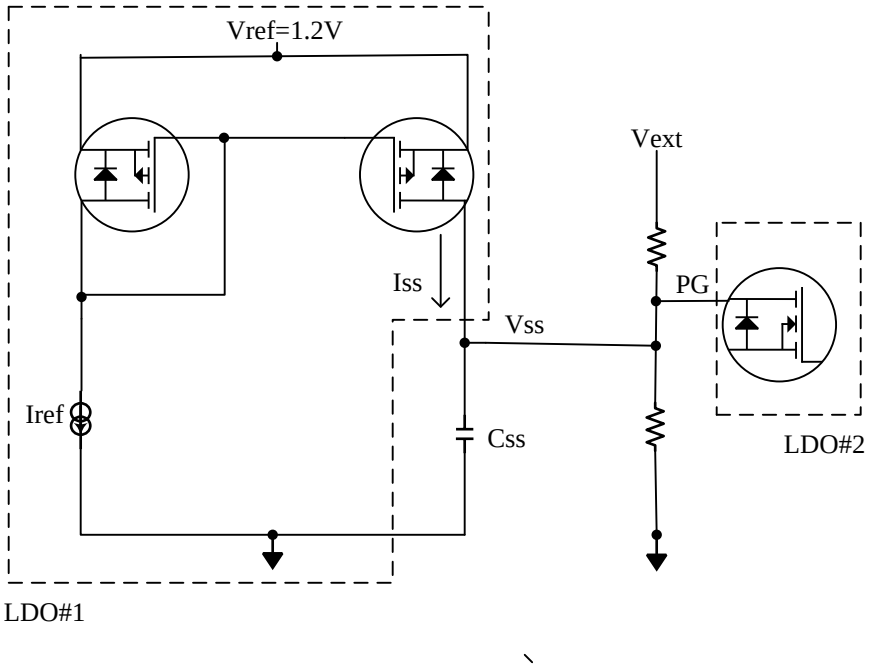


Figure 18. Sequencing LDO1 by Power Good Signal of LDO2

8.4 Device Functional Modes

8.4.1 Enable/Disable

For V_{IN} from 1.5 to 7 V, TPS7H1x01 can be disabled using the SS terminal. The minimum Soft-Start pulldown current is 10 µA, with soft-start to ground voltage of 400 mV or lower. External voltage applied to the SS terminal must be limited to 1.2-V maximum. Removing the logic-low condition on Soft-Start enables the device allowing the Soft-Start capacitor to get charged by the internal current source. Alternatively, for V_{IN} > 3.5 V, the device can be disabled by pulling the enable terminal to logic low. In all other cases, the enable terminal should be connected to V_{IN}.

Device Functional Modes (continued)

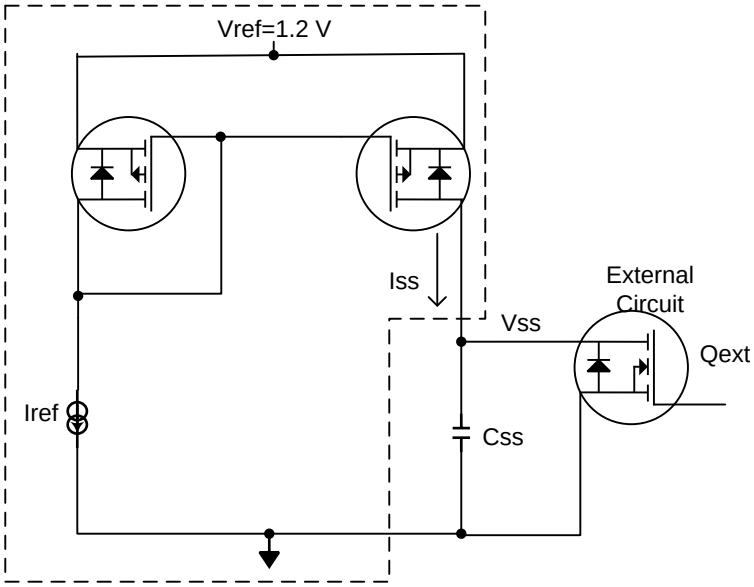


Figure 19. Enable/Disable

The circuit shown in Figure 19 highlights the SS terminal 1 along with block diagram of internal circuitry. Circuitry in dashed outline is internal to the IC composed of PMOSFET current mirror. The PMOS current mirror sources current from the positive supply and external circuitry composed of Q_{ext} is used to sink current from SS terminal 1. As highlighted in the *Electrical Characteristics for TPS7H1201* and *Electrical Characteristics for TPS7H1101* tables – typical I_{SS} = 2.5 µA and max I_{SS} = 3.5 µA for TPS7H1101-SP. If I_{SS} current is exceeded, such as sinking higher current in excess of max I_{SS}, this disables the LDO.

See the *Electrical Characteristics for TPS7H1201* and *Electrical Characteristics for TPS7H1101* tables for the external sink current from SS terminal necessary to disable the IC. Exceeding maximum external sink current does not damage the device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This TPS7H1x01 family of LDO linear regulators, with output current capability up to 3 A are targeted for harsh environment applications. This family of regulators has various features such as low dropout, soft start, output current foldback, high-side current sensing (where sensing voltage at CS pin provides voltage proportional to output current), and current sharing. Thus, multiple LDOs can be daisy chained to provide higher output current for the demanding applications.

9.2 Typical Application

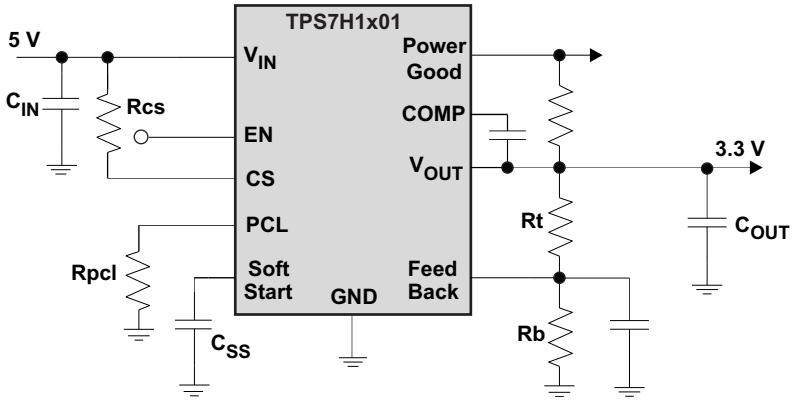


Figure 20. Typical Application Circuit

9.2.1 Design Requirements

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage	1.5 to 7 V
Output voltage	User programmable
Output current	3-A max

9.2.2 Detailed Design Procedure

9.2.2.1 Adjustable Output Voltage (Feedback Circuit)

The output voltage of the TPS7H1101-SP can be set to a user-programmable level between 0.8 and 6.65 V. The output voltage of the TPS7H1201-HT can be set to a user-programmable level between 0.8 and 6.8 V. Achieve this by using a resistor divider connected between V_{OUT}, FB, and GND terminals. R_{TOP} connected between V_{OUT} and V_{FB}, and R_{BOTTOM} connected between V_{FB} and GND.

Use Equation 2 to determine V_{OUT}.

$$V_{OUT} = \frac{(R_{TOP} + R_{BOTTOM}) \bullet V_{FB}}{R_{BOTTOM}} \quad (2)$$

where

- V_{FB} = 0.605 V

Table 2. Resistor Values for Typical Voltages

V_{OUT}	R_{TOP}	R_{BOTTOM}
0.8 V	10 kΩ	30.1 kΩ
1 V	10 kΩ	15 kΩ
1.2 V	10 kΩ	10 kΩ
1.5 V	15 kΩ	10 kΩ
1.8 V	20 kΩ	10 kΩ
2.5 V	32 kΩ	10.1 kΩ
3.3 V	45.9 kΩ	10.2 kΩ
4 V	59 kΩ	10.4 kΩ
5 V	77.7 kΩ	10.6 kΩ
5.5 V	78.7 kΩ	9.65 kΩ
6 V	78.7 kΩ	8.75 kΩ
6.5 V	78.7 kΩ	7.96 kΩ
6.6 V	79.6 kΩ	7.96 kΩ
6.7 V	78.7 kΩ	7.77 kΩ

9.2.2.2 PCL

PCL resistor, R_{pcl}, sets the overcurrent limit activation point and can be calculated per Equation 3.

$$R_{pcl} = (CSR \times V_{ref}) / (I_{CL} - 0.0403) \quad (3)$$

where

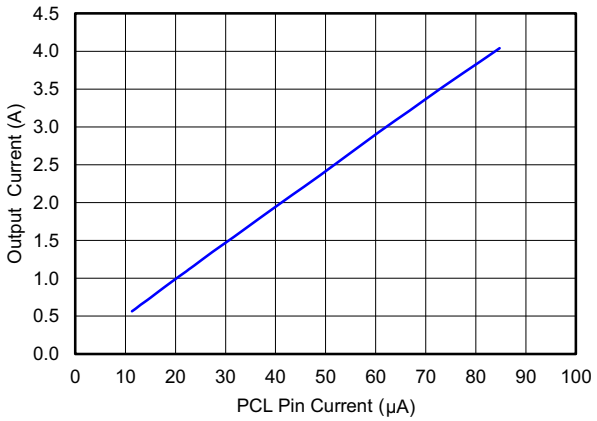
- V_{ref} = 0.605 V
- I_{CL} = programmable current limit (A)
- Current sense ratio (CSR) is the ratio of output load current to I_{CS}. The typical value of the CSR is 47394.

Figure 21 shows the output load current (I_{OUT}) versus PCL terminal current (I_{CL})

A suitable resistor R_{pcl} must be chosen to ensure the CS terminal is within its operating range of 0.3 V to V_{IN}.

For TPS7H1201-HT, the maximum PCL is 700 mA. The range of resistor that can be used on the PCL terminal to GND is 47 to 160 kΩ.

For TPS7H1101-SP, the maximum PCL is 3.5 A. The range of resistor that can be used on the PCL terminal to GND is 8.2 to 160 kΩ.



V_{IN} = 2.3 V V_{OUT} = 1.8 V y = 47394x + 0.0403

Figure 21. I_{OUT} (A) vs I_{PCL} (µA)

9.2.2.3 High-Side Current Sense

Figure 22 shows the cascode NMOS current mirror. V_{cs} must be in the range as specified in the *Electrical Characteristics* table. The following example shows the typical calculation of R_{cs}.

$$I_{CS} = \frac{I_{LOAD} + V_{offset}}{CSR} \tag{4}$$

$$R_{CS} = \frac{V_{IN} - V_{CS}}{I_{CS}}$$

where

- I_{LOAD} is the output load current.
- CSR is the current sense ratio. (5)

When V_{IN} = 2.3 V, select V_{CS} = 2.05 V, I_{LOAD} = 3 A, CSR = 47394, and V_{offset} = 0.1899 A, then I_{CS} = 67.306 µA and R_{CS} = 3.714 kΩ.

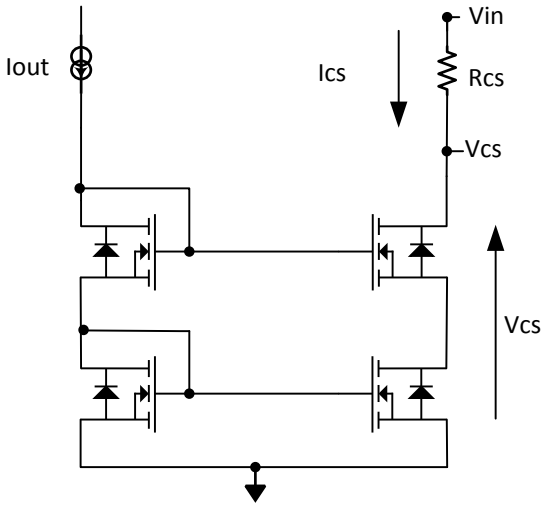
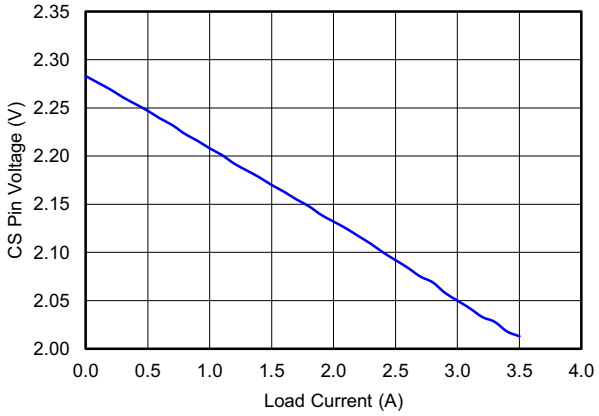


Figure 22. Cascode NMOS Current Mirror

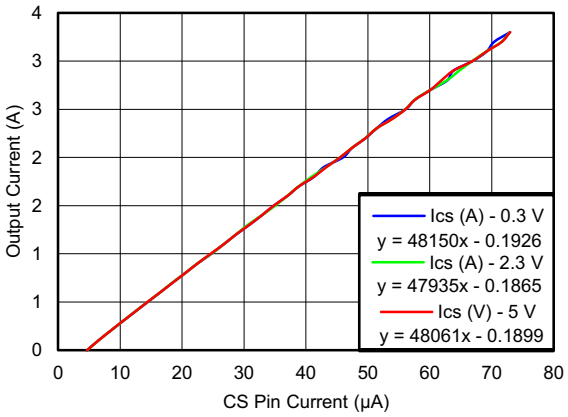
For TPS7H1101-SP, Figure 23 shows the typical curve V_{CS} vs I_{OUT} for V_{IN} = 2.28 V and R_{CS} = 3.65 kΩ. A resistor connected from the CS terminal to V_{IN} indicates voltage proportional to the output current.



V_{IN} = 2.3 V V_{OUT} = 1.8 V y = 0.078x + 2.2853

Figure 23. V_{CS} (V) vs I_{OUT} (A) (TPS7H1101-SP)

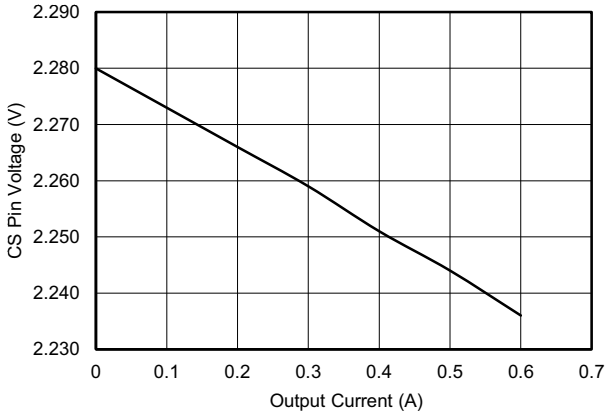
Monitoring current in CS terminal (I_{CS} vs I_{OUT}) indicates the CSR between the main PMOSFET and the current sense MOSFET as shown in Figure 24.



V_{IN} = 2.3 V V_{OUT} = 1.8 V

Figure 24. I_{OUT} (A) vs I_{CS} (A) (TPS7H1101-SP)

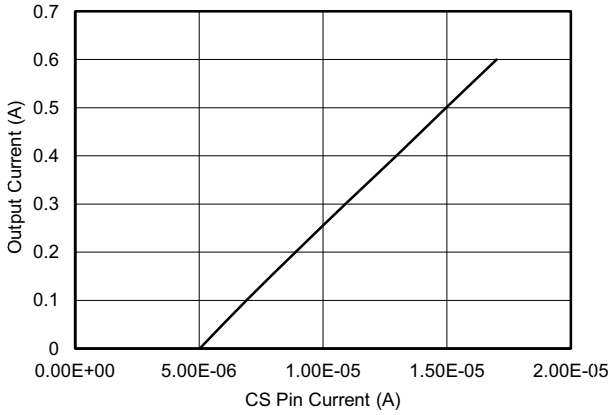
For TPS7H1201-HT, monitoring the voltage at the CS terminal indicates voltage proportional to the output current. Figure 23 shows typical curve V_{CS} vs I_{OUT} for V_{IN} = 2.28 V and R_{CS} = 3.65 kΩ.



y = –0.0732x + 2.2804

Figure 25. V_{CS} (V) vs I_{OUT} (A) (TPS7H1201-HT)

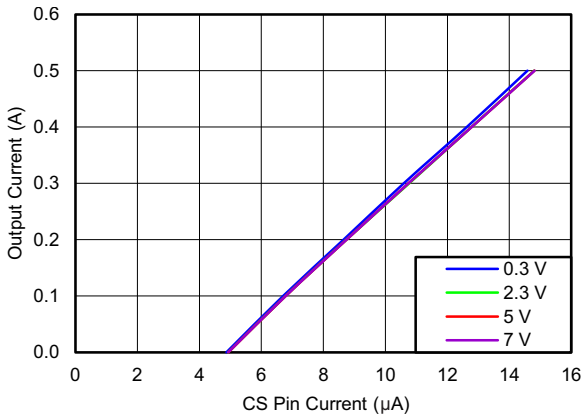
Monitoring current in CS terminal (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMOSFET and the current sense MOSFET as shown in Figure 24.



$$y = 49917x - 0.2466$$

Figure 26. I_{OUT} (A) vs I_{CS} (A)

Figure 27 shows I_{OUT} vs I_{CS} when the voltage on CS terminal is varied from 0.3 to 7 V.



V_{IN} = 2.3 V V_{OUT} = 1.8 V

Figure 27. I_{OUT} (A) vs I_{CS} (A) (TPS7H1201-HT)

9.2.2.4 Current Foldback

1. The TPS7H1101-SP has a current foldback feature which can be enabled when the CS terminal is held high. Shorting CS low disables the foldback current limit.
2. With foldback current limit enabled, when current limit trip point is activated,

   (a) Output voltage drops low
   (b) Output current folds back to approximately 50% of the current limit trip point.
   This results in minimizing the power loss under fault conditions. Monitoring the voltage at the CS terminal indicates voltage proportional to the output current.

9.2.2.5 Transient Response

For TPS7H1101-SP, Figure 28, Figure 29, and Figure 30 indicate the transient response behavior of the LDO for 50% step load change.

Channel 1: Output voltage overshoot/undershoot

Channel 2: Step load in current

Channel 3: Input voltage

Figure 31, Figure 32, and Figure 33 indicate the transient response behavior of the TPS7H1201-HT.

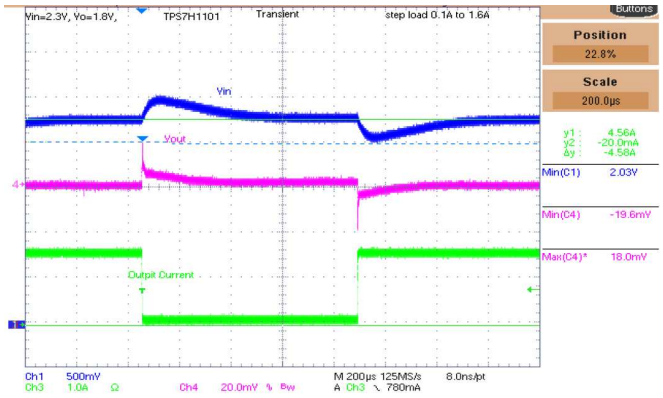


Figure 28. Load Transient Response: Step Load 0.1 to 1.6 A, V_{IN} = 2.3 V, V_{OUT} = 1.8 V (TPS7H1101-SP)

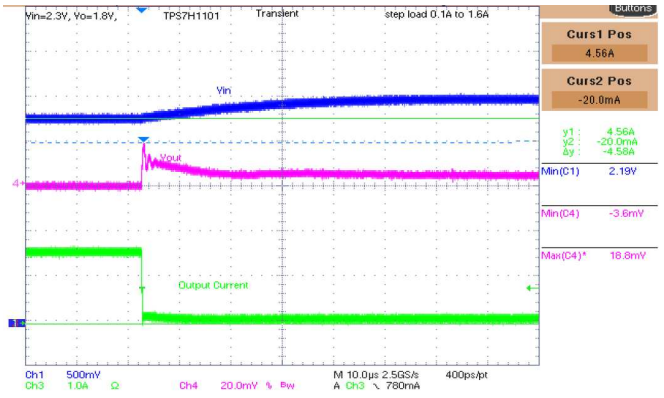


Figure 29. Expanded View Overshoot

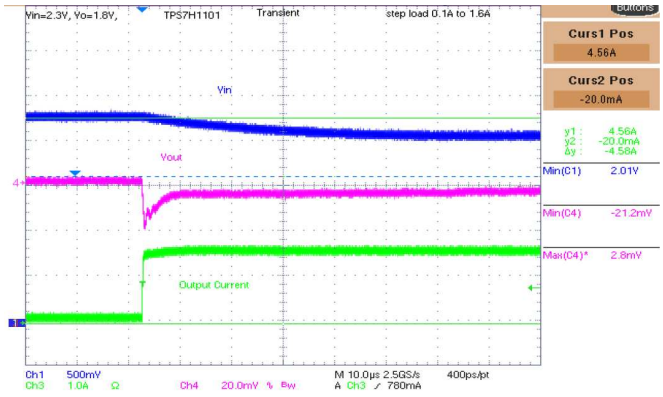


Figure 30. Expanded View Undershoot

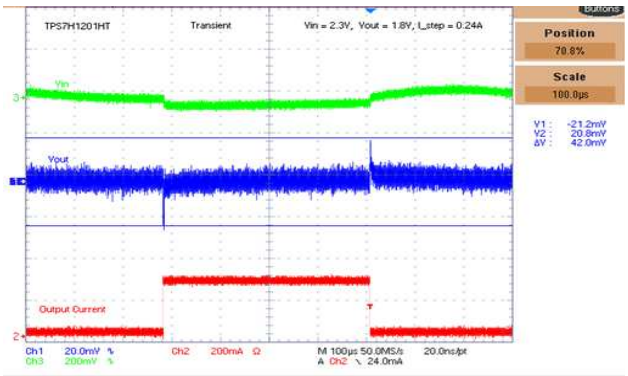


Figure 31. Load Transient Response: Step Load 0 A to 250 µA, V_{IN} = 2.3 V, V_{OUT} = 1.8 V (TPS7H1101-SP)

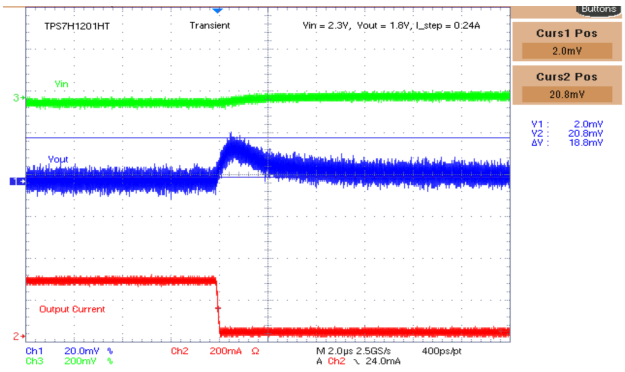


Figure 32. Expanded View Overshoot

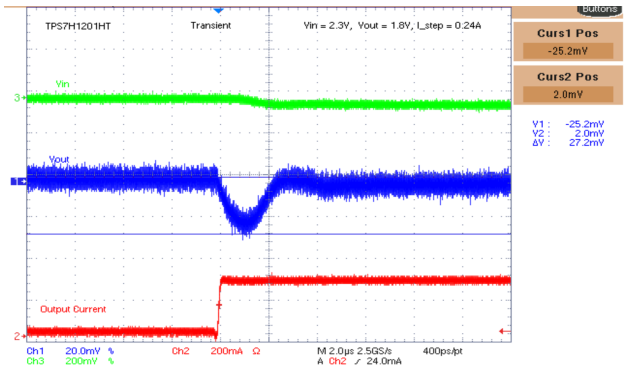


Figure 33. Expanded View Undershoot

9.2.2.6 Current Sharing

For demanding load requirements, multiple LDOs can be paralleled as indicated in Figure 17. In parallel mode, the CS terminal of LDO1 must be connected to the PCL terminal of LDO2 via a series resistor, R_{CL}, and CS terminal of LDO2 must be connected to PCL terminal of LDO1 via series resistor, R_{CL}. The typical value of R_{CL} in parallel operation is 3.75 kΩ for current limit >6 A. In parallel configuration, R_{CL} (resistor from PCL to GND) and R_{CS} (resistor from CS terminal to V_{IN}) must be left open (unpopulated). The R_{CL} value must be selected so that the operating condition of the CS terminal is maintained, as specified in the *Electrical Characteristics for TPS7H1201* and *Electrical Characteristics for TPS7H1101* tables. The current from PCL through RCL of LDO1 is determined by the output load current of LDO2 divided by the CSR. Hence, the voltage at CS terminal of the LDO1 is 0.605 V – ((output load current of LDO2 + 0.2458) / CSR × R_{CL}). Typical value of R_{CL} is 3.65 kΩ. This parallel configuration provides higher reliability (MTBF) for system needs due to reduced stress on the components, as the load current is shared between the two LDOs.

Alternately, it can also provide twice the output current to meet system needs. When using two LDOs in parallel operation for higher output load current, use POL TPS50x01 as an input source.

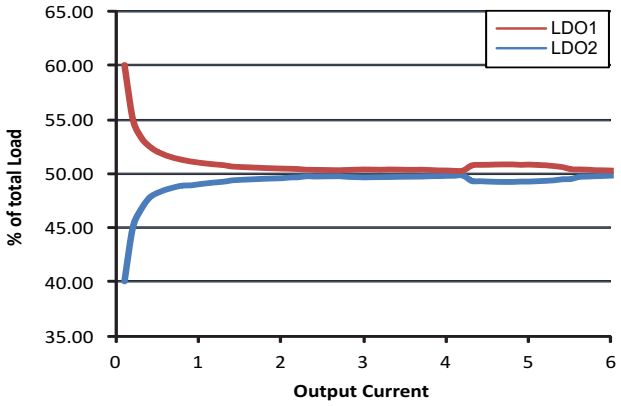


Figure 34. LDO Current Share (TPS7H1101-SP)

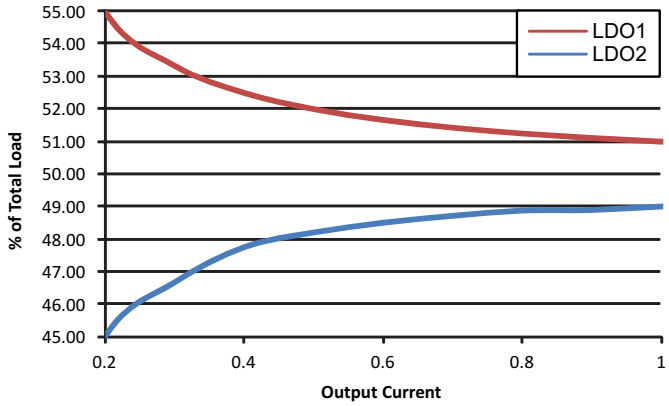


Figure 35. LDO Current Share (TPS7H1201-HT)

9.2.2.7 Compensation

Figure 36 shows a generic block diagram for TPS7H1101-SP LDO with external compensation components. LDO incorporates nested loops, thus providing the high gain necessary to meet design performance.

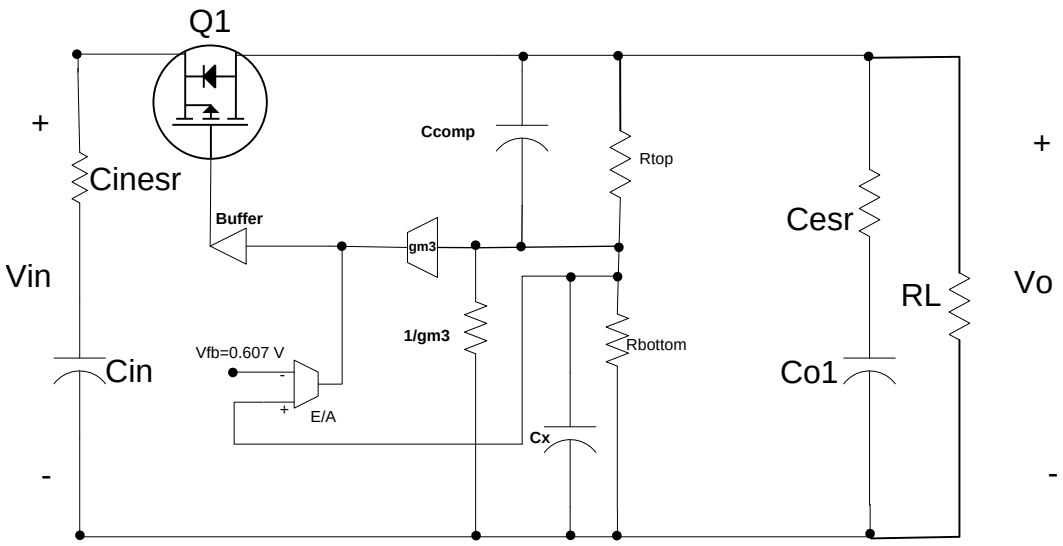


Figure 36. TPS7H1101-SP Compensation

Resistor divider composed of R_{top} and R_{bottom} determine the output voltage set points as indicated by Equation 2.

Output capacitor C_{OUT} introduces a pole and a zero as shown in the following.

$$F_{p\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet R_L} \quad (6)$$

$$F_{z\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet C_{esr}} \quad (7)$$

C_x introduces a pole to the feedback loop and should be selected to compensate for the output capacitor zero, F_{z_co}.

$$F_p = \frac{1}{2 \bullet \pi \bullet C_x \bullet R_{bottom}} \quad (8)$$

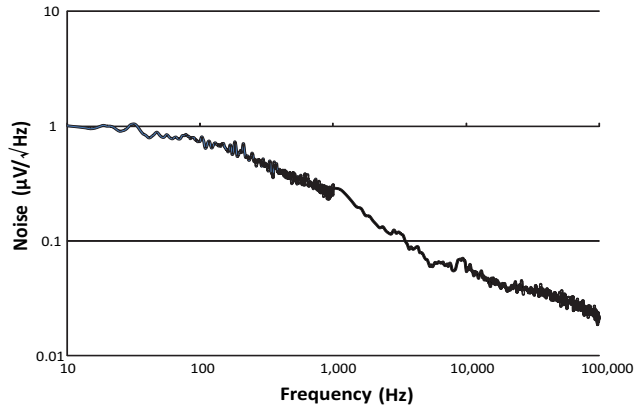
C_x is calculated to be 1000 pF for C_o = 220 µF, C_{esr} = 45 mΩ.

Internal compensation in the LDO cancels the output capacitor pole introduced by C_{OUT} and R_L.

C_{comp} introduces a dominant pole at low frequency. TI recommends that a C_{comp} value of 10 nF be selected that is valid for all line and load conditions.

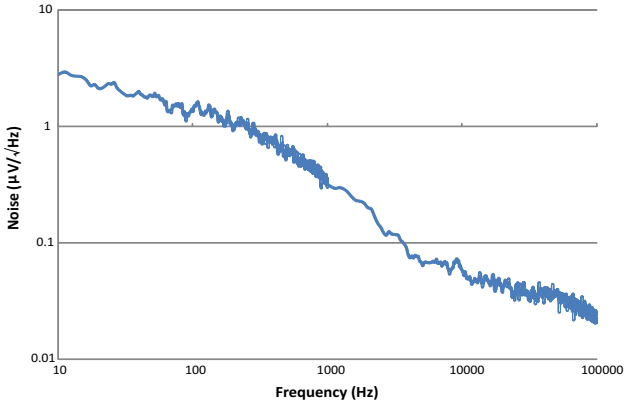
9.2.2.8 Output Noise

Output noise is measured using HP3495A. Figure 37, Figure 38, Figure 39, and Figure 40 show noise of the TPS7H1101-SP and TPS7H1201-HT in µV/√Hz vs Frequency.



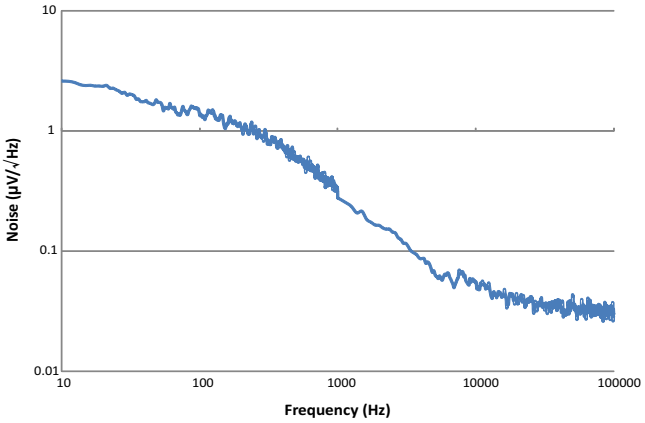
V_{IN} = 2 V V_{OUT} = 1.8 V at 3 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

Figure 37. TPS7H1101-SP – RMS Noise (10 Hz to 100 kHz) = 20.33 µVrms



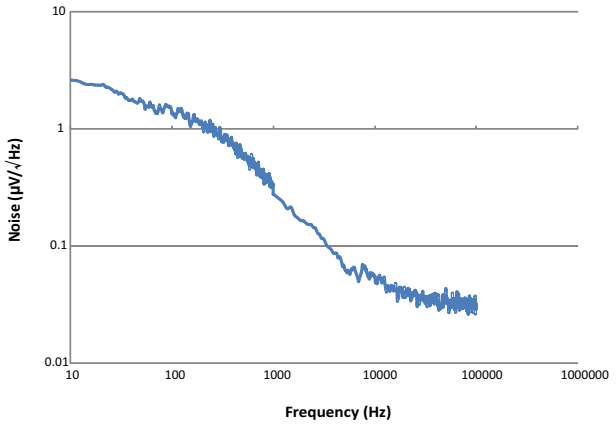
V_{IN} = 7 V V_{OUT} = 6.7 V at I_{LOAD} = 3 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

Figure 38. TPS7H1101-SP - RMS Noise (10 Hz to 100 kHz) = 31.68 µVrms



V_{IN} = 2.1 V V_{OUT} = 1.8 V at I_{LOAD} = 0.5 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

Figure 39. TPS7H1201-HT - RMS Noise (10 Hz to 100 kHz) = 20.26 µVrms



V_{IN} = 7 V V_{OUT} = 6.7 V at I_{LOAD} = 0.5 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

Figure 40. TPS7H1201-HT – RMS Noise (10 Hz to 100 kHz) = 31 µVrms

9.2.2.9 Capacitors

TPS7H1X01 requires the use of a combination of tantalum and ceramic capacitors to achieve good volume to capacitance ratio. Table 3 highlights some of the capacitors used in the device. TI recommends to follow proper derating guidelines as recommended by the capacitor manufacturer based upon output voltage and operating temperature.

Note that polymer-based tantalum capacitors must be derated to at least 60% of rated voltage, whereas manganese oxide (MnO_2) based tantalum capacitors should be derated to 33% of rated voltage depending upon the operating temperature.

TI recommends to use a tantalum capacitor along with a 0.1-µF ceramic capacitor for improved performance. The device is stable for input and output tantalum capacitor values of 10 to 220 µF with the ESR range of 10 mΩ to 2 Ω. However, the dynamic performance of the device varies based on load conditions and the capacitor values used.

It is important to ensure that good design layout practice be followed to ensure that the traces connecting V_{IN} to GND terminals of LDO and V_{OUT} to GND terminals of LDO should be kept short to reduce inductance. Trace length should be no longer than 5 cm.

Table 3. TPS7H1X01 Capacitors

Capacitor Part Number	Capacitor Details (Capacitor, Voltage, ESR)	Type	Vendor
T493X107K016CH612A(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
T493X226M025AH6x20(1)	22 µF, 25 V, 35 mΩ	Tantalum - MnO2	Kemet
T525D476M016ATE035(1)	47 µF, 10 V, 35 mΩ	Tantalum - Polymer	Kemet
T540D476M016AH6520(1)	47 µF, 16 V, 20 mΩ	Tantalum - Polymer	Kemet
T525D107M010ATE025(1)	100 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T541X337M010AH6720(1)	330 µF, 10 V, 6 mΩ	Tantalum - Polymer	Kemet
T525D227M010ATE025(1)	220 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T495X107K016ATE100(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
CWR29FK227JTHC(1)	220 µF, 10 V, 180 mΩ	Tantalum - MnO2	AVX
THJE107K016AJH	100 µF, 16 V, 58 mΩ	Tantalum	AVX
THJE227K010AJH	220 µF, 10 V, 40 mΩ	Tantalum	AVX
SMX33C336KAN360	33 µF, 25 V	Stacked ceramic	AVX
SR2225X7R335K1P5#M123	3.3 µF, 25 V, 10 mΩ	Ceramic	Presidio Components Inc

(1) Operating temperature is –55°C to 125°C.

9.2.3 Application Curves

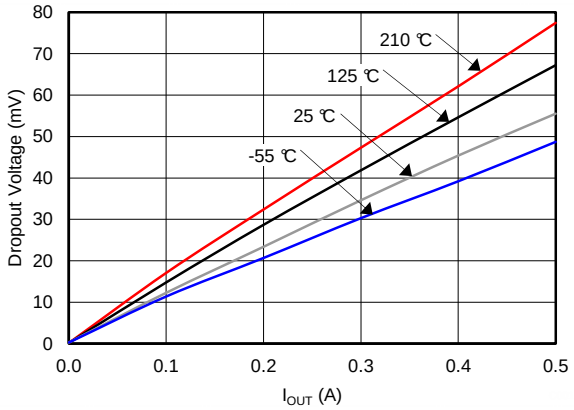


Figure 41. VDO vs I_{OUT} (TPS7H1201-HT)

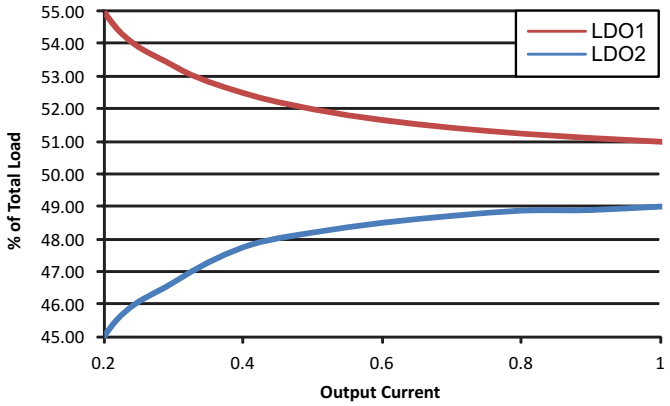


Figure 42. LDO Current Share (TPS7H1201-HT)

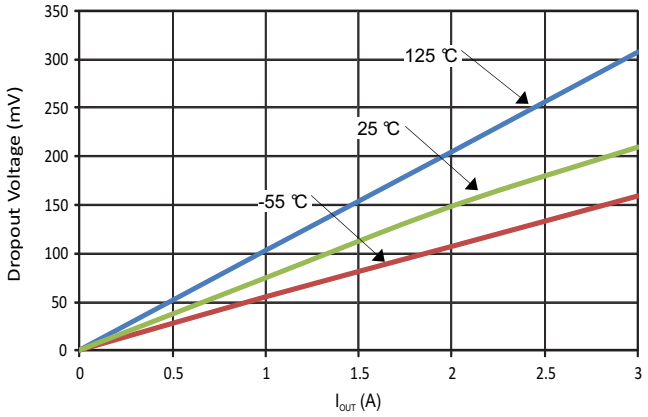


Figure 43. VDO vs I_{OUT} (TPS7H1101-SP)

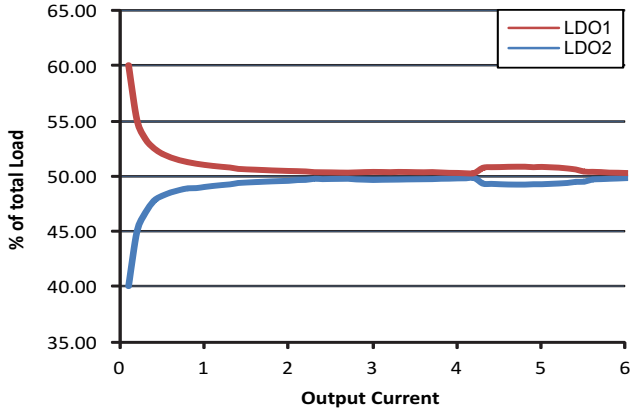


Figure 44. LDO Current Share (TPS7H1101-SP)

10 Power Supply Recommendations

This device is designed to operate with an input voltage supply up to 7 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

11 Layout

11.1 Layout Guidelines

- For best performance, all traces should be as short as possible.
- Use wide traces for IN, Out and GND to minimize the parasitic electrical effects.
- TI recommends a minimum output capacitor of 22uF with ESR of 1ohm or less to prevent oscillations. X7R dielectrics are preferred. See table 2 for various capacitor recommendations.
- Place the output capacitors (COUT) as close as possible to the OUT pin of the device.
- Enable pin pulled up to Vin
- Soft Start pin can be used to perform enable/ disable function as shown in Figure 19.

11.2 Layout Example

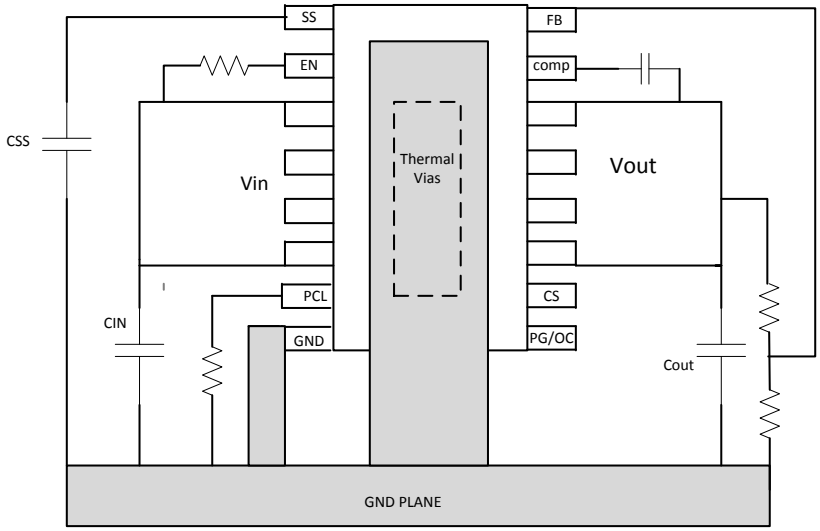


Figure 45. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

Parts	Product Folder	Sample & Buy	Technical Documents	Tools & Software	Support & Community
TPS7H1201-HT	Click here	Click here	Click here	Click here	Click here
TPS7H1101-SP	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1320201VXC	ACTIVE	CFP	HKR	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 125	5962-1320201VXC TPS7H1101-SP	Samples
5962R1320201VXC	ACTIVE	CFP	HKR	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 125	5962R1320201VXC TPS7H1101-RHA	Samples
TPS7H1101HKR/EM	ACTIVE	CFP	HKR	16		TBD	NIAU	N / A for Pkg Type	25 Only	TPS7H1101HKREM	Samples
TPS7H1201SHKS	ACTIVE	CFP	HKS	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 210	TPS7H1201SHKS	Samples
TPS7H1201SKGD1	ACTIVE	XCEPT	KGD	0	70	TBD	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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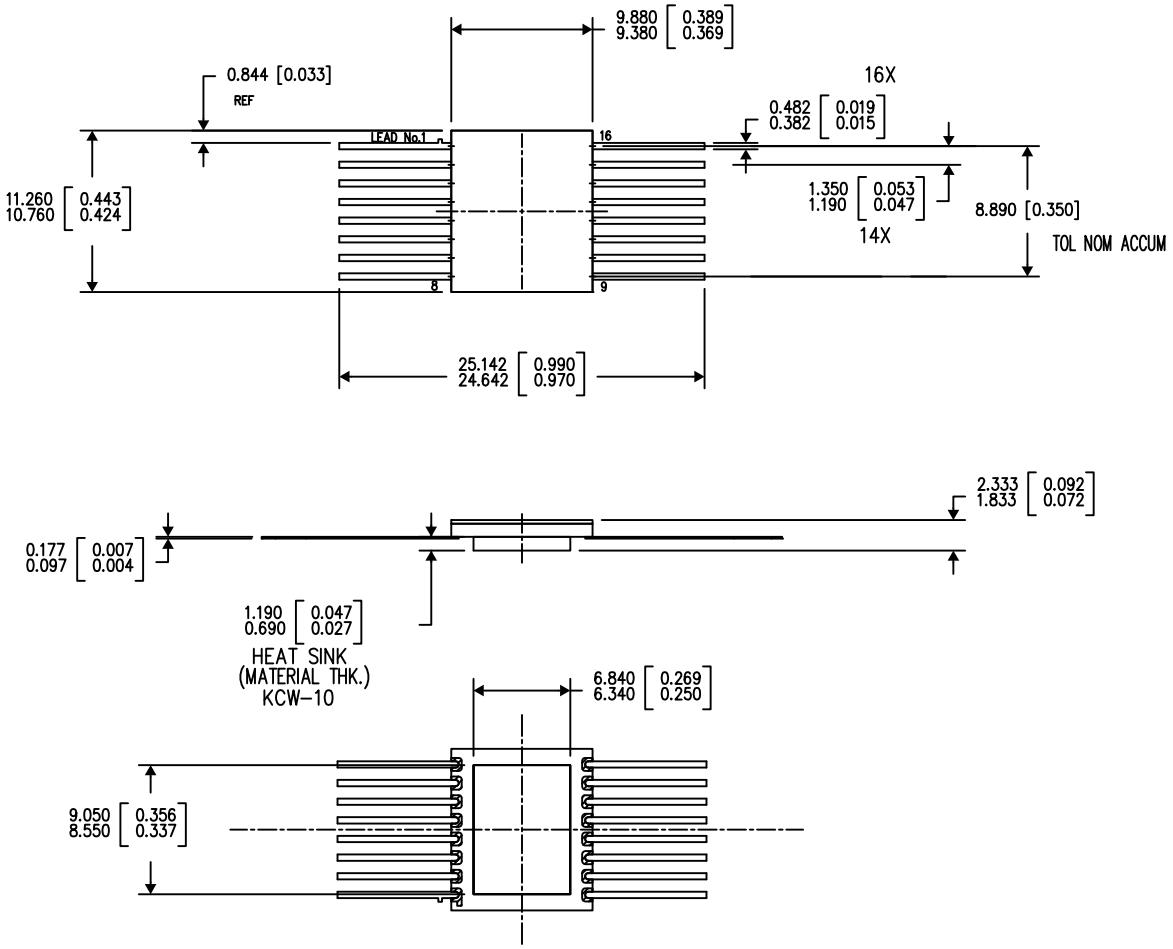
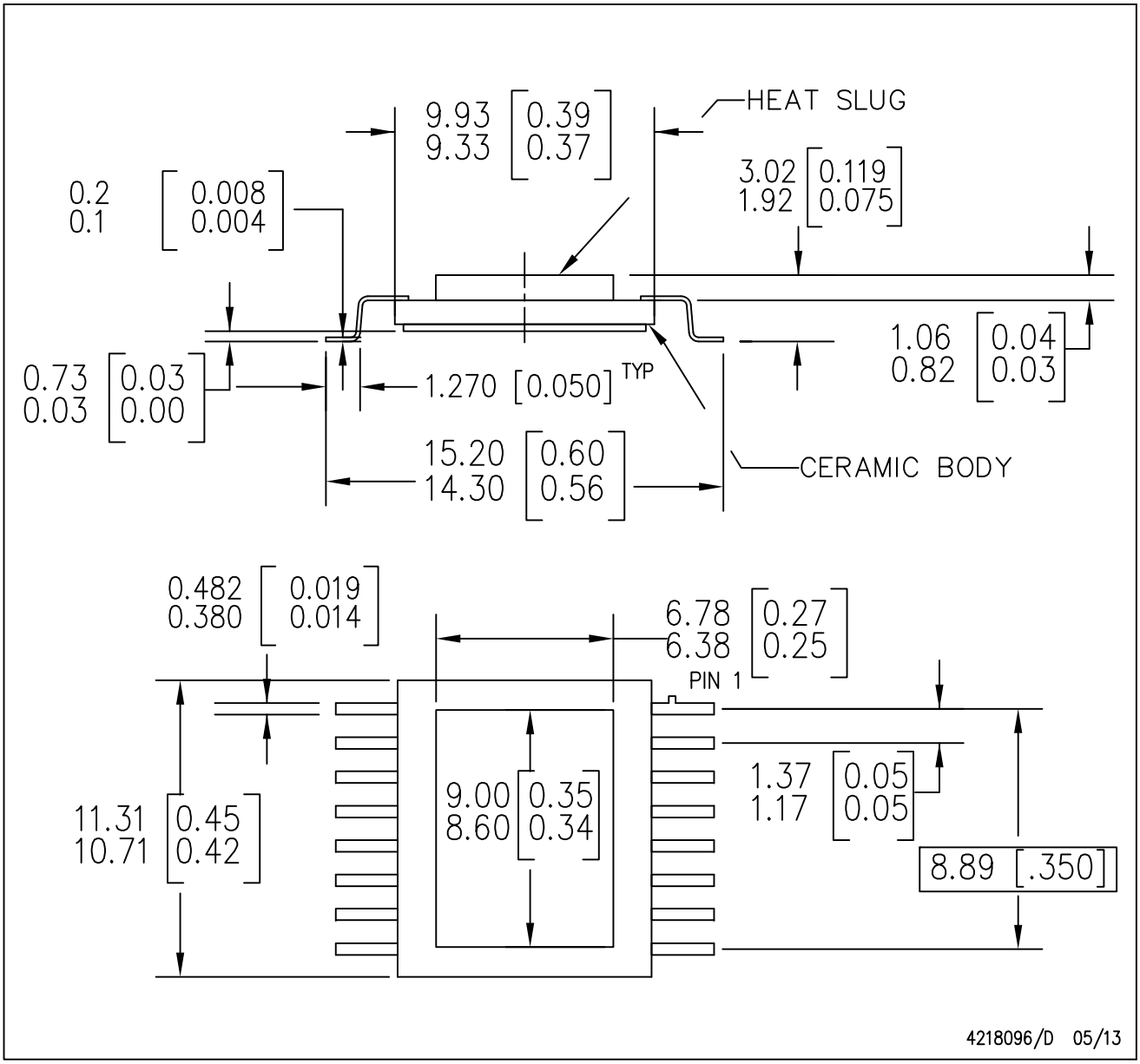
HKR (R–CDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid. Lid and heat slug are connected to pin 8 (Gnd).
D. The terminals will be gold plated.

HKS (R–CDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Pin 8 is connected to lid and heat slug.

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