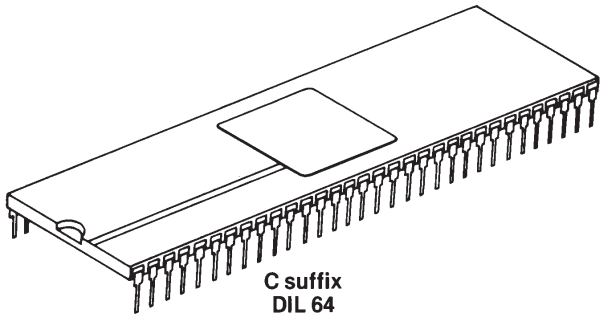
TS68C000

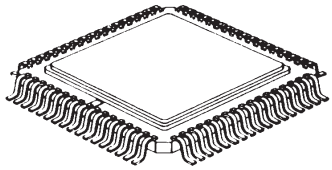
LOW POWER HCMOS 16/32 BIT MICROPROCESSOR

DESCRIPTION

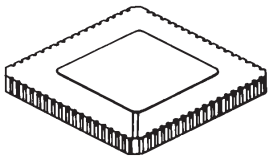
The TS 68C000 reduced power consumption device dissipates an order of magnitude less power than the HMOS TS 68000. The TS 68C000 is an implementation of the TS 68000 16/32 microprocessor architecture. The TS 68C000 has a 16-bit data bus and 24-bit address bus while the full architecture provides for 32-bit address and data-buses. It is completely code-compatible with the HMOS TS 68000, TS 68008 8-bit data bus implementation of the TS 68000 and the TS 68020 32-bit implementation of the architecture. Any user-mode programs written using the TS 68C000 instruction set will run unchanged on the TS 68000, TS 68008 and TS 68020. This is possible because the user programming model is identical for all processors and the instruction sets are proper sub-sets of the complete architecture.



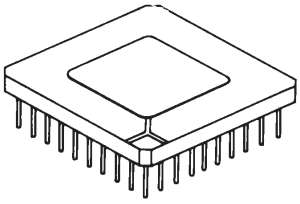
C suffix
DIL 64
Ceramic package



F Suffix
CQFP 68
Ceramic quad flat pack (on request)



E suffix
LCCC 68
Leadless ceramic chip carrier



R suffix
PGA 68
Pin grid array

PIN CONNECTIONS (See chapter A2)
See the ordering information at the end of the data sheet.

MAIN FEATURES

- 16/32-bit data and address register.
- 16 megabytes direct addressing range.
- 56 powerful instruction types.
- Operations on five main data types.
- Memory mapped I/O.
- 14 addressing modes.
- 3 available versions : 8 MHz / 10 and 12.5 MHz.
- Military temperature range : – 55 / + 125°C.
- Power supply : 5 V_{DC} ± 10 %.

SCREENING / QUALITY

This product is manufactured in full compliance with :

- MIL-STD-883 class B.
- DESC drawing 5962-89462.
- TCS standard.

SUMMARY

A - GENERAL DESCRIPTION

INTRODUCTION

This detail specification contains both a summary of the TS 68C000 as well as detailled set of parametrics. The purpose is twofold to provide an instruction to the TS 68C000 and support for the sophisticated user. For detail information on the TS 68C000, refer to «68000 16-Bit Microprocessor User's Manual».

1 - DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

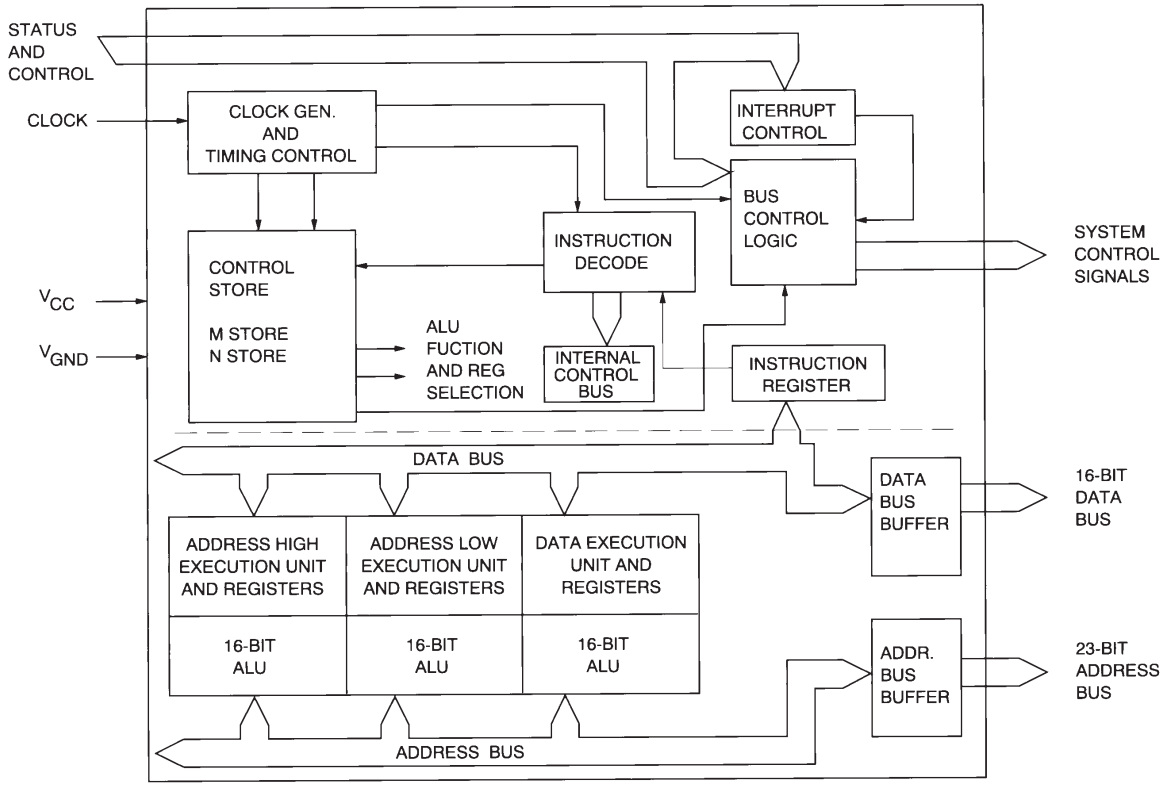


Figure 1 : Block diagram.

2 · PIN ASSIGNMENTS

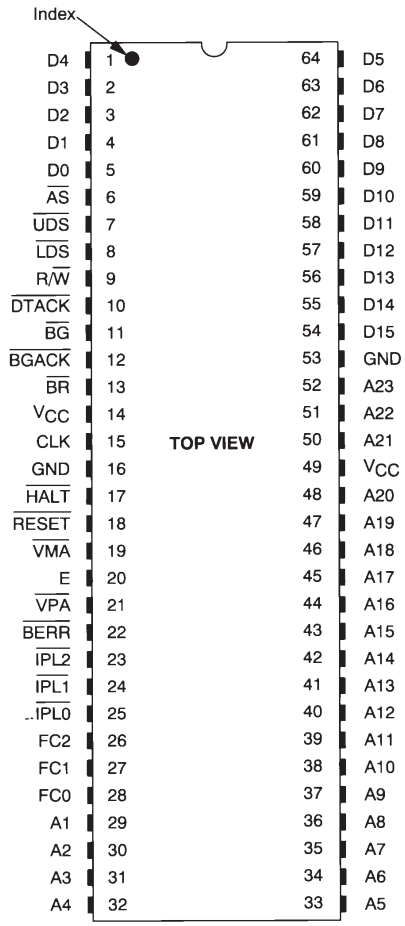


Figure 2.1 : 64-pin dual-in-line package.

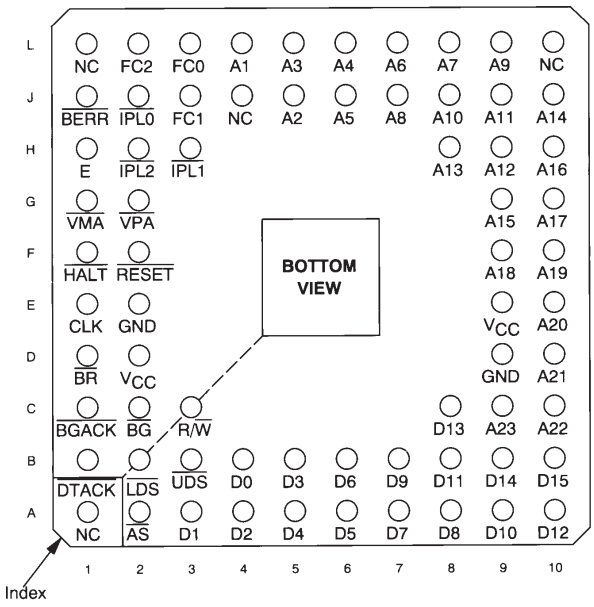


Figure 2.2 : 68-terminal pin grid array.

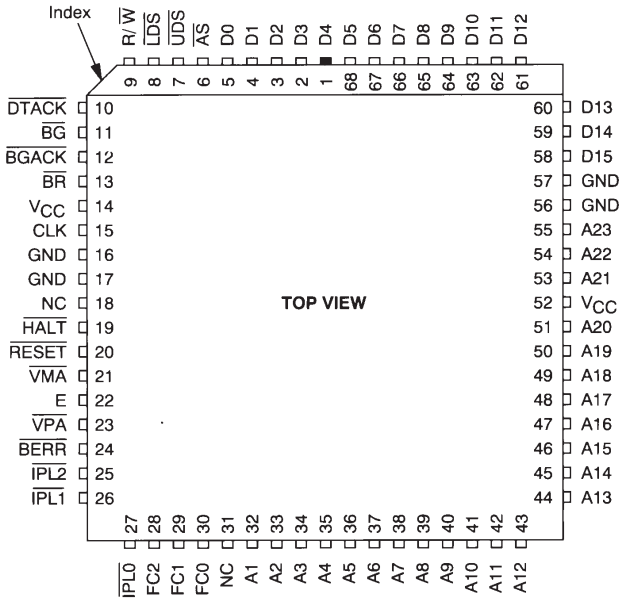


Figure 2.3 : 68-lead quad pack

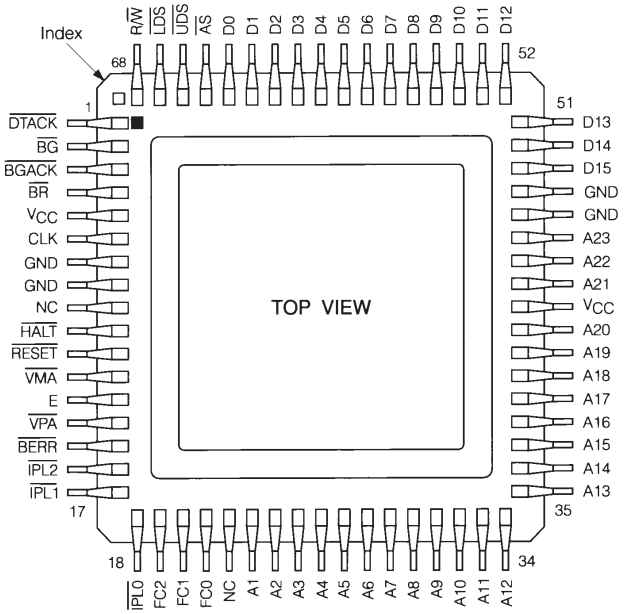


Figure 2.4 : 68-ceramic quad flat pack.

3 - TERMINAL DESIGNATIONS

The function, category and relevant symbol of each terminal of the device are given in the following table :

Table 1

Symbol	Function	Category
V_{CC}	Power supply (2 terminals)	Supply
V_{SS}	Power supply (2 terminals)	Terminals
FC0 to FC2	Processor status	Outputs
$\overline{IPL0}$ to $\overline{IPL2}$	Interrupt control	Inputs
A1 to A23	Address Bus	Outputs
AS	Asynchronous Bus Control	Outputs
R / $\overline{W}$		
$\overline{UDS}$		
$\overline{LDS}$		
$\overline{DTACK}$		Input
$\overline{BR}$	Bus arbitration Control	Inputs
$\overline{BGACK}$		
$\overline{BG}$		Output
$\overline{BERR}$	System control	Input
$\overline{RESET}$		Input / Output
$\overline{HALT}$		
$\overline{VPA}$	6800 peripheral control	Input
$\overline{VMA}$		Output
E		Output
CLK	Clock	Input
D0 to D15	Data Bus	Input / Output

* V_{SS} is the reference terminal for the voltages.

4 - SIGNAL DESCRIPTION

The input and output signals are illustrated functionnally in Figure 3 and are described in the following paragraphs.

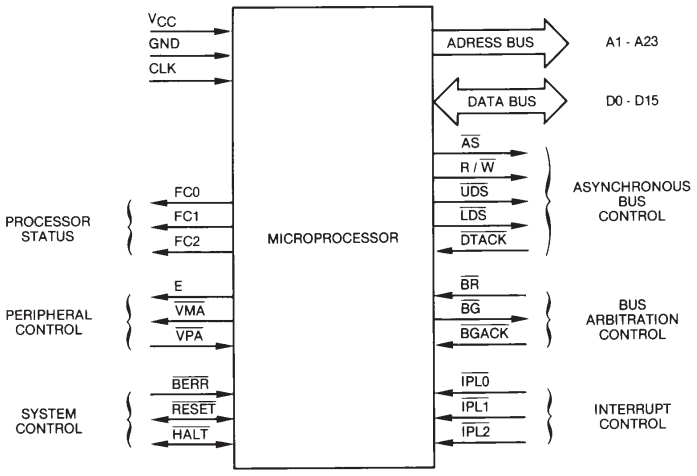


Figure 3 : Input and output signals.

Table 2 - Data strobe control of data bus

$\overline{UDS}$	$\overline{LDS}$	R / $\overline{W}$	D8-D15	D0-D7
High	High		No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	Valid data bits 8-15

ADDRESS BUS (A1 THROUGH A23)

This 24-bit, unidirectional, three-state bus is capable of addressing 16 megabytes of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2 and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are set to a logic high.

DATA BUS (D0 THROUGH D15)

This 16-bit, bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-D7.

ASYNCHRONOUS BUS CONTROL

Asynchronous data transfers are handled using the following control signals : address strobe, read / write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

ADDRESS STROBE ($\overline{AS}$)

This signal indicates that there is a valid address on the address bus.

READ / WRITE (R / $\overline{W}$)

This signal defines the data bus transfer as a read or write cycle. The R / $\overline{W}$ signal also works in conjunction with the data strobes as explained in the following paragraph.

UPPER AND LOWER DATA STROBE ($\overline{UDS}$, $\overline{LDS}$)

These signals control the flow of data on the data bus, as shown in Table 2. When the R / $\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R / W line is low, the processor will write to the data bus as shown.

DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$)

This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

BUS ARBITRATION CONTROL

The three signals, bus request, bus grant, and bus grant acknowledge, form a bus arbitration circuit to determine which device will be the bus master device.

BUS REQUEST ($\overline{BR}$)

This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

BUS GRANT ($\overline{BG}$)

This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

BUS GRANT ACKNOWLEDGE ($\overline{BGACK}$)

This input indicates that some other device has become the bus master. This signal should not be asserted until the following four conditions are met :

1 - a bus grant has been received,

2 - address strobe is inactive which indicates that the microprocessor is not using the bus,

3 - data transfer acknowledge is inactive which indicates that neither memory nor peripherals are using the bus, and

4 - bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$)

These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. Level seven cannot be masked. The least significant bit is given in IPL0 and the most significant bit is contained in $\overline{IPL2}$. These lines must remain stable until the processor signals interrupt acknowledge (FC0-FC2 are all high) to insure that the interrupt is recognized.

SYSTEM CONTROL

The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

BUS ERROR ($\overline{BERR}$)

This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of :

1 - nonresponding devices,

2 - interrupt vector number acquisition failure,

3 - illegal access request as determined by a memory management unit, or

4 - other application dependent errors.

The bus error signal interacts with the halt signal to determine if the current bus cycle should be re-executed or if exception processing should be performed.

RESET ($\overline{RESET}$)

This bidirectional signal line acts to reset (start a system initialization sequence) to processor in response to an external reset signal. An internally generated reset (result of a $\overline{RESET}$ instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external $\overline{HALT}$ and $\overline{RESET}$ signals applied at the same time.

HALT ($\overline{HALT}$)

When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state.

When the processor has stopped executing instructions, such as in a double bus fault condition, the $\overline{HALT}$ line is driven by the processor to indicate to external devices that the processor has stopped.

EF 6800 PERIPHERAL CONTROL

These control signals are used to allow the interfacing of synchronous EF 6800 peripheral devices with the asynchronous TS 68C000. These signals are explained in the following paragraphs.

ENABLE (E)

This signal is the standard enable signal common to all EF 6800 type peripheral devices. The period for this output is ten TS 68C000 clock periods (six clocks low, four clocks high). Enable is generated by an internal ring counter which may come up in any state (i.e., at power on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

VALID PERIPHERAL ADDRESS ($\overline{VPA}$)

This input indicates that the device or region addressed is an TS 68000 Family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt during an IACK cycle.

VALID MEMORY ADDRESS ($\overline{VMA}$)

This output is used to indicate to TS 68000 peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address ($\overline{VPA}$) input which indicates that the peripheral is an TS 68000 Family device.

PROCESSOR STATUS (FC0, FC1, FC2)

These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 3. The information indicated by the function code outputs is valid whenever address strobe ($\overline{AS}$) is active.

Table 3

Function code output			Cycle time
FC2	FC1	FC0	
Low	Low	Low	(Undefined, reserved)
Low	Low	High	User data
Low	High	Low	User program
Low	High	High	(Undefined, reserved)
High	Low	Low	(Undefined, reserved)
High	Low	High	Supervisor data
High	High	Low	Supervisor program
High	High	High	Interrupt Acknowledge

CLOCK (CLK)

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time and the clock signal must conform to minimum and maximum pulse width times. The clock is a constant frequency square wave with no stretching or shapping techniques required.

B · DETAILED SPECIFICATIONS

1 · SCOPE

This drawing describes the specific requirements for the microprocessor TS 68C000, 8, 10 and 12.5 MHz, in compliance with MIL-STD-883 class B.

2 · APPLICABLE DOCUMENTS

2.1 · MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-M-38510 : general specifications for microcircuits.

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be is shown in figures 2.1, 2.2, 2.3 and 2.4.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-M-38510 except finish C (as described in 3.5.6.1 of 38510).

3.2.3 · Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-M-38510 appendix C (when defined) :

- PGA 68 64 LEAD DIP
- 64 DIL SQ. LCC 68 PINS
- 68 LCCC 68 TERMINALS JCC
- 68 CQFP

The precise case outlines are described on figures 9.1, 9.2, 9.3 and 9.4 and into MIL-M-38510.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings (Table 4)

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 4 - Absolute maximum ratings

Unless otherwise stated, all voltages are referenced to the reference terminal as defined in Table 1, § A-3 of this specification.

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+6.5	V
V_I	Input voltage		−0.3	+6.5	V
V_O	Output voltage		NA	NA	V
V_{OZ}	Off state voltage		−0.3	11.0	V
I_o	Output currents		NA	NA	mA
I_i	Input currents		NA	NA	mA
P_{dmax}	Max power dissipation	T_{case} = −55°C		0.27	W
		T_{case} = +125°C		0.27	W
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+150	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

3.3.2 - Recommended conditions of use and guaranteed characteristics

a) Guaranteed characteristics (Tables 8 and 9)

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification is guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommanded operating ranges specified below.

b) Recommended conditions of use (Table 5)

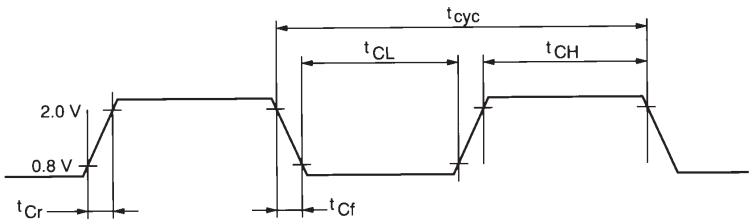
To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

These conditions shall not be for inspection purposes.

Some recommanded values may, however, be taken in other parts of this specification as detail conditions for an applicable test (Table 10).

c) Additionnal electrical characteristics (Table 10)

See § 5.5.2.



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high a voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 4 : Clock input timing diagram.

Table 5 - Recommended conditions of use

Unless otherwise stated, all voltages are referenced to the reference terminal as defined in Table 1, § A-3 of this specification.

Symbol	Parameter	Operating range			
		Model	Min	Max	Unit
V_{CC}	Supply voltage	All	4.5	5.5	V
V_{IL}	Low level input voltage	All	0	0.8	V
V_{IH}	High level input voltage (see also § 3.3.3)	All	2.0	V_{CC}	V
T_{case}	Operating temperature	All	– 55	+ 125	°C
R_L	Value of output load resistance	All	Note		Ω
C_L	Output loading capacitance	All		Note	pF
$t_{r(c)}$	Clock rise time (see Figure 4)	All		10	ns
$t_{f(c)}$	Clock fall time (see Figure 4)	All		10	ns
f_c	Clock frequency (see Figure 4)	TS 68C000-8	4.0	8.0	MHz
		TS 68C000-10	4.0	10.0	MHz
		TS 68C000-12	4.0	12.5	MHz
t_{cyc}	Clock time (see Figure 4)	TS 68C000-8	125	250	ns
		TS 68C000-10	100	250	ns
		TS 68C000-12	80	250	ns
$t_{w(CL)}$	Clock pulse width low (see Figure 4)	TS 68C000-8	55	125	ns
		TS 68C000-10	45	125	ns
		TS 68C000-12	35	125	ns
$t_{w(CH)}$	Cycle pulse width high (see Figure 4)	TS 68C000-8	55	125	ns
		TS 68C000-10	45	125	ns
		TS 68C000-12	35	125	ns

Note : Load networks number 1 to 4 as specified in § 5.4 (Figures 5.1 and 5.2) gives the maximum loading for the relevant output.

3.3.3 - Special recommended conditions for C.MOS devices

a) CMOS latch-up

The CMOS cell is basically composed of two complementary transistors (a P-channel and an N-channel), and, in the steady state, only one transistor is turned-on. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus the overall result is extremely low power consumption because there is no power loss through the active P-channel transistor. Also since only once transistor is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become «latched» in a mode that may result in excessive current drain and eventual destruction of the device. Although the device is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltages specification is not exceeded from voltage transients ; others may require no additional circuitery.

b) CMOS applications

– The TS 68C000 completely satisfies the input/output drive requirements of CMOS logic devices.

– The HCMOS TS 68C000 provides an order of magnitude power dissipation reduction when compared to the HMOS TS 68000. However, the TS 68C000 does not offer a «power down» or «halt» mode. The minimum operating frequency of the TS 68C000 is 4 MHz.

3.4 · Thermal characteristics

Table 6

Package	Symbol	Parameter	Value	Unit
DIL 64	θ J-A	Thermal resistance Junction to Ambient	25	°C/W
	θ J-C	Thermal resistance Junction to Case	6	°C/W
PGA 68	θ J-A	Thermal resistance Junction to Ambient	30	°C/W
	θ J-C	Thermal resistance Junction to Case	6	°C/W
LCCC 68	θ J-A	Thermal resistance Junction to Ambient	40	°C/W
	θ J-C	Thermal resistance Junction to Case	8	°C/W
CQFP 68	θ J-A	Thermal resistance Junction to Ambient	40	°C/W
	θ J-C	Thermal resistance Junction to Case	10	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification

- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurements conditions are given below :

- Table 7 : Static electrical characteristics for all electrical variants.
- Tables 8 and 9 : Dynamic electrical characteristics for 8, 10 and 12.5 MHz.

For static characteristics (Table 7), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause § 5.4 of this specification (Tables 8 and 9).

Indication of «min.» or «max.» in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause § 3.3.2 here above.

5.2 - Static characteristics

V_{CC} = 5.0 V V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55 / +125°C and T_C = −40°C / +85°C.

Table 7

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
1	I_{CC}	Supply current	41	V_{CC} = 5.5 V F_C = 8 MHz F_C = 10 MHz F_C = 12 MHz	All		42 45 50	mA
2	V_{OL} (1)	Low level output voltage for : A1 to A23 FC0 to FC2 ; $\overline{BG}$	37	V_{CC} = 4.5 V I_{OL} = 3.2 mA	25°C max min		0.5	V
3	V_{OL} (2)	Low level output voltage for : $\overline{HALT}$	37	V_{CC} = 4.5 V I_{OL} = 1.6 mA	25°C max min		0.5	V
4	V_{OL} (3)	Low level output voltage for : $\overline{AS}$; R/$\overline{W}$: D0 to D15 UDS ; $\overline{LDS}$; $\overline{VMA}$ and E	37	V_{CC} = 4.5 V I_{OL} = 5.3 mA	25°C max min		0.5	V
5	V_{OL} (4)	Low level output voltage for : $\overline{RESET}$	37	V_{CC} = 4.5 V I_{OL} = 5.0 mA	25°C max min		0.5	V
6	V_{OH}	High level output voltage for all outputs	37	V_{CC} = 4.5 V I_{OH} = −400 µA	25°C max min	2.4	V_{CC} −0.75	V
7	I_{IH} (1)	High level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5 V V_I = 5.5 V	25°C max min		2.5	µA
8	I_{IL} (1)	Low level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5 V V_I = 0 V	25°C max min	−2.5		µA

Table 7 (Continued)

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
9	I_{IH} (2)	High level input current for : $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5 V V_I = 5.5 V	25°C max min		20	µA
10	I_{IL} (2)	Low level input current for $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5 V V_I = 0 V	25°C max min	– 20		µA
11	I_{OHZ}	High level output 3-state leakage current		V_{CC} = 5.5 V V_{OH} = 2.4 V	25°C max min		20	µA
12	I_{OLZ}	Low level output 3-state leakage current		V_{CC} = 5.5 V V_{OL} = 0.4 V	25°C max min		20	µA
13	V_{IH}	High level input voltage for all inputs		V_{CC} = 4.5 V V_{CC} = 5.5 V	25°C max min	2.0		V
14	V_{IL}	Low level input voltage for all inputs		V_{CC} = 4.5 V V_{CC} = 5.5 V	25°C max min		0.8 0.8 0.8	V V V
14A	C_{in}	Input capacitance (all inputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C max min		25 NA NA	pF pF pF
14B	C_{out}	Output capacitance (all inputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C max min		20 NA NA	pF pF pF
14C	V_{test}	Internal protection Transient energy rating		See Note 9 5 cycles	25°C	– 500	+ 500	V

* Algebraic values.
** Measurement method : see § 5.1. and 5.4.
Refered notes are given in § 5.4.4.

5.3 · Dynamic characteristics

V_{CC} = 5.0 V V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = – 55 / + 125°C and T_C = – 40°C / + 85°C.

Table 8A · Dynamic characteristics · TS 68C000-8

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
27	t_{su} (DICL)	Set-up time Data-in to clock low (Note 1)	6 - 7	See 5.4.3 (a) to (c) f_C = 8 MHz	25°C max min	20 Note 10		ns
47	t_{su} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns
47	t_{su} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns
47	t_{su} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns
47	t_{su} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns

Table 8A · Dynamic characteristics · TS 68C000-8 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
47	t_{su} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns
2	t_W (CL)	Clock width low	6 - 7	Idem test 27	25°C max min	55 Note 10	125	ns
3	t_W (CH)	Clock width high	6 - 7	Idem test 27	25°C max min	55	125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	6 - 7	Idem test 27 Load : 3	25°C max min		70	ns
9	t_{PHL} (CHSLX)	Propagation time clock high to $\overline{AS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to $\overline{LDS}$, $\overline{UDS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{AS}$ high	6 - 7	Idem test 27 Load : 4	25°C max min		70 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{LDS}$, $\overline{UDS}$ high	6 - 7	Idem test 27 Load : 4	25°C max min		70 Note 3	ns
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/$\overline{W}$ high	6 - 7	Idem test 27 Load : 4	25°C max min		70 Note 3	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/$\overline{W}$ low	6 - 7	Idem test 27 Load : 4	25°C max min		70 Note 3	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	6 - 7	Idem test 27 Load : 4	25°C max min		70 Note 3	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	6 - 7	Idem test 27 Load : 3	25°C max min		70	ns
32	t_{HRRF}	$\overline{RESET}$ / $\overline{HALT}$ input transition time	6 - 7	Idem test 27	25°C max min		200	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to $\overline{BG}$ low	8	Idem test 27 Load : 3	25°C max min		70	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to $\overline{BG}$ high	8	Idem test 27 Load : 3	25°C max min		70	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	9	Idem test 27 Load : 4	25°C max min		70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	9	Idem test 27 Load : 4	25°C max min		70	ns
8	t_h (SHAZ)	Hold time CLK high to Address	6 - 7	Idem test 27 Load : 3	25°C max min	0		ns

Table 8A - Dynamic characteristics - TS 68C000-8 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
11	t_{su} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min	30 Note 4		ns
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 +90	CLKS Note 2 ns
37	t_{PLH} (GALEH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 +90	CLKS Note 2 ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	7	Idem test 27	25°C max min	20 Note 5	—	ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	6 - 7	Idem test 27	25°C max min	20 Note 5	—	ns
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	7	Idem test 27 Load : 4	25°C max min	30 Note 4	—	ns

* Algebraic values.
** Measurement method : see § 5.4.
Refered notes are given in § 5.4.4.

Table 8B - Dynamic characteristics - TS 68C000-10

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
27	t_{su} (DICL)	Set-up time Data-in to clock low (Note 1)	6 - 7	See 5.4.3 (a) to (c) f_C = 10 MHz	25°C max min	20 Note 10		ns
47	t_{su} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns
47	t_{su} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns
47	t_{su} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns
47	t_{su} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns
47	t_{su} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 10		ns
2	t_w (CL)	Clock width low	6 - 7	Idem test 27	25°C max min	45	125	ns
3	t_w (CH)	Clock width high	6 - 7	Idem test 27	25°C max min	45	125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	6 - 7	Idem test 27 Load : 3	25°C max min		60	ns

Table 8B · Dynamic characteristics - TS 68C000-10 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
9	t_{PHL} (CHSLX)	Propagation time clock high to AS low	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to LDS, UDS low	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to AS high	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to LDS, UDS high	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/W high	6 - 7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/W low	6 - 7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	6 - 7	Idem test 27 Load : 4	25°C max min		60	ns
32	t_{HRRF} (CHGL)	RESET / HALT transition time	6 - 7	Idem test 27	25°C max min		200	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to BG low	8	Idem test 27 Load : 3	25°C max min		60	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to BG high	8	Idem test 27 Load : 3	25°C max min		60	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to VMA low	9	Idem test 27 Load : 4	25°C max min		70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	9	Idem test 27 Load : 4	25°C max min		55	ns
8	t_h (SHAZ)	Hold time CLK high to Address	6 - 7	Idem test 27 Load : 3	25°C max min	0		ns
11	t_{su} (AVSL)	Set-up time Address valid to AS, LDS, UDS low	6 - 7	Idem test 27 Load : 4	25°C max min	20 Note 4		ns
35	t_{PHL} (BRLGL)	Propagation time BR low to BG low	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 + 80	CLKS Note 2 ns
37	t_{PLH} (GALGH)	Propagation time BGACK low to BG high	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 + 80	CLKS Note 2 ns
48	t_{su} (BELDAL)	Set-up time BERR low to DTACK low	7	Idem test 27	25°C max min	20 Note 5		ns

Table 8B · Dynamic characteristics - TS 68C000-10 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	6 - 7	Idem test 27	25°C max min	 20 Note 5		ns
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	7	Idem test 27 Load : 4	25°C max min	 20 Note 4		ns
* Algebraic values. ** Measurement method : see § 5.4. Refered notes are given in § 5.4.4.								

Table 8C · Dynamic characteristics - TS 68C000-12

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
27	t_{su} (DICL)	Set-up time Data-in to clock low (Note 1)	6 - 7	See 5.4.3 (a) to (c) f_C = 12 MHz	25°C max min	 10 Note 10		ns
47	t_{su} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 10		ns
47	t_{su} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 10		ns
47	t_{su} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 10		ns
47	t_{su} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 10		ns
47	t_{su} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 10		ns
2	t_W (CL)	Clock width low	6 - 7	Idem test 27	25°C max min	 35	125	ns
3	t_W (CH)	Clock width high	6 - 7	Idem test 27	25°C max min	 35	125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	6 - 7	Idem test 27 Load : 3	25°C max min		55	ns
9	t_{PHL} (CHSLX)	Propagation time clock high to $\overline{AS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to $\overline{LDS}$, $\overline{UDS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{AS}$ high	6 - 7	Idem test 27 Load : 4	25°C max min		50 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{LDS}$, $\overline{UDS}$ high	6 - 7	Idem test 27 Load : 4	25°C max min		50 Note 3	ns

Table 8C - Dynamic characteristics - TS 68C000-12 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/$\overline{W}$ high	6 - 7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/$\overline{W}$ low	7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	6 - 7	Idem test 27 Load : 4	25°C max min		55	ns
32	t_{HRRF}	$\overline{RESET}$ / $\overline{HALT}$ transition time	6 - 7	Idem test 27	25°C max min		150	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to $\overline{BG}$ low	5	Idem test 27 Load : 3	25°C max min		50	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to $\overline{BG}$ high	8	Idem test 27 Load : 3	25°C max min		50	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	9	Idem test 27 Load : 4	25°C max min		70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	9	Idem test 27 Load : 4	25°C max min		45	ns
8	t_h (SHAZ)	Hold time CLK high to Address	6 - 7	Idem test 27 Load : 3	25°C max min	0		ns
11	t_{su} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min	15 Note 4		ns
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 + 70	CLKS Note 2 ns
37	t_{PLH} (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 + 70	CLKS Note 2 ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	7	Idem test 27	25°C max min	20 Note 5		ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	6 - 7	Idem test 27	25°C max min	20 Note 5		ns
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	7	Idem test 27 Load : 4	25°C max min	15 Note 4		ns

* Algebraic values.

** Measurement method : see § 5.4.

Refered notes are given in § 5.4.4.

Table 9 - AC electrical specification - clock timing

Symbol	Parameter	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f	Frequency of operation	4.0	8.0	4.0	10.0	4.0	12.5	MHz
t_{cyc}	Cycle time	125	250	100	250	80	250	ns
t_{CL} t_{CH}	Clock pulse width	55 55	125 125	45 45	125 125	35 35	125 125	ns
t_{Cr} t_{Cf}	Rise and fall time		10 10		10 10		10 10	ns

5.4 - Test conditions specific to the device

5.4.1 - Loading network

The applicable loading network shall be as defined in column «Test conditions» of Tables 8, refering to the loading network number as shown in Figures 5.1 and 5.2 below.

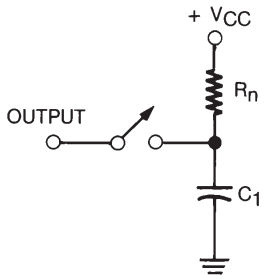


Figure 5.1 : Passive loads.

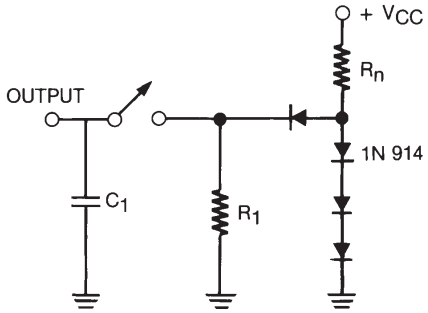


Figure 5.2 : Active loads.

Load NBR	Figure	R_1	R_n	C_1*	Output application
1	5.1	—	910 Ω	130 pF	$\overline{\text{RESET}}$
2	5.1	—	2.9 kΩ	70 pF	$\overline{\text{HALT}}$
3	5.2	6.0 k	1.22 kΩ	130 pF	A1 to A23, $\overline{\text{BG}}$ and FC0 to FC2
4	5.2	6.0 k	740 Ω	130 pF	All other outputs
* C_1 includes all parasitic capacitances of test machines.					

5.4.2 · Time definitions

The times specified in Table 8 as dynamic characteristics are defined in Figures 6 to 9 below by a reference number given in the column «Method» of the tables together with the relevant figure number.

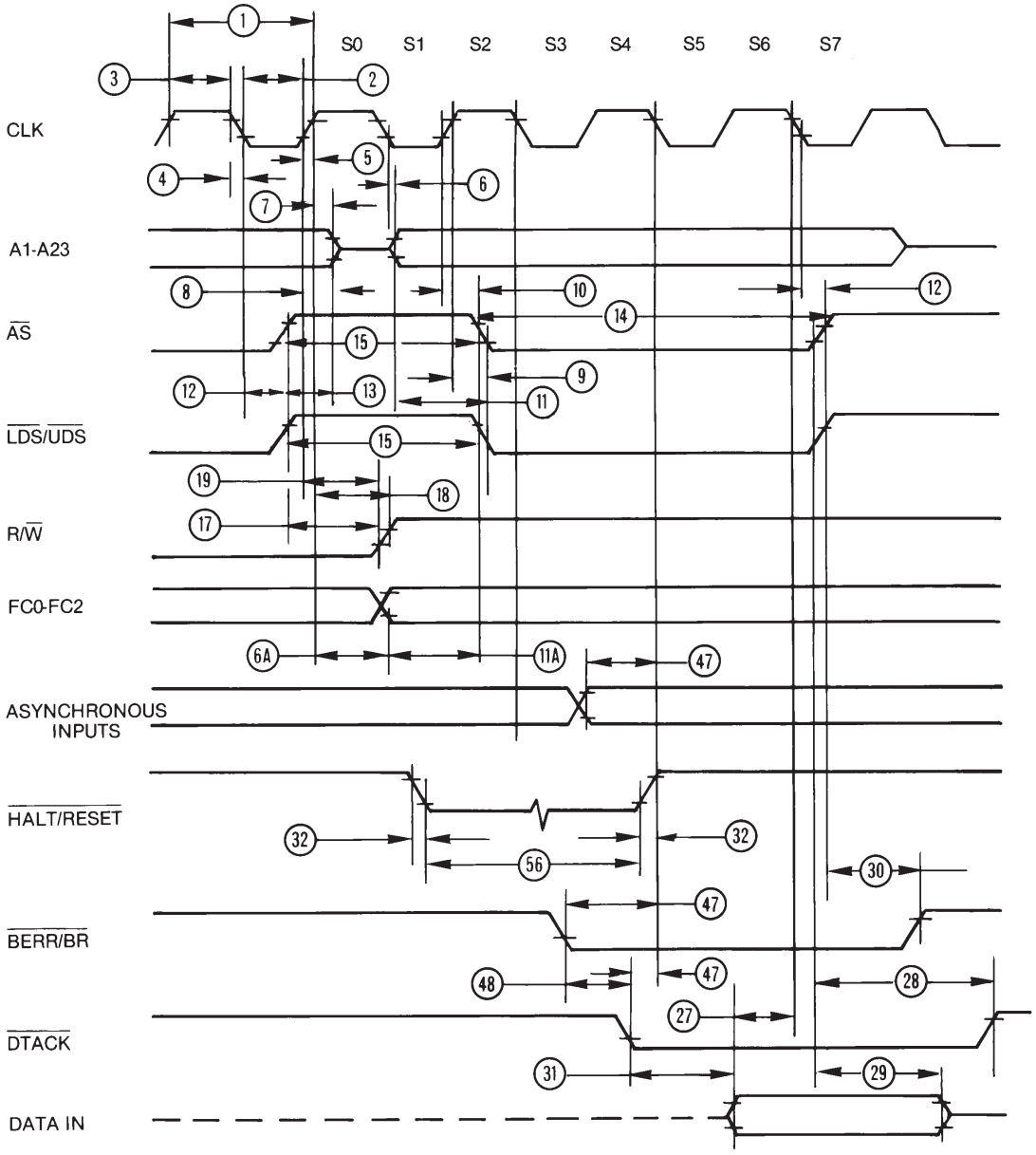


Figure 6 : Read cycle timing.

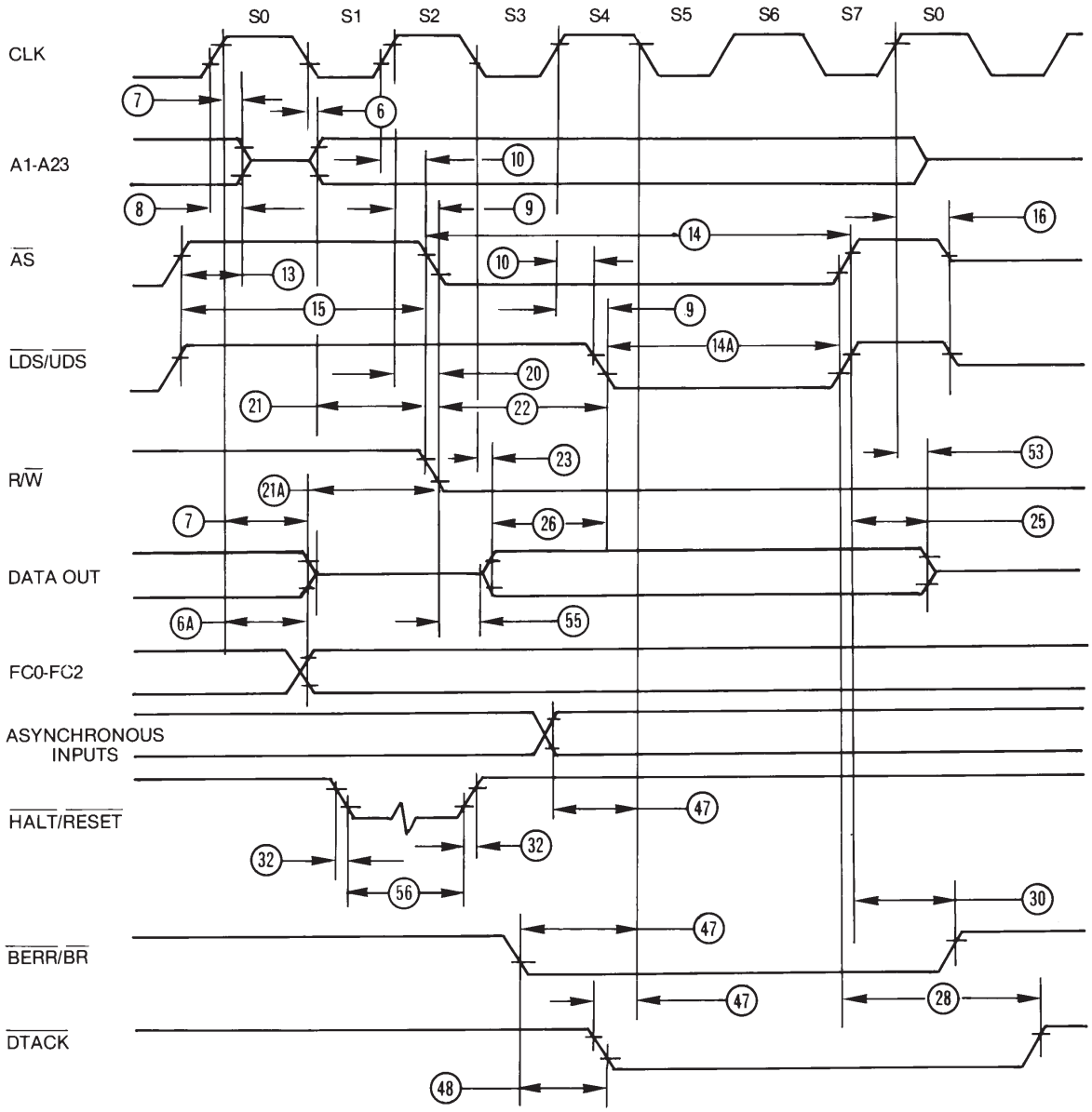


Figure 7 : Write cycle timing.

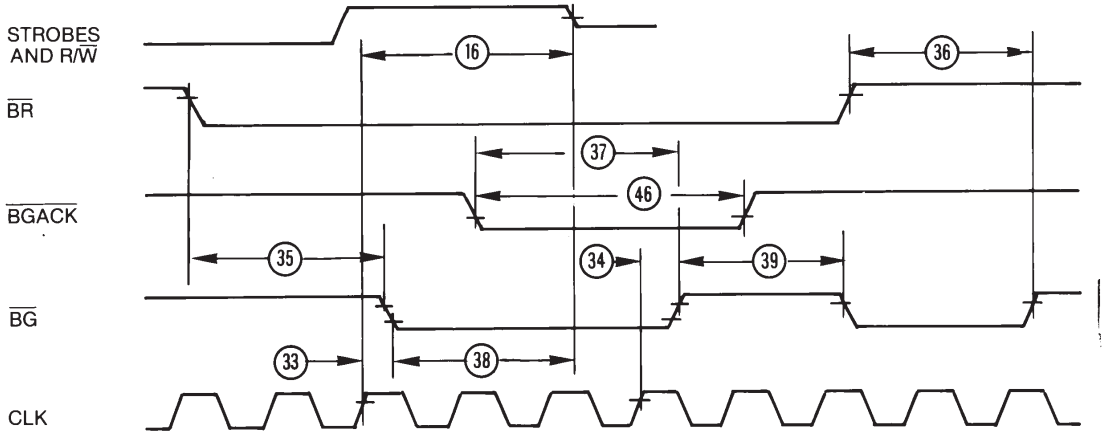


Figure 8 : AC electrical waveforms - bus arbitration.

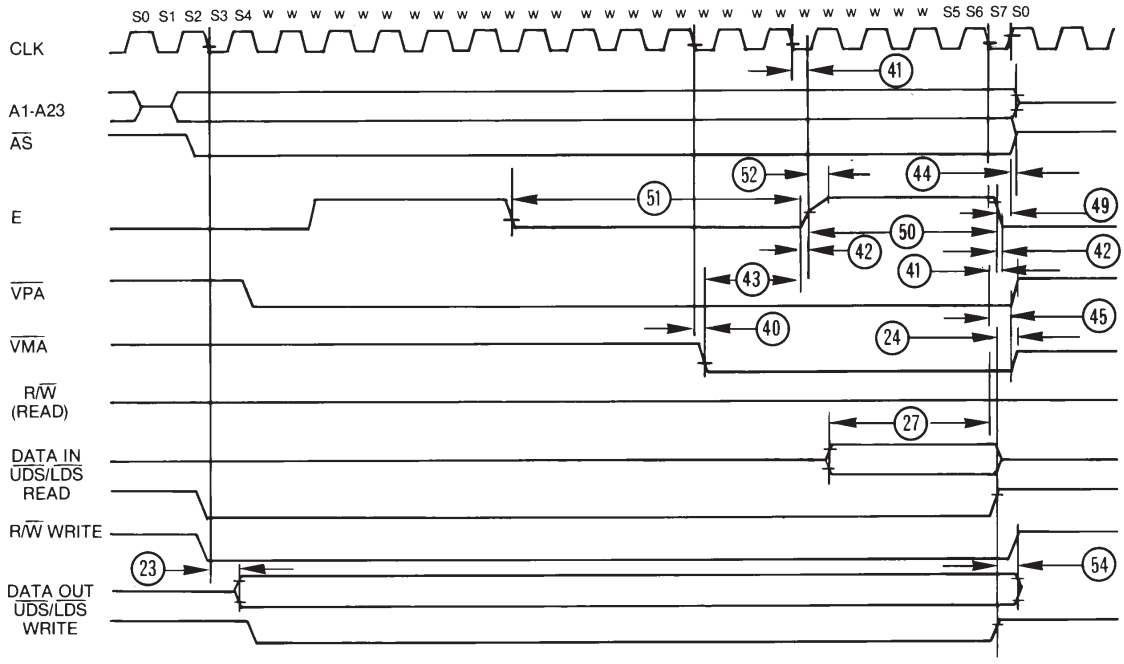


Figure 9 : Enable / interface timing.

5.4.3 · Input and output signals for dynamic measurements

a) Input pulse characteristics

Where input pulse generator is loaded by only a 50 Ω resistor, the input pulse characteristics shall be as shown in Figure 10.

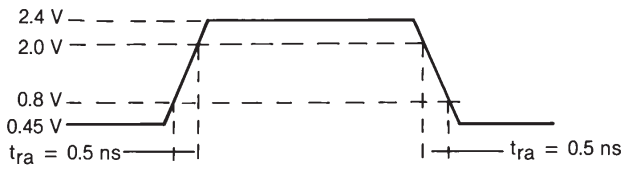


Figure 10 : Input pulse characteristics.

b) Time measurement input voltage references

Input voltages which are taken as reference for time measurement shall be :

V_{IL} = 0.8 V

V_{IH} = 2.0 V

c) Time measurement output voltage reference for valid state output

Where output ios (or becomes to) valid state, the output voltages which are taken as reference for time measurements, shall be as shown in Figure 11.

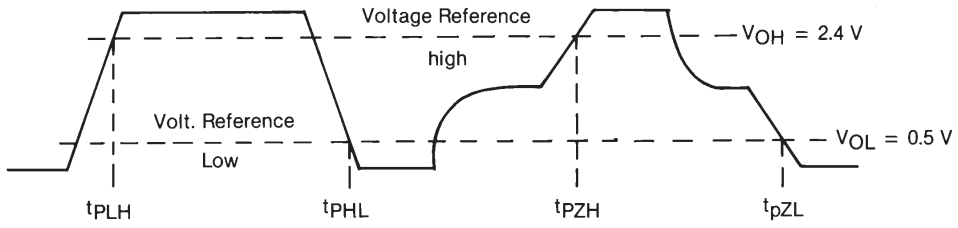


Figure 11 : Output voltage references.

5.4.4 · Refered notes to the Tables 7 and 8

The following notes shall apply where refered into the Tables 8 and 9 and/or additional information given in § 5.5.2 of this specification.

Note 1 : If the asynchronous setup time (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.

Note 2 : Where «CLKS» is stated as unit time limit, the relevant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.

Note 3 : For a loading capacitance of less than or equal to 50 picofarads, substract 5 nanoseconds from the value given in the maximum columns.

Note 4 : Actual value depends on actual period.

Note 5 : If 47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, 48 may be 0 nanoseconds.

Note 6 : The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.

Note 7 : The falling edge of 56 triggers both the negation of the strobes ($\overline{AS}$, and X DS) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

Note 8 : When $\overline{AS}$ and R / $\overline{W}$ are equally loaded (± 20 %), substract 10 nanoseconds from the values in these columns.

Note 9 : Each terminal of the device under test shall be tested separately against all existing V_{CC} and V_{SS} terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the both limits as given in Table 8.

Note 10 : This value should be treated as a minimum for design purpose. For the conformance testing the value shall be regarded as the maximum time.

5.5 - Additional information

Additional information shall not be for any inspection purposes.

5.5.1 - Power considerations

See § 3.4.

5.5.2 - Additional electrical characteristics

The following additional characteristics, which are obtained from circuit design, are given for information only.

Unless otherwise stated, for dynamic additional characteristics, the given reference numbers refer to Figures 6 to 9 and loading number refer to Figures 5.1 and 5.2 (see § 5.4 of this specification).

The given limits should be valid for all operating temperature ranges as defined in § 3.3.2 of this specification.

Table 10

Item Nbr	Symbol	Parameter	Ref Nbr	Load Nbr	TS 68C000-8 Limits		TS 68C000-10 Limits		TS 68C000-12 Limits		Unit
					Min	Max	Min	Max	Min	Max	
6A	V_{OH}	High level output voltage for E with pullup R = 1.1 K to V_{CC}			min	V_{CC} - 0.75	min	V_{CC} - 0.75	min	V_{CC} - 0.75	V
37	t_{PLZ} t_{PHZ} (CLAZX)	Propagation time CLK low to Address 3-state	Fig. 6 Ref. 7	3		80		70		60	ns
39	t_{PHZ} (CHSZX)	Propagation time CLK high to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ 3-state	Fig. 7 Ref. 16	4		80		70		60	ns
40	t_{PLZ} t_{PHZ} (CHRZ)	Propagation time CLK high to R / $\overline{W}$ 3-state	Fig. 8 Ref. 16	4		80		70		60	ns
41	t_{PHZ} t_{PLZ} (CHAZX)	Propagation time CLK high to Data 3-state	Fig. 7 Ref. 7	4		80		70		60	ns
43	t_h (SHAZ)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to Address	Fig. 6 Ref. 13	3	30		20		10		ns
44	t_w (SL)	$\overline{AS}$/DS width low	Fig. 6 Ref. 14		240 Note 4		195 Note 4		160 Note 4		ns
45	t_w (SL)	$\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ width high	Fig. 6 Ref. 15		150 Note 4		105 Note 4		65 Note 4		ns
46	t_{su} (SHRH)	Set-up time $\overline{LDS}$, $\overline{UDS}$ high to R / $\overline{W}$ high	Fig. 6 Ref. 17	4	40 Note 4		20 Note 4		10 Note 4		ns
47	t_{su} (AVRL)	Set-up time Address valid to R / $\overline{W}$ low	Fig. 6 Ref. 21	4	20 Note 4		0 Note 4		0 Note 4		ns

Table 10 (Continued)

Item Nbr	Symbol	Parameter	Ref Nbr	Load Nbr	TS 68C000-8 Limits Min	TS 68C000-8 Limits Max	TS 68C000-10 Limits Min	TS 68C000-10 Limits Max	TS 68C000-12 Limits Min	TS 68C000-12 Limits Max	Unit
48	t_{PHL} (RLSL)	Propagation time R / $\overline{W}$ low to lds, uds low	Fig. 7 Ref. 22	4	80 Note 4		50 Note 4		30 Note 4		ns
49	t_h (SHDO)	Hold time $\overline{LDS}$, $\overline{UDS}$ high to Data-out	Fig. 7 Ref. 25	4	30 Note 4		20 Note 4		15 Note 4		ns
50	t_h (SHDI)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to Data-in	Fig. 6 Ref. 29		0		0		0		ns
52	t_h (BRHGH)	Propagation time $\overline{BR}$ high to $\overline{BG}$ high (Note 6)	Fig. 8 Ref. 36	3	1.5	3.5 +90	1.5	3.5 +80	1.5	3.5 +70	CLKS Note 2 ns
54	t_{PHZ} t_{PLZ} (GLZ)	Propagation time $\overline{BG}$ low to Data and Address 3-state	Fig. 8 Ref. 36	BG, address 3 Data 4		80		70		60	ns
55	t_w (GH)	$\overline{BG}$ width high	Fig. 8 Ref. 39		1.5		1.5		1.5		CLKS ns
56	t_{PLH} (VMLEH)	Propagation time $\overline{VMA}$ low to E high	Fig. 9 Ref. 43	4	200		150		90		ns
57	t_h (SHVPH)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to VPA high	Fig. 20 Ref. 44 (see § 6.6.3)	4	0	120	0	90	0	70	ns
58	t_h (ELAI)	Hold time E low to address	Fig. 9 Ref. 45	3	30		10		10		ns
59	t_w (BGL)	$\overline{BGACK}$ width low	Fig. 8 Ref. 46		1.5		1.5		1.5		CLKS Note 2
61	t_w (EH)	E width high	Fig. 9 Ref. 50		450		350		280		ns
62	t_w (EL)	E width low	Fig. 9 Ref. 51		700		550		440		ns
63	t_{PHL} (FCVSL)	Propagation time FC valid to $\overline{AS}$, $\overline{DS}$ low	Fig. 6 Ref. 1A or 11A	4	60 Note 4		50 Note 4		40 Note 4		ns
64	t_{PHL} (SHDAH)	Propagation time $\overline{AS}$, $\overline{DS}$ high to $\overline{DTACK}$ high	Fig. 6 Ref. 28	4	0	245 Note 4	0	190 Note 4	0	150 Note 4	ns
65	t_{PLH} (SHBEH)	Propagation time $\overline{AS}$, $\overline{DS}$ high to $\overline{BERR}$ high	Fig. 8 Ref. 30	4	0		0		0		ns
66	t_{su} (DALDI)	Set-up time $\overline{DTACK}$ low to Data-in (Note 1)	Fig. 6 Ref. 31			90 Note 4		65 Note 4		50 Note 4	ns
67	t_{THL} t_{TLH} (RH)	Transition time $\overline{HALT}$, $\overline{RESET}$ input	Fig. 6 Ref. 32			200		200		200	ns
69	t_w (HRPW)	$\overline{HALT}$ and $\overline{RESET}$ pulse width after power up	Fig. 6 Ref. 56		10		10		10		CLKS Note 2
70	t_{PHL} (ASRV)	Propagation time $\overline{AS}$ low to R / $\overline{W}$ valid	Fig. 7 Ref. 20A	4		20 Note 8		20 Note 8		20 Note 8	ns
71	t_{PHL} (FCVRL)	Propagation time FC valid to R / $\overline{W}$ low	Fig. 7 Ref. 21A	4	60 Note 4		50 Note 4		30 Note 4		ns
73	t_h (CHDOI)	Hold time CLK high to Data-out	Fig. 7 Ref. 53	4	0		0		0		ns
74	t_{PLH} t_{PHL} (RLDBO)	Propagation time R / $\overline{W}$ low to Data-bus impedance change	Fig. 7 Ref. 55	4	30		20		10		ns
75	t_{PHL} (SHEL)	Propagation time $\overline{AS}$, $\overline{DS}$ low to E low	Fig. 9 Ref. 49	4 Note 7	−70	+70	−55	+55	−45	+45	ns
76	t_h (ELDOI)	Hold time E low to Data-out	Fig. 9 Ref. 54	4	30		20		15		ns

Refered notes are given in § 5.4.4.

6 - FUNCTIONAL DESCRIPTION

6.1 - Description of registers

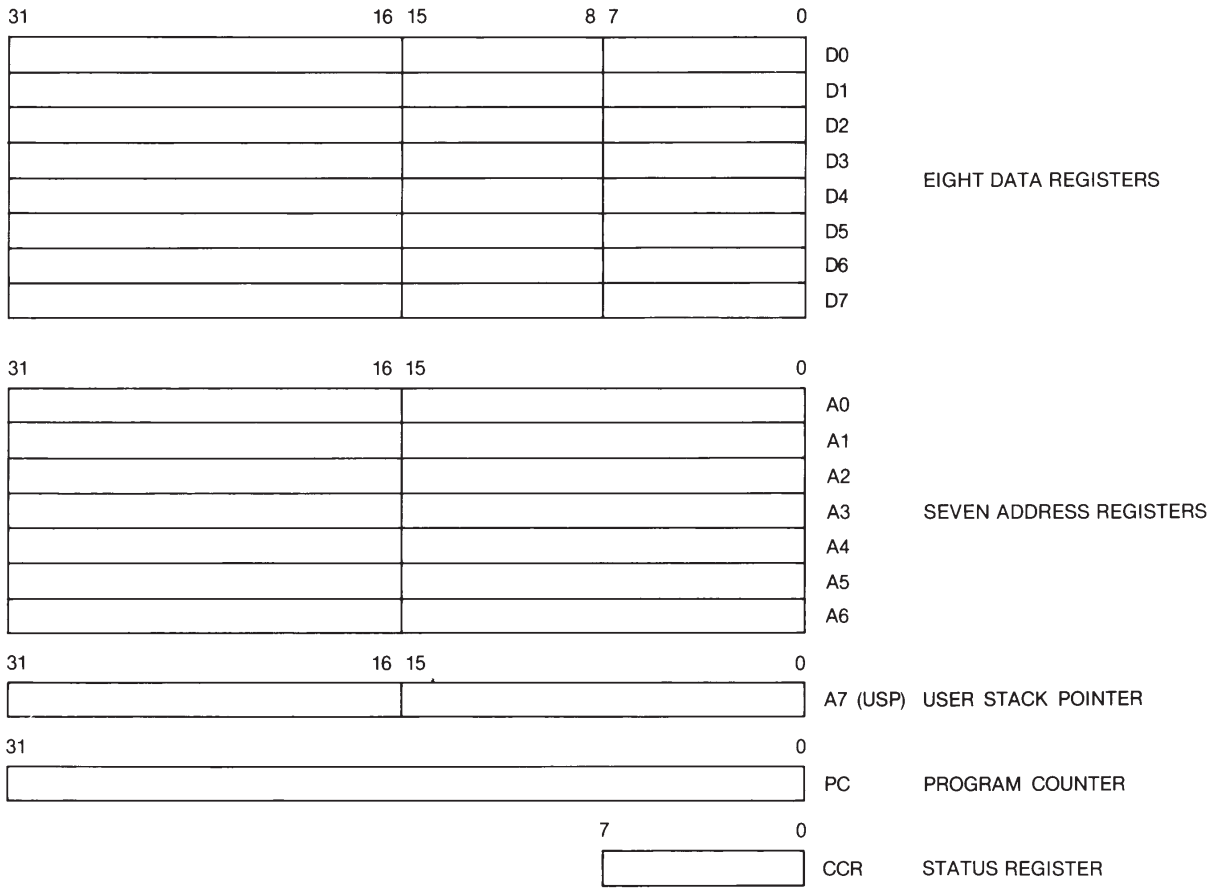


Figure 12 : User programming model.

As shown in the user programming model (Figure 12), the TS 68C000 offers 16/32-bit registers and a 32-bit program counter. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) operations. The second set of seven registers (A0-A6) and the user stack pointer (USP) may be used as software stack pointers and base address registers. In addition, the registers may be used for word and long word operations. All of the 16 registers may be used as index registers.

In supervisor mode, the upper byte of the status register and the supervisor stack pointer (SSP) are also available to the programmer. These registers are shown in Figure 13.

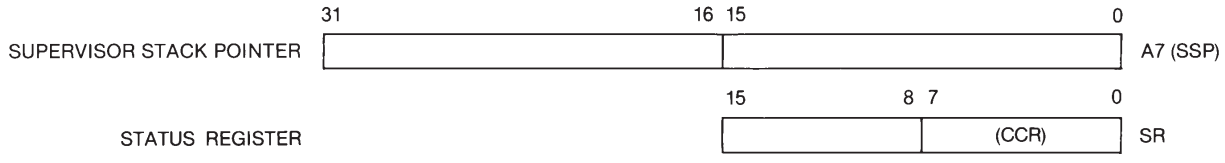


Figure 13 : Supervisor programming model supplement.

The status register (Figure 14) contains the interrupt mask (eight levels available) as well as the condition codes : extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

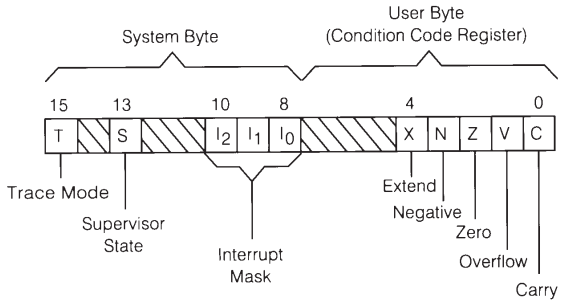


Figure 14 : Status register.

6.2 - Data types and addressing modes

Five basic data types are supported. These data types are :

- Bits
- BCD Digits (4 Bits)
- Bytes (8 Bits)
- Words (16 Bits)
- Long Words (32 Bits)

In addition, operations on other data types such as memory addresses, status word data, etc. are provided in the instruction set.

The 14 addressing modes, shown in Table 11, include six basic types :

- Register Direct
- Register Indirect
- Absolute
- Program Counter Relative
- Immediate
- Implied

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting, and indexing. The program counter relative mode can also be modified via indexing and offsetting.

6.3 - Data transfer operations

Transfer of data between devices involves the following leads :

1 - address bus A1 through A23,

2 - data bus D0 through D15, and

3 - control signals.

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the TS 68C000 for interlocked multiprocessor communications.

READ CYCLE

During a read cycle, the processor receives data from the memory of a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobes is issued. When the A0 bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions is internally.

WRITE CYCLE

During a write cycle, the processor sends data to either the memory of a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued.

Table 11 · Addressing modes

Addressing Modes	Syntax
Register Direct Addressing	
Data Register Direct	Dn
Address Register Direct	An
Absolute Data Addressing	
Absolute Short	xxx.W
Absolute Long	xxx.L
Program Counter Relative Addressing	
Relative with Offset	d_{16}(PC)
Relative with Index Offset	d_8(PC,Xn)
Register Indirect Addressing	
Register Indirect	(An)
Postincrement Register Indirect	(An) +
Predecrement Register Indirect	− (An)
Register Indirect with Offset	d_{16}(An)
Indexed Register Indirect with Offset	d_8(An,Xn)
Immediate Data Addressing	
Immediate	= XXX
uick Immediate	= 1- = 8
Implied Addressing	
Implied Register	SR / USP / SP / PC

Notes :

Dn = Data Register.
An = Address Register.
Xn = Address of Data Register used as Index Register.
SR = Status Register.
PC = Program Counter.
SP = Stack Pointer.
USP = User Stack Pointer.
( ) = Effective Address.
d_8 = 8-Bit Offset (Displacement).
d_{16} = 16-Bit Offset (Displacement).
= xxx = Immediate Data.

Table 12 · Instruction set summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
Bcc	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DBcc	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Lead Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical OR
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

READ-MODIFY-WRITE CYCLE

The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the datra back to the same address. In the TS 68C000, this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write are byte operations.

6.4 · Instruction set overview

The TS 68C000 instruction set is shown in Table 12. Some additional instructions are variations, or sub-sets, of these and they appear in Table 13. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned, multiply and divide, «quick» arithmetic operations, BCD arithmetic, and expanded operations (through traps).

Table 13 - Variations of instruction types

Instruction Type	Variation	Description
ADD	ADD ADDA ADDQ ADDI ADDX	Add Add Address Add Quick Add Immediate Add with Extend
AND	AND ANDI ANDI to CCR ANDI to SR	Logical AND And Immediate And Immediate to Condition Codes And Immediate to Status Register
CMP	CMP CMPA CMPM CMPI	Compare Compare Address Compare Memory Compare Immediate
EOR	EOR EORI EORI to CCR EORI to SR	Exclusive OR Exclusive OR Immediate Exclusive OR Immediate to Condition Codes Exclusive OR Immediate to Status Register
MOVE	MOVE MOVEA MOVEM MOVEP MOVEQ MOVE from SR MOVE to SR MOVE to CCR MOVE USP	Move Move Address Move Multiple Registers Move Peripheral Data Move Quick Move from Status Register Move to Status Register Move to Condition Codes Move User Stack Pointer
NEG	NEG NEGX	Negate Negate with Extend
OR	OR ORI ORI to CCR ORI to SR	Logical OR OR Immediate OR Immediate to Condition Codes OR Immediate to Status Register
SUB	SUB SUBA SUBI SUBQ SUBX	Subtract Subtract Address Subtract Immediate Subtract Quick Subtract Extend

6.5 - Processing states

The TS 68C000 is always in one of three processing states : normal, exception, or halted.

NORMAL PROCESSING

The normal processing state is that associated with instruction execution ; the memory references are to fetch instructions and operands, and to store results. A special case of normal state is the stopped state which the processor enters when a stop instruction is executed. In this state, no further references are made.

EXCEPTION PROCESSING

The exception processing state is associated with interrupts, trap instructions, tracing, and other exception conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

HALTED PROCESSING

The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus errors occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

Asserting the reset and halt line for ten cycles will cause a processor reset, except when V_{CC} is initially applied to the processor. In this case, an external reset must be applied for least 100 milliseconds.

6.6 - Interface with EF 6800 peripherals

Extensive line of EF 6800 peripherals are directly compatible with the TS 68C000.

Note : It is the own user's responsibility to verify the actual EF 6800 peripheral performances to be compatible to the actual used TS 68C000 microprocessor performances.

Some of the EF 6800 peripheral that are particulary useful are :

EF 6821 : Peripheral Interface Adapter

EF 6840 : Programmable Timer Module

EF 6850 : Asynchronous Communications Interface Adapter

EF 6852 : Synchronous Serial Data Adapter

EF 6854 : Advanced Data Link Controller

To interface the synchronous EF 6800 peripherals with the asynchronous TS 68C000, the processor modifies its bus cycle to meet the EF 6800 cycle requirements whenever an EF 6800 device address is detected. This is possible since both processors use memory mapped I/O. Figure 15 is a flowchart of the interface operation between the processor and EF 6800 devices.

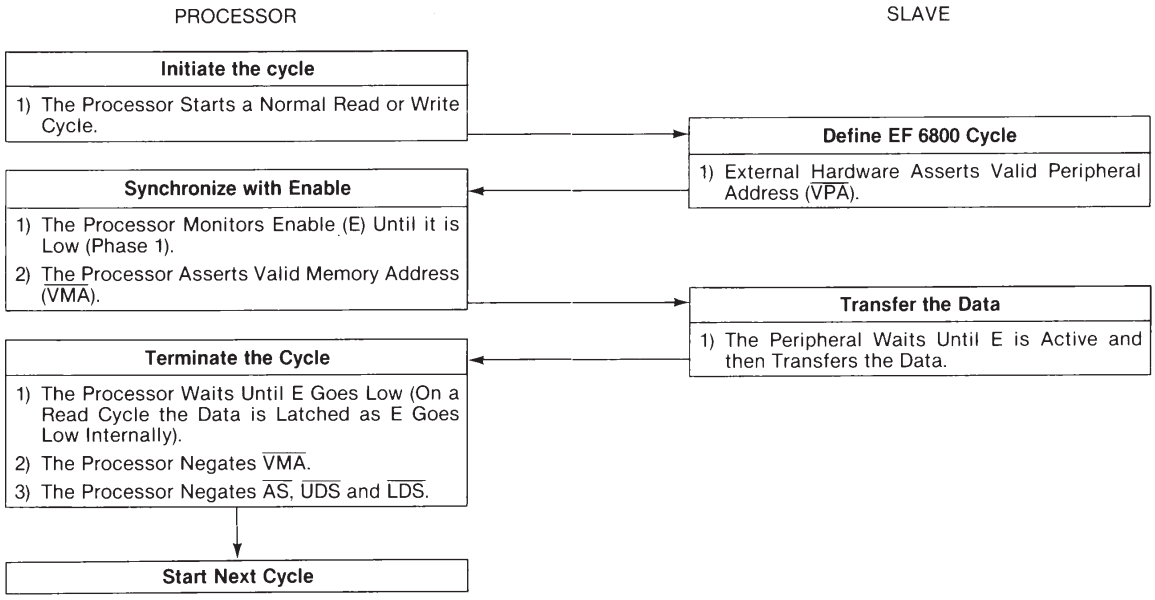


Figure 15 : EF 6800 interfacing flowchart.

6.6.1 · Data Transfer Operation

Three signals on the processor provide the EF 6800 interface. They are : enable (E), valid memory address ($\overline{VMA}$), and valid peripheral address ($\overline{VPA}$). Enable corresponds to the E or phase 2 signal in existing EF 6800 systems. The bus frequency is one tenth of the incoming TS 68C000 clock frequency. The timing of E allows 1 MHz peripherals to be used 8 MHz TS 68C000. Enable has a 60/40 duty cycle, that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive $\overline{VPA}$ accesses on successive E pulses.

EF 6800 cycle timing is given in Figures 16, 17, 19 and 20. At state zero (SO) in the cycle, the address bus is in the high-impedance state. A function code is asserted on the function code output lines. One-half clock later, in state 1, the address bus is released from the high-impedance state.

During state 2, the address strobe ($\overline{AS}$) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R / $\overline{W}$) signal is switched to low (write) during state 2. One-half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus. The processor now inserts wait states until it recognizes the assertion of $\overline{VPA}$.

The $\overline{VPA}$ input signals the processor that the address on the bus is the address of an EF 6800 device (or an area reserved for EF 6800 devices) and that the bus should conform to the phase 2 transfer characteristics of the EF 6800 bus. Valid peripheral address is derived by decoding the address bus, conditioned by the address strobe. Chip select for the EF 6800 peripherals should be derived by decoding the address bus conditioned by $\overline{VMA}$.

After recognition of $\overline{VPA}$, the processor assures that the enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the EF 6800 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal. Figures 16 and 17 depict the best and worst case EF 6800 cycle timing. This cycle length is dependent strictly upon when $\overline{VPA}$ is asserted in relationship to the E clock.

If we assume that external circuitry asserts $\overline{VPA}$ as soon as possible after the assertion of $\overline{AS}$, then $\overline{VPA}$ will be recognized as being asserted on the falling edge of S4. In this case, no «extra» wait cycles will be inserted prior to the recognition of $\overline{VPA}$ asserted and only the wait cycles inserted to synchronize with the E clcok will determine the total length of the cycle. In any case, the synchronization delay will be some integral number of clock cycles within the following two extremes :

1 - Best Case - $\overline{VPA}$ is recognized as being asserted on the falling edge three clock cycles before E rizes (or three clock cycles after E falls).

2 - Worst Case - $\overline{VPA}$ is recognized as being asserted on the falling edge two clock cycles before E rises (or four clock cycles after E falls).

During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one-half clock cycle later in state 7 and the enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. During a write cycle, the data bus is put in the high-impedance state and the read/write signal is switched high. The peripheral logic must remove $\overline{VPA}$ within one clock after the address strobe is negated.

$\overline{DTACK}$ should not be asserted while $\overline{VPA}$ is asserted. Notice that the TS 68C000 $\overline{VMA}$ is active low, constrasted with the active high EF 6800 $\overline{VMA}$. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting the peripherals.

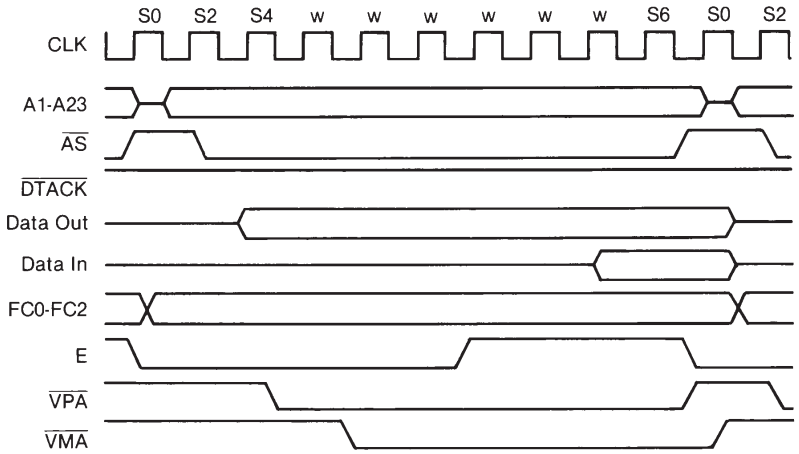


Figure 16 : TS 68C000 to EF 6800 peripheral timing - best case.

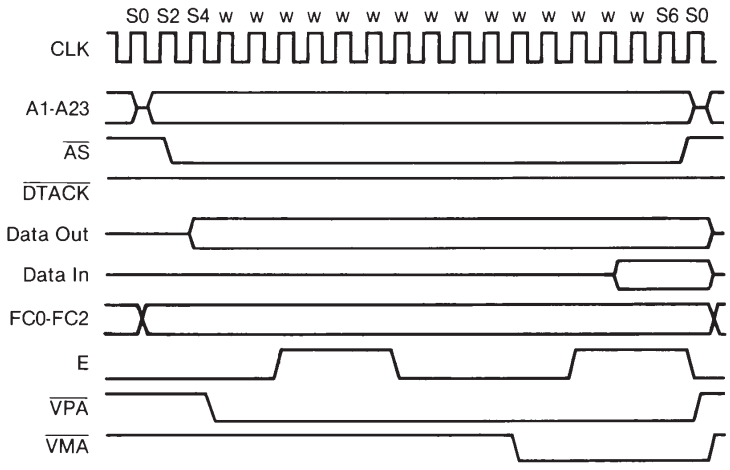


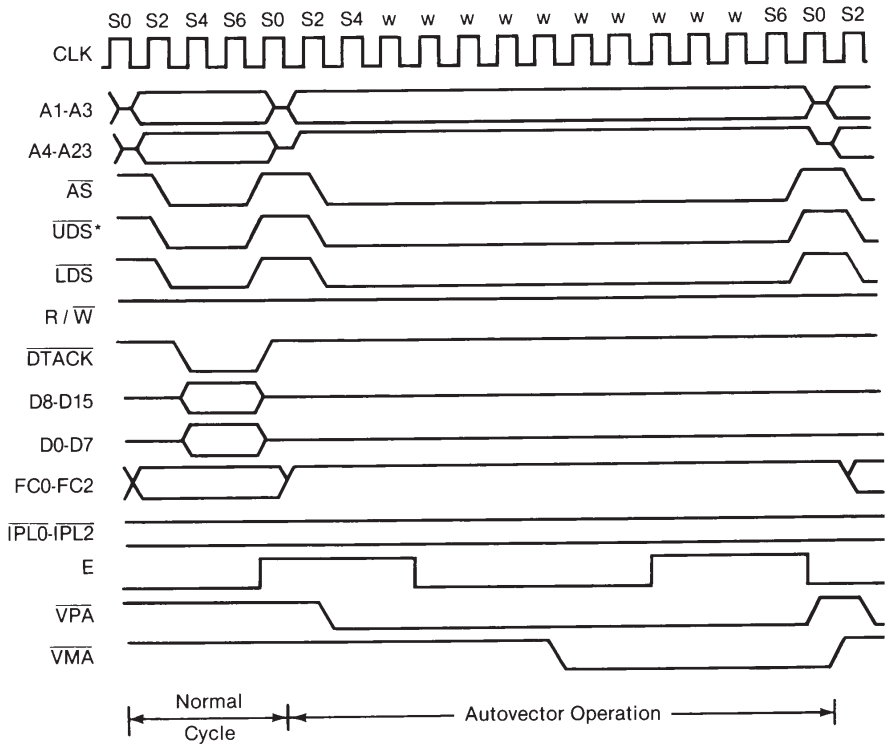
Figure 17 : TS 68C000 to EF 6800 peripheral timing - worst case.

6.6.2 · Interrupt Interface Operation

During an interrupt acknowledge cycle while the processor is fetching the vector, the $\overline{VPA}$ is asserted, the TS 68C000 will assert $\overline{VMA}$ and complete a normal EF 6800 read cycle as shown in Figure 18. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is know as autovectoring. The seven autovectors are vector number 25 through 31 (decimal).

Autovectoring operates in the same fashion (but is not restricted to) the EF 6800 interrupt sequence. The basic difference is that there are six normalinterrupt vectors and one NMI type vector. As with both the EF 6800 and the TS 68C000's normal vectored interrupt, the interrupt service routine can be located any-where in the address space. This is due to the fact that while the vector numbers are fixed the contents of the vector table entries are assigned by the user.

Since $\overline{VMA}$ is asserted during autovectoring. The EF 6800 peripheral address decoding should prevent unintended accesses.



Allthrough $\overline{UDS}$ and $\overline{LDS}$ are asserted, no data is read from the bus during the autovector cycle. The vector number is generated internally).

Figure 18 : Autovector operation timing diagram.

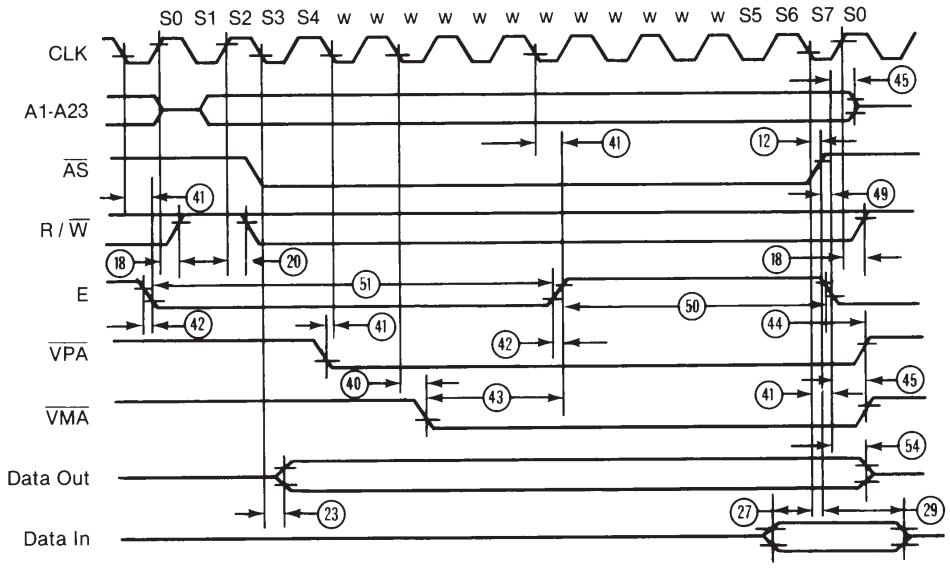
6.6.3 - Dynamic electrical characteristics TS 68C000 to EF 6800 peripheral

Num.	Symbol	Parameter	8 MHz		10 MHz		12.5 MHz		Unit
			Limits		Limits		Limits		
			Min	Max	Min	Max	Min	Max	
12	CLSH	Clock low to $\overline{AS}$, $\overline{DS}$ high (see Note 1)		70		55		50	ns
18	CHRH	Clock high to R / $\overline{W}$ high (see Note 1)	0	70	0	60	0	60	ns
20	CHRL	Clock high to R / $\overline{W}$ low (write) (see Note 1)		70		60		60	ns
23	CLDO	Clock low to data out valid (write)		70		55		55	ns
27	CLDO	Data in to clock low (setup time on read) (see Note 2)	15		10		10		ns
29	SHDII	$\overline{AS}$, $\overline{DS}$ high to Data in invalid (hold time on read)	0		0		0		ns
40	CLVML	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high		70		70		70	ns
41	CLET	Clock low to E transition		70		55		45	ns
42	Erf	E output rise and fall time		25		25		25	ns
43	VMLEH	$\overline{VMA}$ low to E high	200		150		90		ns
44	SHVPH	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high	0	120	0	90	0	70	ns
45	ELCAI	E low to control, address bus invalid (address hold time)	30		10		10		ns
47	ASI	Asynchronous input setup time (see Note 2)	20		20		20		ns
49	SHEL	$\overline{AS}$, $\overline{DS}$ high to E low (see Note 3)	– 70	70	– 55	55	– 80		ns
50	EH	E width high	450		350		280		ns
51	EL	E width low	700		550		440		ns
54	ELDOI	E low to data out invalid	30		20		15		ns

Note 1 : For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.

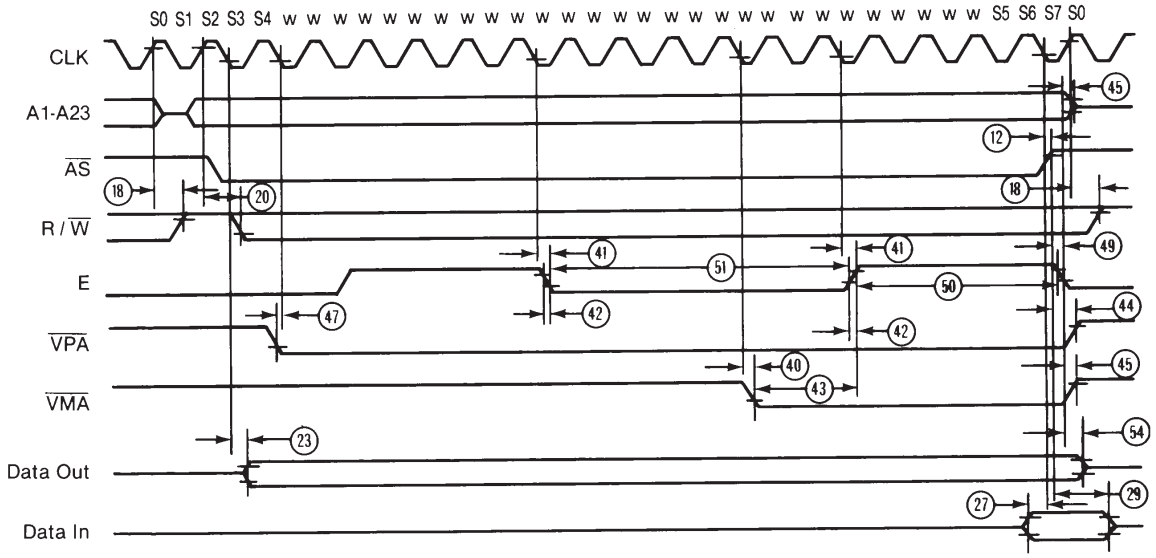
Note 2 : If the asynchronous setup time (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) required can be ignored. The data must only satisfy the date in clock-low setup time (27) for the following cycle.

Note 3 : The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and × $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.



Note : This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the worst case possibly atteinable.

Figure 19 : TS 68C000 to EF 6800 peripheral timing diagram - best case.



Note : This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the worst case possibly atteinable.

Figure 20 : TS 68C000 to EF 6800 peripheral timing diagram - worst case.

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510.

7.2 - Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with MIL-STD-883 and guarantying the parameters not tested at extreme temperatures for the entire temperature range.

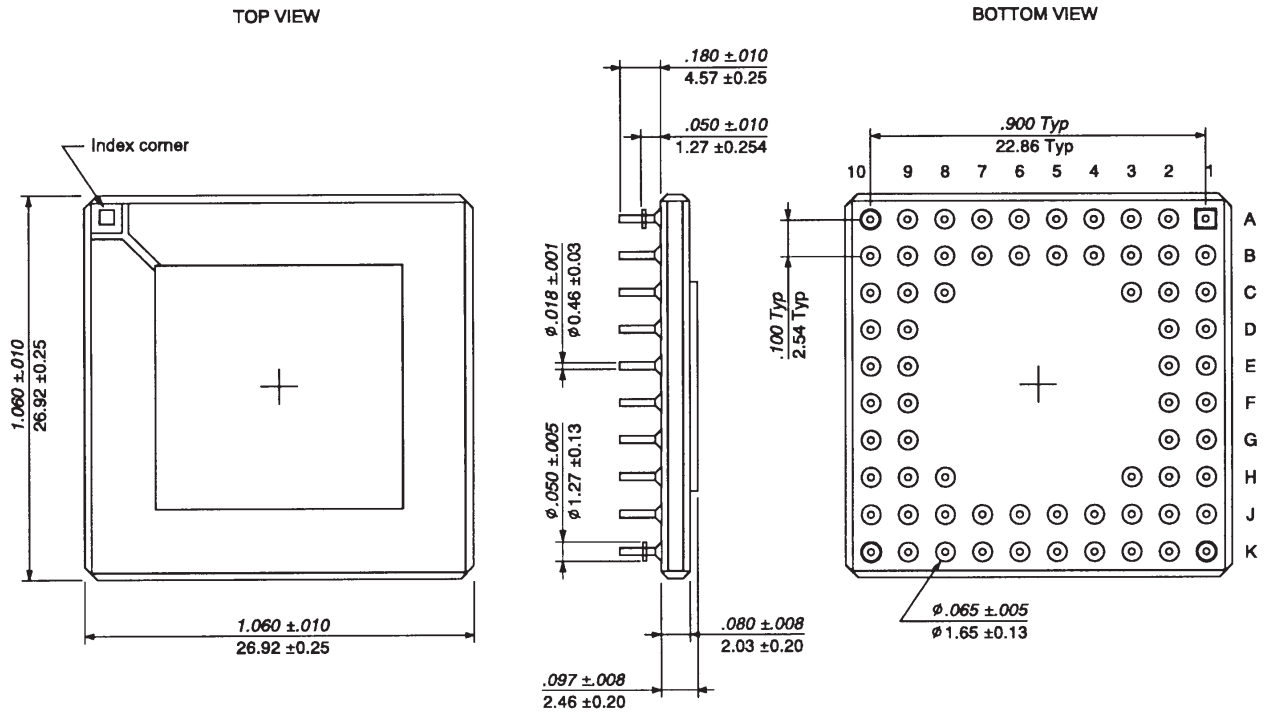
8 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

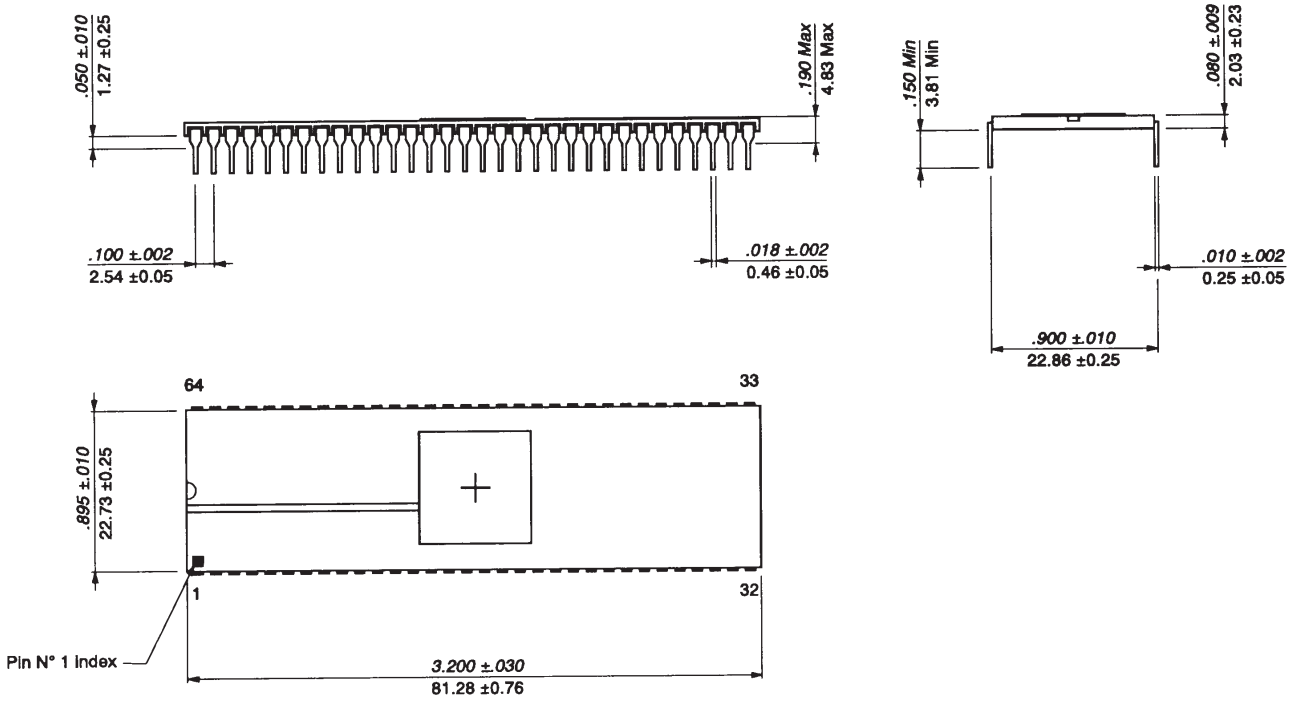
a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 %, if pratical.

9 - PACKAGE MECHANICAL DATA

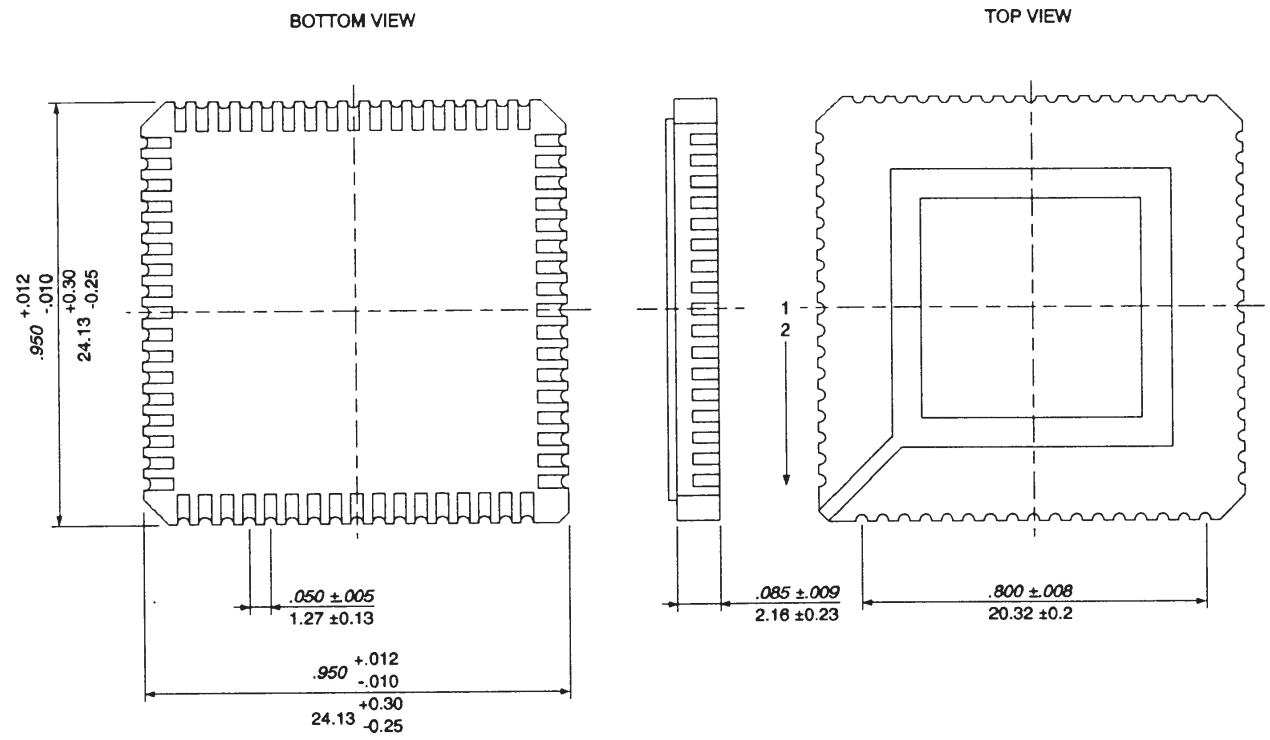
9.1 - 68 pins - Pin grid array



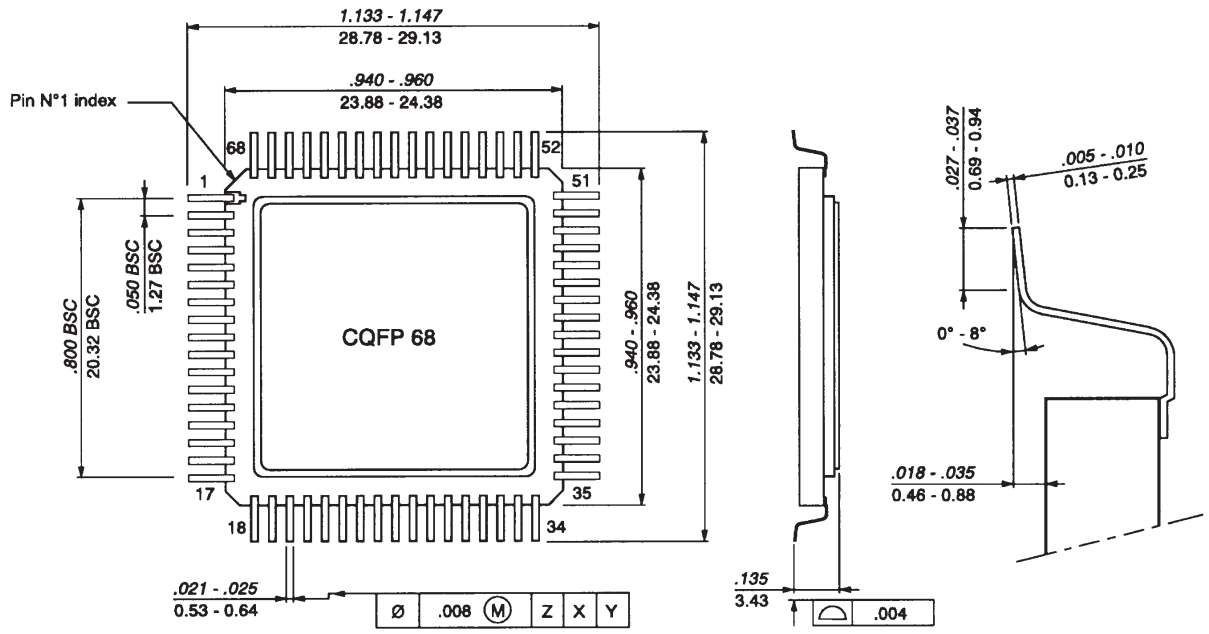
9.2 - 64 pins - Ceramic side brazed package



9.3 - 68 pins - Leadless ceramic chip carrier



9.4 - 68 pins - Ceramic quad flat pack



10 - ORDERING INFORMATION

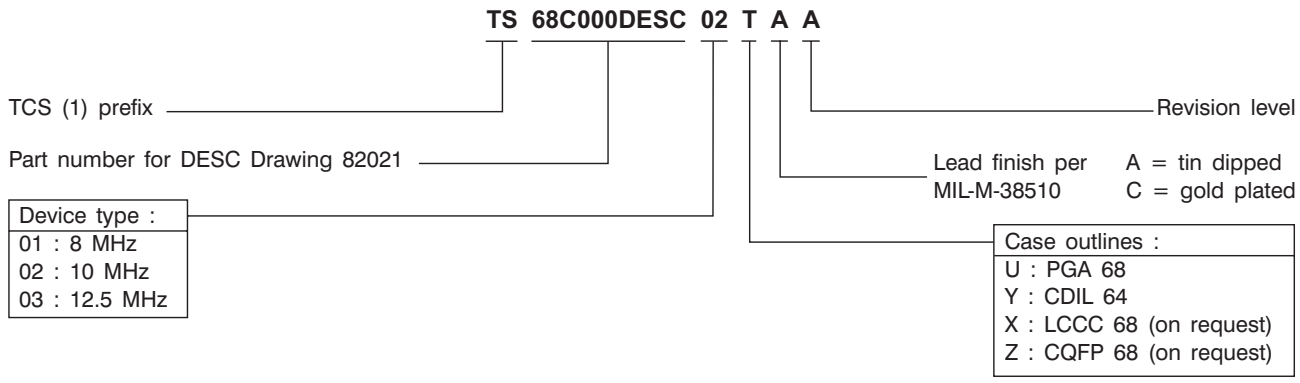
10.1 - MIL-STD-883

TS 68C000 M C1 B/C 8 A

- TCS (1) prefix
- Device
- M = -55 / +125°C
- Revision level
- Operating frequency (MHz)
- MIL-STD-883 class B

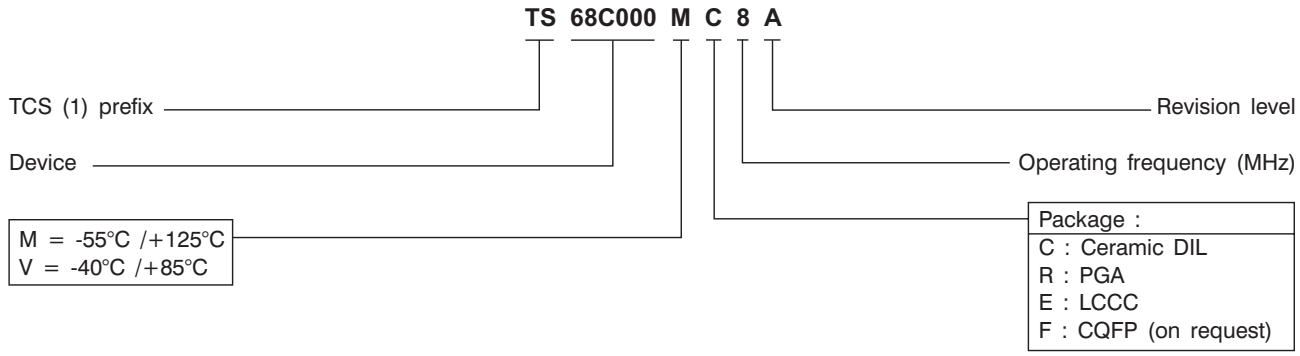
Package :
C : Ceramic DIL
R : PGA
E : LCCC
C1 : Ceramic DIL, tin dipped leads
E1 : LCCC, tin dipped leads
F : CQFP

10.2 · DESC



Note : Temperature range is $-55°C \leqslant T_C \leqslant +125°C$ for DESC product.

10.3 · Standard product



Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

This product is manufactured by THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - 38521 SAINT-EGREVE / FRANCE.

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