TS 68HC811E2

8-BIT MICROCONTROLLER

DESCRIPTION

The TS 68HC811E2 high-density CMOS (HCMOS) microcontroller unit (MCU) contains highly sophisticated on-chip peripheral capabilities. This high-speed and low-power MCU has a multiplexed bus, a nominal bus speed of two megahertz, and the fully static design allows operations at frequencies down to dc. This publication contains condensed information on the MCU.

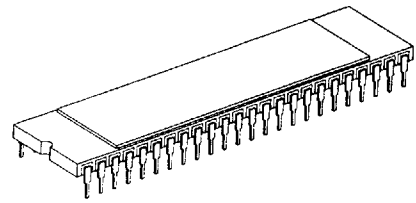
MAIN FEATURES

- 16-bit timer system with four-stage programmable prescaler :
  - 4 output compare channels,
  - 3 input compare channels,
  - 1 input capture or output capture (software selectable).
- Power saving STOP and WAIT modes.
- Synchronous Serial Peripheral Interface (SPI).
- Asynchronous NRZ serial communications interface (SCI).
- 8-bit pulse accumulator circuit.
- Bit test and branch instructions.
- Real time interrupt circuit.
- Computer Operating System (COP) watchdog system.
- TS 68HC11 CPU.
- 2K bytes of on-chip EEPROM with block protect for extra security.
- 256 bytes of on-chip static RAM, all saved during standby.
- Eight-channel 8-bit A/D converter (for CQFP only).
- 38 general purpose I/O pins :
  - 16 bidirectional input/output (I/O) pins,
  - 11 input only pins,
  - 11 output only pins.
- Power supply : 5.0 V_{DC} ± 10 %.
- Military temperature range : −55 to +125°C (T_C).

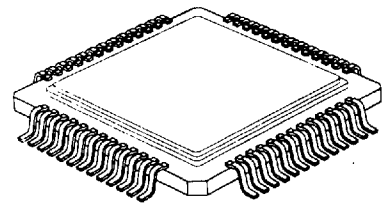
SCREENING / QUALITY

This product is manufactured in full compliance with either :

- MIL-STD-883 (class B).
- DESC 5962-89527.
- or according to TCS standards.



C Suffix
DIL 48
Ceramic side brazed dual in line



F Suffix
CQFP 52
Ceramic quad flat pack

See the ordering information page 54.

Pin connection : see pages 3 and 32.

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A - GENERAL DESCRIPTION

1 - INTRODUCTION

Figure 1 is a block diagram of the TS 68HC811E2.

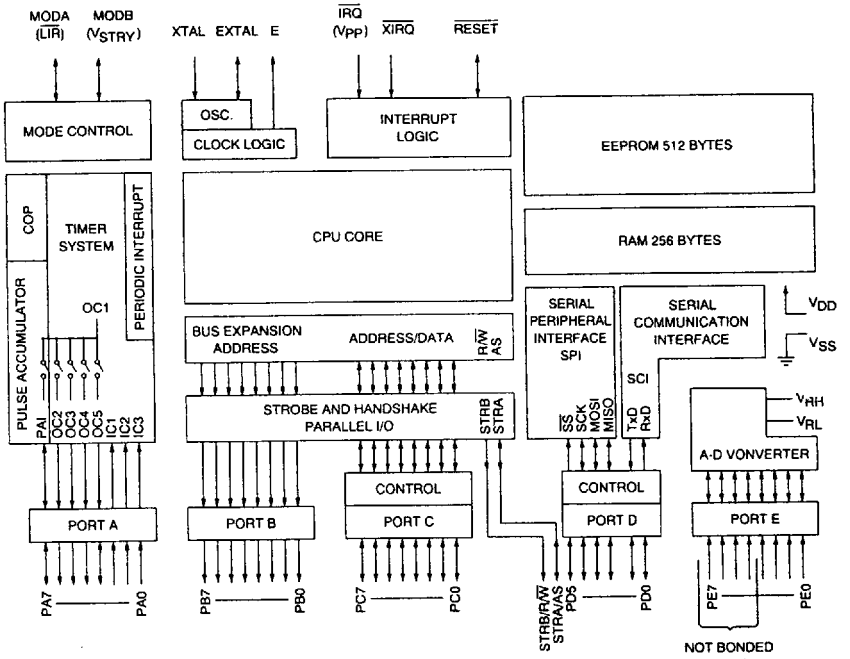


Figure 1 : TS 68HC811E2 block diagram.

2 - SIGNAL DESCRIPTION

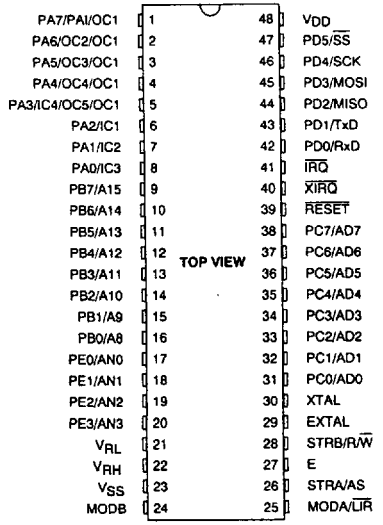


Figure 2.1 : Dil 48 terminal designation.

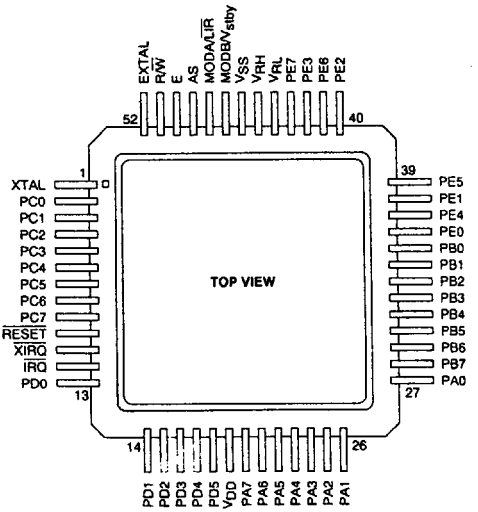


Figure 2.2 : CQFP terminal designation.

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the microcontroller TS 68HC811E2, in compliance with MIL-STD-883 class B or TCS standards.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535 : general specifications for microcircuits.
3) DESC Drawing 5962-89527.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2.1 and 2.2.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835.

3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic package which is conform to case outlines of MIL-STD-1835 (when defined) :

- DIL 48,
- 52 ceramic quad flat pack CQFP.

The precise case outlines are described in § 9.1 and 9.2.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings (see Table 1)

Table 1

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+7.0	V
P_{dmax}	Max power dissipation			150	mW
T_{case}	Operating temperature	TS 68HC811E2 CM	−55	+125	°C
		TS 68HC811E2 CV	−40	+85	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+160	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

3.3.2 · *Recommended condition of use*

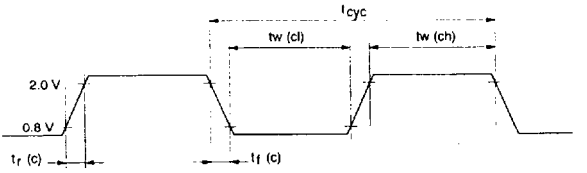
Unless otherwise stated, all voltages are referenced to the reference terminal.

Table 2

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	4.50	5.50	V
V_{IL}	Low level input voltage	V_{SS}	$0.2 \times V_{DD}$	V
V_{IH}	High level input voltage	$0.8 \times V_{DD}$	V_{DD}	V
T_{case}	Operating temperature TS 68HC811E2CM Operating temperature TS 68HC811E2CV	−55 −40	+125 +85	°C °C
V_{OH}	Maximum high level output voltage	$V_{DD} - 0.1$	V_{DD}	V
V_{OL}	Maximum low level output voltage	V_{SS}	0.4	V
f_c	Clock frequency (crystal frequency)		8.4	MHz

This device contains protective circuitry to protect the input against damage due to high static voltages or electrical fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltage to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Load network specified in § 5.4.1.



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise of fall will be linear between 0.8 volt and 2.0 volts.

Figure 3 : Clock input timing diagram.

3.4 · Thermal characteristics (at 25°C)

Table 3

Package	Symbol	Parameter	Value	Unit
DIL 48	θ JA	Thermal resistance - Ceramic junction to Ambient	38	°C/W
	θ JC	Thermal resistance - Ceramic junction to Case	5	°C/
CQFP 52	θ JA	Thermal resistance - Ceramic junction to Ambient	31	°C/W
	θ JC	Thermal resistance - Ceramic junction to Case	5	°C/W

Power considerations.

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or TCS standards.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum.

3.6.1 - Thomson logo

3.6.2 - Manufacturer's part number

3.6.3 - Class B identification

3.6.4 - Date-code of inspection lot

3.6.5 - ESD identifier if available

3.6.6 - Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-PRF-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified. For inspection purpose, refer to relevant specification :

– DESC see § 4.1.

Table 4 : Static electrical characteristics for all electrical variants. See § 5.2.

For static characteristics, test methods refer to clause 5.4 hereafter of this specification (Table 5)

For static characteristics, test methods refer to clause 5.4 hereafter of this specification (Table 4).

For dynamic characteristics (Tables 5 to 10), test methods refer to IEC 748-2 method number, where existing.

5.2 - Static characteristics

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_c = −55 / + 125° C or −40 / + 85° C.

Table 4 - DC electrical characteristics

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; A = T_L to T_H (unless otherwise noted)

Symbol	Parameter		Min	Max	Unit
V_{OH}	Output high voltage I_{Load} = −0.8 mA, V_{DD} = 4.5 V (Note 1)	All outputs except $\overline{RESET}$ XTAL, and MODA	V_{DD} - 0.8		V
V_{OL}	Output low voltage I_{Load} = 1.6 mA	All outputs except XTAL		0.4	V
V_{IH}	Input high voltage	All inputs except $\overline{RESET}$ $\overline{RESET}$	0.7 x V_{DD} 0.8 x V_{DD}	V_{DD} V_{DD}	V V
V_{IL}	Input low voltage	All inputs	V_{SS}	0.2 x V_{DD}	V
I_{OZ}	I/O ports, three-state leakage V_{in} = V_{IH} or V_{IL}	PA3/PA7, PC0-PC7, PD0-PD5, AS/STRA, MODA/$\overline{LIR}$, $\overline{RESET}$		±10	µA
I_{in}	Input current (Note 2) V_{in} = V_{DD} or V_{SS} V_{in} = V_{DD} or V_{SS}	PA0-PA2, $\overline{IRQ}$, $\overline{XIRQ}$ MODB/V_{STBY}		±1 ±10	µA µA
V_{SB}	RAM standby voltage powerdown		4.0	V_{DD}	V
I_{SB}	RAM standby current powerdown			20	µA
	Total supply current (Note 3)				
I_{DD}	RUN : Single chip Expanded multiplexed			20 30	mA mA
W_{IDD}	WAIT : All peripheral functions shut down Single-chip mode Expanded multiplexed mode			10 15	mA mA
S_{IDD}	STOP : No clocks, single-chip mode			300	µA
C_{in}	Input capacitance	PA0-PA2, PE0-PE7, $\overline{IRQ}$, $\overline{XIRQ}$, $\overline{EXTAL}$ PA3, PA7, PC0-PC7, PD0-PD5, AS/STRA, MODA/$\overline{LIR}$, $\overline{RESET}$		8 14	pF pF
P_D	Power dissipation	Single-chip mode Expanded-multiplexed mode		110 165	mW mW

Note 1 : V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wire-OR mode.

Note 2 : See A/D specification for leakage current for port E.

Note 3 : All ports configured as inputs, $V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{DD} - 0.2$ V, no dc loads, EXTAL is driven with a square wave, and t_{cyc} = 476.5 ns.

5.3 - Dynamic (switching) characteristics

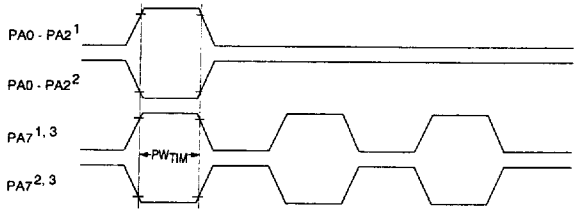
The limits and values given in this section apply over the full case temperature range −55°C to +125°C and V_{CC} in the range 4.5 V to 5.5 V V_{IL} = 0.5 V and V_{IH} = 2.4 V (See also notes 1 and 2).

Table 5 - Control timing

V_{DD} = 5.0 Vdc ± 10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$

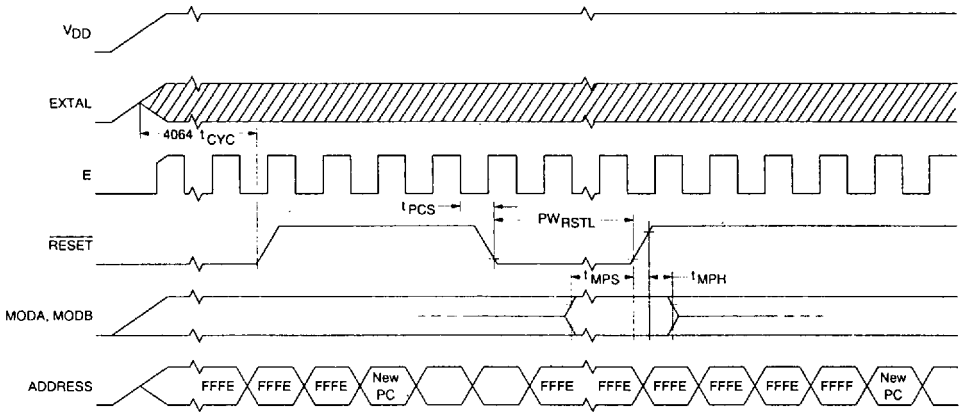
Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f_O	Frequency of operation	dc	1.0	dc	2.0	dc	2.1	MHz
t_{cyc}	E clock period	1000		500		476		ns
f_{XTAL}	Crystal frequency		4.0		8.0		8.4	MHz
4 f_O	External oscillator frequency	dc	4.0	dc	8.0	dc	8.4	MHz
t_{PCS}	Processor control setup Time (see Figures 5, 7 and 8) $t_{PCS} = 1/4\ t_{cyc} - 50$ ns	200		75		69		ns
PW_{RSTL}	Reset input pulse width (Note 1 and Figure 5) (To guarantee external reset vector) (Minimum input time ; may be preempted by internal reset)	8 1		8 1		8 1		t_{cyc}
t_{MPS}	Mode programming setup time (see Figure 5)	2		2		2		t_{cyc}
t_{MPH}	Mode programming hold time (see Figure 5)	0		0		0		ns
PW_{IRQ}	Interrupt pulse width $\overline{IRQ}$ edge sentive mode (see Figures 6 and 8) $PW_{IRQ} = t_{cyc}$ 20 ns	2		2		2		ns
t_{WRS}	Wait recovery startup time (see Figure 7)		4		4		4	t_{cyc}
PW_{TIM}	Timer pulse width Input capture, pulse accumulator input (see Figure 4) $PW_{TIM} = t_{cyc} + 20$ ns	1020		520		496		ns

Note : $\overline{RESET}$ will be recognized during the first clock it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. See RESET, INTERRUPT, AND LOW-POWER MODES for details.



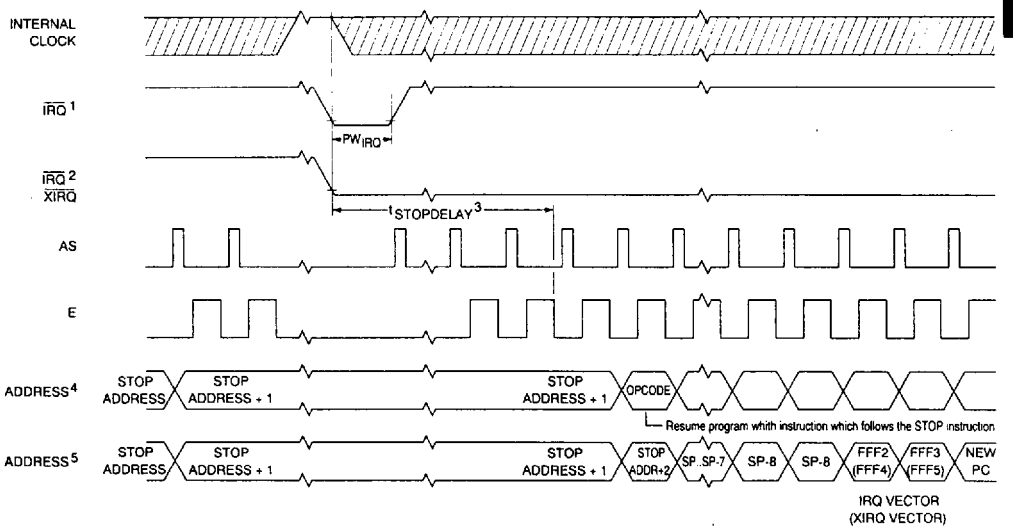
Note 1 : Rising sensitive input.
Note 2 : Falling edge sensitive input.
Note 3 : Maximum pulse accumulator clocking rate is E frequency divided by 2.

Figure 4 : Timer inputs timing diagram.



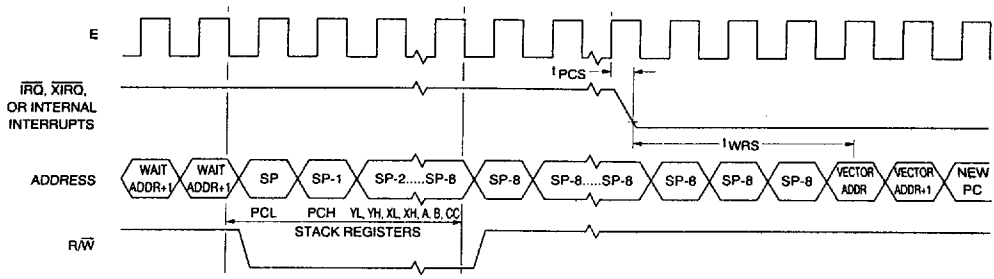
Note : Refer to table 5 for pin states during $\overline{\text{RESET}}$

Figure 5 : POR external reset timing diagram.



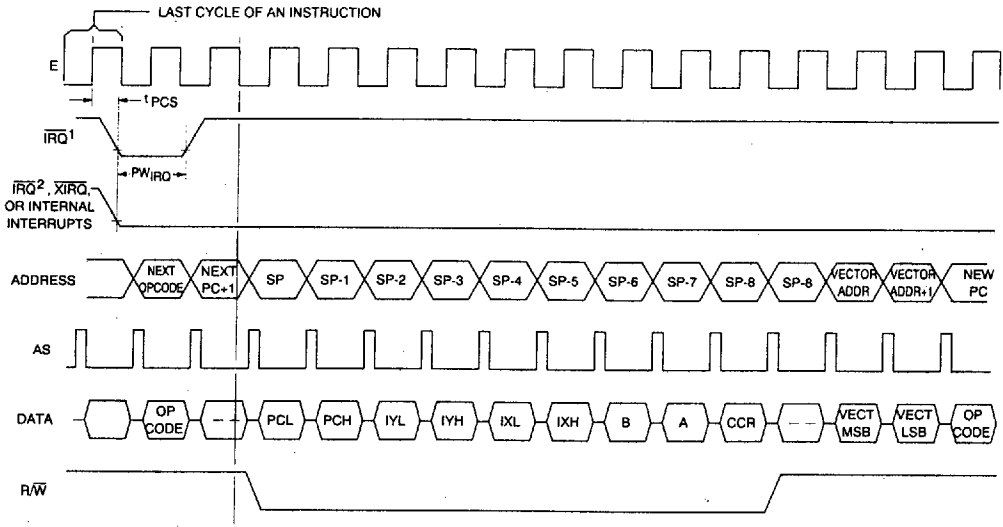
Note 1 : Edge sensitive $\overline{\text{IRQ}}$ pin (IRQE bit = 1)
Note 2 : Level sensitive $\overline{\text{IRQ}}$ pin (IRQ bit = 0).
Note 3 : $t_{STOPDELAY}$ = 4064 t_{cyc} if DLY bit = 1 or 4 t_{cyc} if DLY = 0.
Note 4 : $\overline{\text{XIRQ}}$ with X bit in CCR = 1.
Note 5 : $\overline{\text{IRQ}}$ or ($\overline{\text{XIRQ}}$ with X bit in CCR = 0).

Figure 6 : Stop recovery timing diagram.



Note 1 : Refer to table 5 for pin states during WAIT.
Note 2 : $\overline{\text{RESET}}$ will also cause recovery from WAIT.

Figure 7 : WAIT recovery from interrupt timing diagram.



Note 1 : Edge sensitive $\overline{\text{IRQ}}$ pin (IRQ bit = 1).
Note 2 : Level sensitive $\overline{\text{IRQ}}$ pin (IRQE bit = 0).

Figure 8 : Interrupt timing diagram.

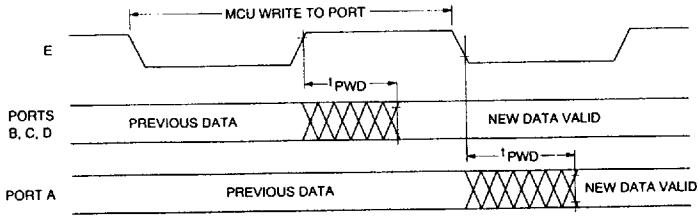
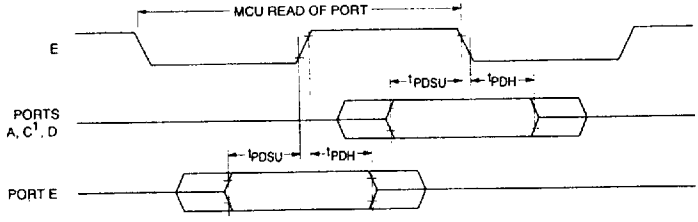


Figure 9 : Port write timing diagram.



Note : For non-latched operation of Port C.

Figure 10 : Port read timing diagram.

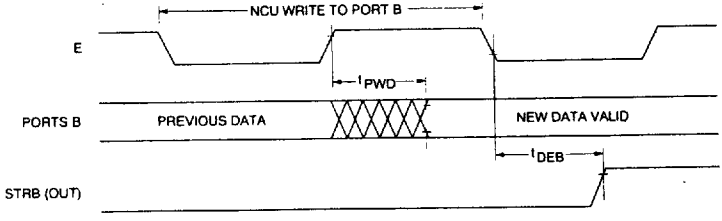


Figure 11 : Simple output strobe timing diagram.

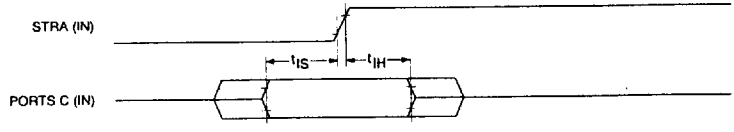
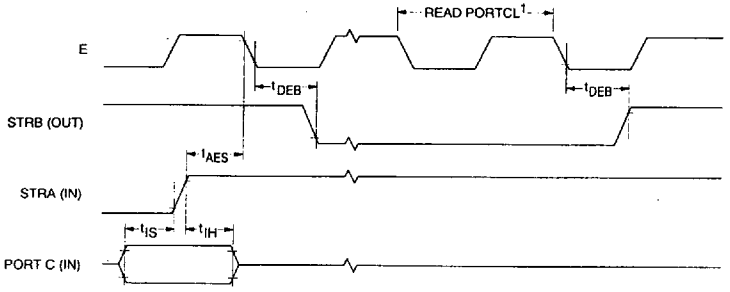
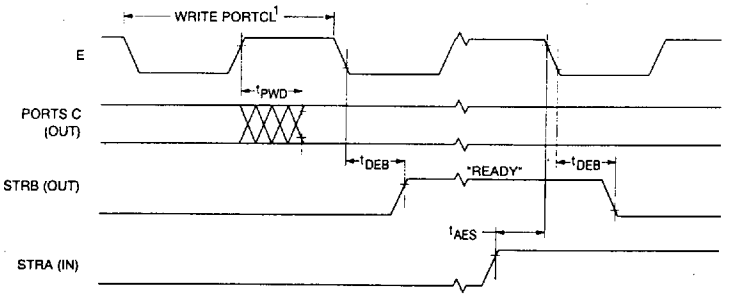


Figure 12 : Simple intput strobe timing diagram.



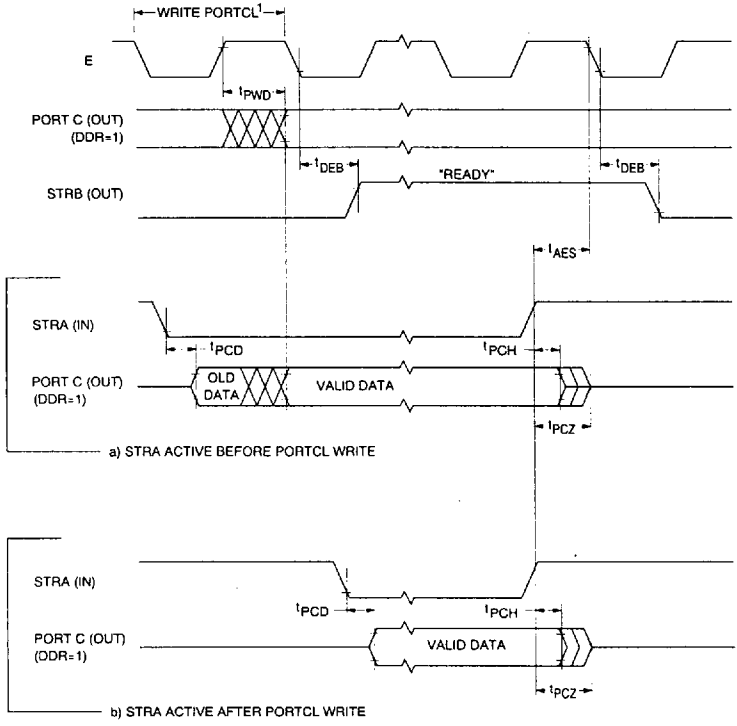
Note 1 : After reading PIOC with STAF set.
Note 2 : Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Figure 13 : Port C input handshake timing diagram.



Note 1 : After reading PIOC with STAF set.
Note 2 : Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Figure 14 : Port C output handshake timing diagram.



Note 1 : After reading PIOC with STAF set.
Note 2 : Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Figure 15 : Three-state variation of output handshake timing diagram (STRA enables output buffer).

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Table 6 - Peripheral port timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C + 85°C$ or $-55 \leqslant T_C \leqslant +125°C$

Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f_O	Frequency of operation (E clock frequency)	1.0	1.0	2.0	2.0	2.1	2.1	MHz
t_{cyc}	E clock period	1000		500		476		ns
t_{PDSU}	Peripheral data setup time (MCU read of ports A, C, D and E) (see Figure 10)	100		100		100		ns
t_{PDH}	Peripheral data hold time (MCU read of ports A, C, D and E) (see Figure 10)	50		50		50		ns
t_{PWD}	Delay time, peripheral data write (See Figures 9, 11, 13 and 14) MCU write to port A MCU writes to ports, B, C and D t_{PWD} = 1/4 t_{cyc} + 90 ns		 175 340		 175 215		 175 209	 ns ns
t_{IS}	Input data setup time (port C) (see Figures 12 and 13)	60		60		60		ns
t_{IH}	Input data hold time (port C) (see Figures 12 and 13)	100		100		100		ns
t_{DEB}	Delay time, E fall to STRB t_{DEB} = 1/4 t_{cyc} + 130 ns (see Figures 11, 13, 14 and 15)		380		255		249	ns
t_{AES}	Setup time, STRA asserted to E fall (see Note) (see Figures 13, 14 and 15)	0		0		0		ns
t_{PCD}	Delay time, STRA asserted to port C data output valid (see Figure 15)		100		100		100	ns
t_{PCH}	Hold time, STRA negated to port C data (see Figure 15)	10		10		10		ns
t_{PCZ}	Three-state hold time (see Figure 15)		150		150		150	ns

Note : If this setup time is met, STRB will acknoweldge in the next cycle. If it is not met, the respons may be delayed one more cycle.

Table 7 - A/D converter characteristics

V_{DD} = 5.0 Vdc ± 10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C + 85°C$ or $-55 \leqslant T_C \leqslant +125°C$; 750 kHz $\leqslant$ E $\leqslant$ 2.1 MHz (unless otherwise noted)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of Bits Resolved by the A/D	8		Bits
Non-linearity	Maximum deviation from the ideal A/D transfer characteristics		± 1/2	LSB
Zero error	Difference between the output of an ideal and an actual A/D for zero input voltage		± 1/2	LSB
Full-scale error	Difference between the output of an ideal and an actual A/D for full-scale input voltage		± 1/2	LSB
Total unadjusted error	Maximum sum of non-linearity, zero, error, and full-state error (Note 1)		± 1/2	LSB
Quantization error	Uncertainty due to converter resolution		± 1/2	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error source included		± 1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage (Note 2)	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage (Note 2)	V_{SS} - 0.1	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL} (Note 2)	3		V
Conversion time	Total time to perform a single analog-to-digital conversion : a. E clock b. Internal RC oscillator		32 t_{cyc} + 40	t_{cyc} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	Guaranteed		
Zero-input reading	Conversion result when $V_{in} = V_{RL}$	00		Hex
Full-scale reading	Conversion result when $V_{in} = V_{RH}$		FF	Hex
Sample acquisition time	Analog input acquisition sampling time : a. E clock b. Internal RC oscillator	12	 12	t_{cyc} µs
Input leakage	Input leakage on A/D pins PE0-PE7 V_{RL}, V_{RH}		400 1.0	nA µA

Note 1 : Source impedances greater than 10 kΩ will adversaly affect accuracy due mainly to input leakage.
Note 2 : Performance verified down to 2.5 V ΔV_R, but accuracy is tested and guaranteed at ΔV_R = 5 V ± 10 %.

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Table 8 - Expansion bus timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 16

Num.	Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	f_O	Frequency of operation (E clock frequency)	1.0	1.0	2.0	2.0	2.1	2.1	MHz
1	t_{cyc}	Cycle time	1000		500		476		ns
2	PW_{EL}	Pulse width, E low $PW_{EL} = 1/2\ t_{cyc} - 23$ ns	477		227		215		ns
3	PW_{EH}	Pulse width, E high $PW_{EH} = 1/2\ t_{cyc} - 28$ ns	472		222		210		ns
4	t_r, t_f	E and AS rise and fall time		20		20		20	ns
9	t_{AH}	Address hold time $t_{AH} = 1/8\ t_{yc} - 29.5$ ns (Note 1a)	95.5		33		30		ns
12	t_{AV}	Non-muxed address valid time to E rise $t_{AV} = PW_{EL} - (t_{ASD} + 80$ ns) (Note 1b)	281.5		94		85		ns
17	t_{DSR}	Read data setup time	30		30		30		ns
18	t_{DHR}	Read data hold time (maxe = t_{MAD})	10	145.5	10	83	10	80	ns
19	t_{DDW}	Write data delay time $t_{DDW} = 1/8\ t_{cyc} + 65.5$ ns (Note 1a)		190.5		128		125	ns
21	t_{DHW}	Write data hold time $t_{DHW} = 1/8\ t_{cyc} - 29.5$ ns (Note 1a)	95.5		33		30		ns
22	t_{AVM}	Muxed address valid time to E rise $t_{AVM} = PW_{EL} - (t_{ASD} + 90$ ns) (Note 1b)	271.5		84		75		ns
24	t_{ASL}	Muxed address valid time to AS fall $t_{ASL} = PW_{ASH} - 90$ ns	151		26		20		ns
25	t_{AHL}	Muxed address hold time $t_{AHL} = 1/8\ t_{cyc} - 29.5$ ns (Note 1b)	95.5		33		30		ns
26	t_{ASD}	Delay time, E to AS rise $t_{ASD} = 1/8\ t_{cyc} - 9.5$ ns (Note 1a)	115.5		53		50		ns
27	PW_{ASH}	Pulse width, AS high $PW_{ASH} = 1/4\ t_{cyc} - 29$ ns	221		96		90		ns
28	t_{ASED}	Delay time, AS to E rise $t_{ASED} = 1/8\ t_{cyc} - 9.5$ ns (Note 1b)	115.5		53		50		ns
29	t_{ACCA}	MPU address access time $t_{ACCA} = t_{AVM} + t_r + PW_{EH} - t_{DSR}$ (Note 1b)	733.5		296		275		ns
35	t_{ACCE}	MPU access time $t_{ACCE} = PW_{EH} - t_{DSR}$		442		192		180	ns

Table 8 - Expansion bus timing (Continued)

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 16

Num.	Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
			Min	Max	Min	Max	Min	Max	
36	t_{MAD}	Muxed address delay (previous cycle MPU read) $t_{MAD} = t_{ASD} + 30$ ns (Note 1a)	145.5		83		80		ns

Note 1 : Input clocks with duty cycles other than 50 % will affect bus performance. Timing parameters affected by input clock duty cycle are identified by a and b. To recalculate the approximate bus timing values, substitute the following expression in place of 1/8 t_{cyc} in the above formulas where applicable :
a. (1 − DC) × 1/4 t_{cyc} for : (t_{DDW}, t_{DHW}, t_{MAD})
b. DC × 1/4 t_{cyc} for : (t_{AVM}, t_{AHL}, t_{ASED}, t_{ACCA})
where : DC is the decimal value of duty cycle percentage (high time).

Table 9 - Serial peripheral interface (SPI) timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 17

Num.	Symbol	Characteristic	Min	Max	Unit
	$f_{op(m)}$ $f_{op(s)}$	Operating frequency Master Slave	dc dc	0.5 2.1	f_{op} MHz
1	$t_{cyc(m)}$ $t_{cyc(s)}$	Cycle time Master Slave	2.0 480		t_{cyc} ns
2	$t_{lead(m)}$ $t_{lead(s)}$	Enable lead time Master Slave	Note 1 240		ns ns
3	$t_{lag(m)}$ $t_{lag(s)}$	Enable lag time Master Slave	Note 1 240		ns ns
4	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	Clock (SCK) high time Master Slave	340 190		ns ns
5	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	Clock (SCK) low time Master Slave	340 190		ns ns
6	$t_{su(m)}$ $t_{su(s)}$	Data setup time (inputs) Master Slave	100 100		ns ns
7	$t_{h(m)}$ $t_{h(s)}$	Data hold time (inputs) Master Slave	100 100		ns ns
8	t_a	Access time (time to data active from high-impedance state) Slave	0	120	ns
9	t_{dis}	Disable time (hold time to high-impedance state) Slave		240	ns
10	tv(s)	Data valid (after enable edge) Note 2		240	ns
11	tho	Data hold time (outputs) (after enable edge)	0		ns
12	t_{rm} trs	Rise time (20 % V_{DD} to 70 % V_{DD}, C_L = 200 pF) SPI outputs (SCK, MOSI, and MISO) SPI inputs (SCK, MISO, MOSI, and SS)		100 2.0	ns µs

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Table 9 - Serial peripheral interface (SPI) timing (Continued)

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 17

Num.	Symbol	Characteristic	Min	Max	Unit
13	t_{fm}	Fall time (70 % V_{DD} to 20 % V_{DD}, C_L = 200 pF) SPI outputs (SCK, MOSI, and MISO)		100	ns
	tfs	SPI inputs (SCK, MISO, MOSI, and SS)		2.0	µs

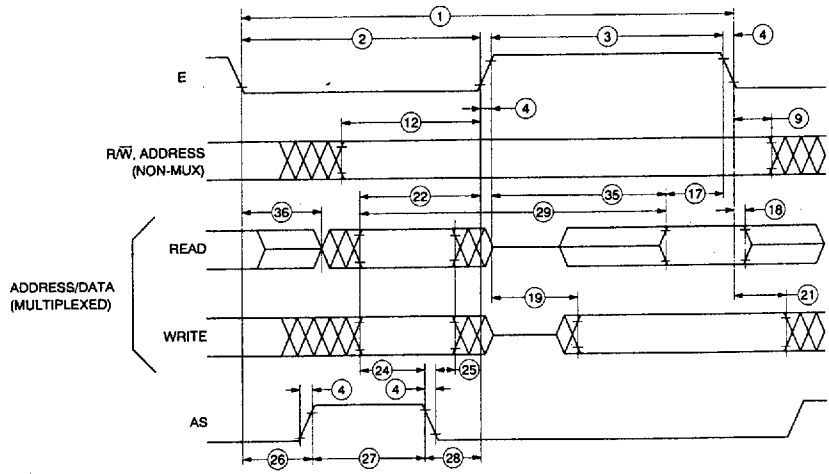
Note 1: Signal production depends on software.
Note 2: Assumes 200 pF load on all SPI pins.

Table 10 - EEPROM characteristics

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; T_C = 25°C

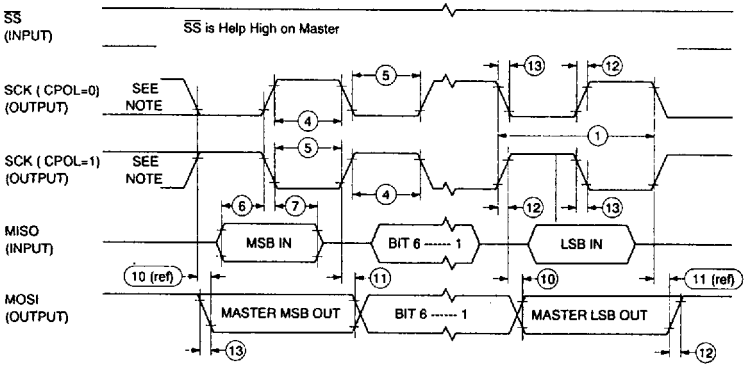
Characteristics		Min	Max	Unit
Programming time (Note 1)	Under 1.0 MHz with RC oscillator enabled 1.0 to 2.0 MHz with RC oscillator disabled 2.0 MHz (or anytime RC oscillator enabled)		25 must use RC 25	ms ms ms
Erase time (Note 1)	Byte, row, and bulk		10	ms
Write/erase endurance (Note 2)			5.000	cycles
Data retention (Note 2)			10	years

Note 1: The RC oscillator must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0 MHz.
Note 2: See current quarterly reliability monitor report for current failure rate information.



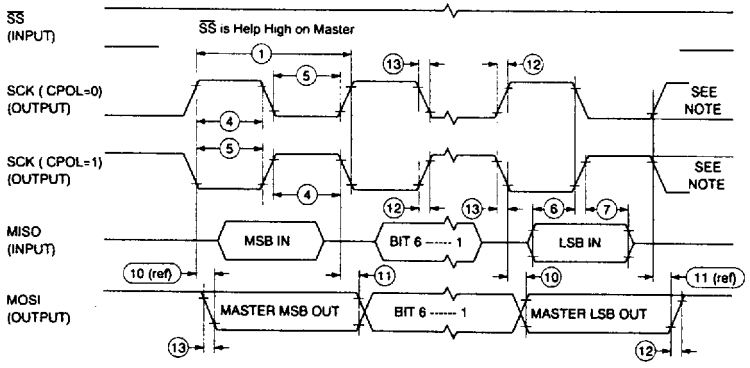
Note: Measurement points shown are 20 % and 70 % V_{DD}.

Figure 16: Expansion bus timing diagram.



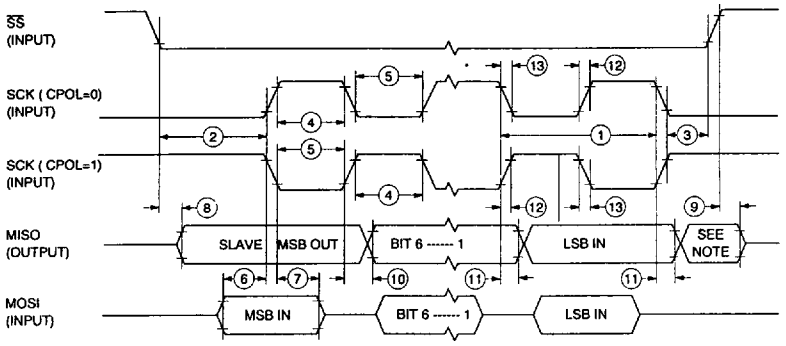
Note : This last clock edge is generated internnally but is not seen at the SCK pin.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17a : SPI timing diagrams
SPI master timing (CPHA = 0).



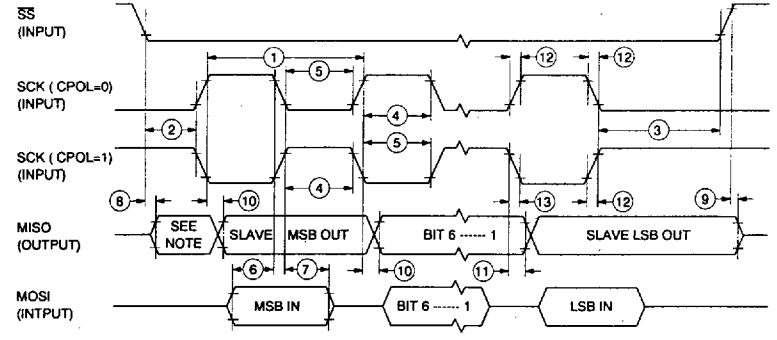
Note : This last clock edge is generated internnally but is not seen at the SCK pin.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17b : SPI timing diagrams
SPI master timing (CPHA = 1).



Note : Not defined but normally LSB of character previously transmitted.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17c : SPI timing diagrams
SPI slave timing (CPHA = 0).



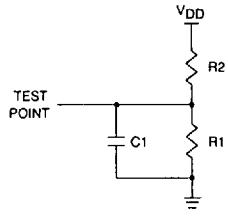
Note : Not defined but normally LSB of character previously transmitted.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17d : SPI timing diagrams
SPI slave timing (CPHA = 1).

5.4 - Test conditions specific to the device

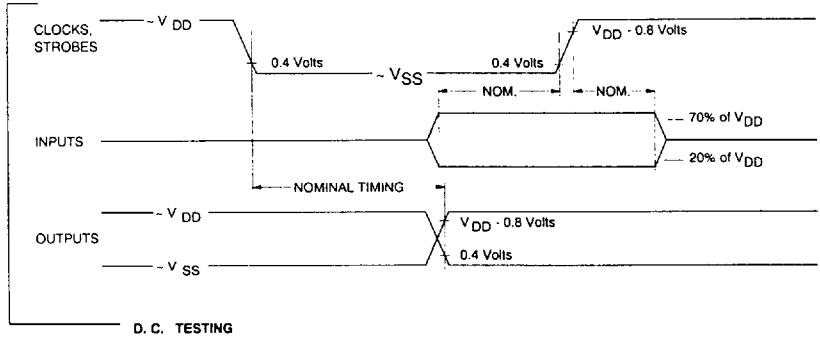
5.4.1 - Loading network

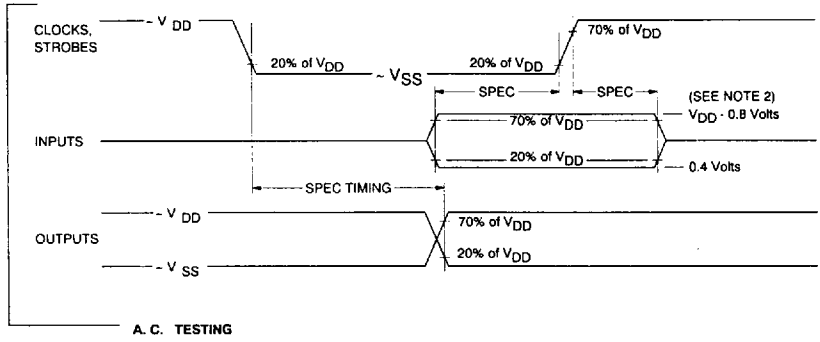
The applicable loading network of Tables 5, 6, 8, 9, refer to the loading network number as shown in Figure 18 below.



Equivalent test load (Note 1)

Pins	R1	R2	C1
PA3-PA7 PB0-PB7 PC0-PC7 PD0-PD5 E, AS, R/$\overline{W}$	3.26 K	2.38 K	30 pF
PD1-PD4	3.26 K	2.38 K	200 pF





Note 1: Full test loads are applied during all ac electrical test and ac timing measurements.

Note 2: During ac timing measurements, inputs are driven to 0.4 volts and V_{DD} - 0.8 volts while timing measurements are taken at the 20 % and 70 % of V_{DD} points.

Figure 18: Test methods.

5.4.2 - Time definitions

The times specified in Tables 5, 6, 8, 9 as dynamic characteristics are defined in Figure 18 above.

6 - FUNCTIONAL DESCRIPTION

6.1 - Operating modes

The MCU uses two dedicated pins (MODA and MODB) to select one of two basic operating modes or one of two special operating modes. The basic operating modes are single-chip and expanded-multiplexed ; the special operating modes are bootstrap and special test. The following paragraphs describe the different modes.

SINGLE-CHIP MODE (MODE0)

In this mode, the MCU functions as a self-contained microcontroller and has no external address or data bus. This mode provides maximum use of the pins for on-chip peripheral functions, and all address and data activity occur within the MCU.

EXPANDED MULTIPLEXED MODE (MODE 1)

In this mode, the MCU can address up to 64 K bytes of address space. Higher-order address bits are output on the port B pins, and lower-order address bits and the data bus are multipliexed on the port C pins. The AS pin provides the control output used in demultiplexing the loworder address at port C. The R/$\overline{W}$ pin is used to control the direction of data transfer on port C bus.

BOOTSTRAP MODE

In this mode, all vectors are fetched from the 192-byte on-chip bootloader ROM. This mode is very versatile and can be used for such functions as test and diagnostics on completed modules and for programming the EEPROM. The serial receive logic is initialized by software in the bootloader ROM, which provides program control for the serial communications interface (SCI) baud and word format. In this mode, a special control bit is configured that allows for self-testing of the MCU. This mode can be changed to other modes under program control.

TEST MODE

This modes is primarily intended for main production at time of manufacture ; however, it may be used to program calibration or personality data into the internal EEPROM. In this mode, a special control bit is configured to permit access to a number of special test control bits. This mode can be changed to other modes under program control.

6.2 - Signal description

V_{DD} AND V_{SS}

Power is supplied to the microcontroller using these two pins. V_{DD} is +5 volts (± 0.5 V) power, and V_{SS} is ground.

$\overline{RESET}$

This active low bidirectional control pin is used as an input to initialize the MCU to a known startup state and as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or the computer operating properly (COP) circuit.

XTAL, EXTAL

These pins provide the interface for either a crystal or a CMOS-compatible clock to control the internal clock generator circuitry. The frequency applied shall be four times higher than the desired clock rate. Refer to Figure 19 for crystal and clock connections.

E

This pin provides an output for the internally generated E clock, which can be used for timing reference. The frequency of the E output is one-fourth that of the input frequency at the XTAL and EXTAL pins.

$\overline{IRQ}$

This pin provides the capability for asynchronously applying interrupts to the MCU. Either negative edge-sensitive or level-sensitive triggering is program selectable. This pin is configured to level-sensitive during reset. An external resistor connected to V_{DD} is required on $\overline{IRQ}$.

$\overline{XIRQ}$

This pin provides the capability for asynchronously applying non-maskable interrupts to the MCU after a power on reset (POR). During reset, the X bit in the condition code register is set, and anay interrupt is masked until enabled by software. This input is level-sensitive and requires an external pullup resistor to V_{DD}.

MODA/$\overline{LIR}$ AND MODB/V_{stby}

During reset, these pins are used to control the two basic operating modes and the two special operating modes. The $\overline{LIR}$ output can be used as an aid in debugging once reset is completed. The open-drain $\overline{LIR}$ pin goes to an active low during the first E-clock cycle of each instruction and remains low for the duration of that cycle. The mode selections are shown below.

MODB	MODA	Mode selected
1	0	Single chip
1	1	Expanded multiplexed
0	0	Special bootstrap
0	1	Special test

V_{RL} AND V_{RH}

These pins provide the reference voltage for the A/D converter.

R/$\overline{W}$/STRB

This pin provides two different functions, depending on the operating mode. In single-chip mode, the pin provides STRB (output strobe) function ; in the expanded multiplexed mode, it provides R/$\overline{W}$ (read-write) function. The R/$\overline{W}$ is used to control the direction of transfers on the external data bus.

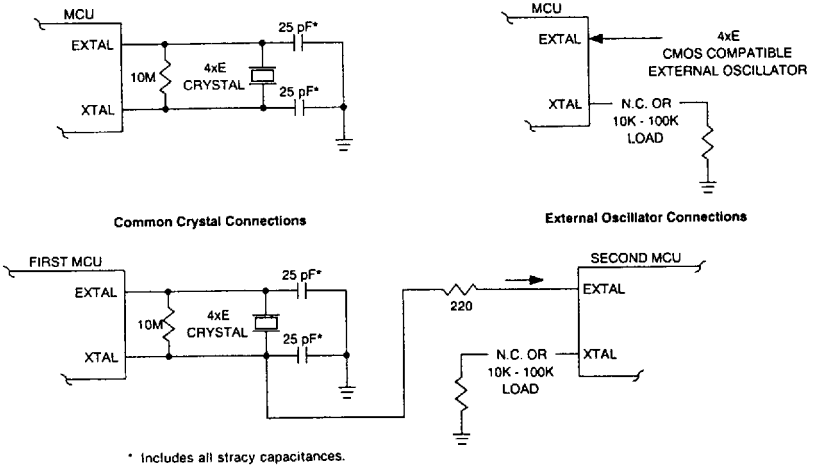


Figure 19 : Oscillator connections.

AS/STRA

This pin provides two different functions depending on the operating mode. In single-chip mode, the pin provides STRA (input strobe) function, and in the expanded-multiplexed mode, it provides AS (address strobe) function. The AS may be used to demultiplex the address and data signals at port C.

INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PE0-PE7)

These I/O lines are arranged into four 8-bit ports (A, B, C, and E) and one 6-bit port (D). All ports serve more than one purpose depending on the operating mode. Table 11 lists a summary of the pin functions to operating modes. Refer to INPUT/OUTPUT PORTS for additionnal information.

6.3 - Input/output ports

Port functions are controlled by the particular mode selected. In the single-chip mode and bootstrap mode, four ports are configured as parallel I/O data ports and port E can be used for general-purpose static inputs and/or analog-to-digital converter channel inputs. In the expanded-multiplexed mode and test mode, ports B, C, AS, and R/$\overline{W}$ are configured as a memory expansion bus. Table 11 lists the different port signals available. The following paragraphs describe each port.

PORT A

In all operating modes, port A may be configured for three input capture funcitons ; four output compare functions ; and pulse accumulator input (PAI) or a fifth output compare function. Each input capture pin provides for a transitional input, which is used to latch a timer value into the 16-bit input capture register. External devices provide the transitional input, and internal decoders determine which input transition edge is sensed. The output compare pins provide an output whenever a match is made between the value in the free-running counter (in the timer system) and a value loaded into the particular 16-bit output compare register. When port A bit 7 is configured as a PAI, the external input pulses are applied to the pulse accumulator system. The remaining port A lines may be used as general-purpose input or output lines.

PORT B

In the single-chip mode, all port B pins are general purpose output pins. Port B may also be used in a simple strobed output mode where the STRB pulses each time port B is written. In the expanded-multiplexed mode, all of the port B pins act as high-order (bits 8-15) address output pins.

Table 11 - Port signal functions

Port-bit	Single-chip and bootstrap mode	Expanded multiplexed and special test mode
A-0	PA0/IC3	PA0/IC3
A-1	PA1/IC2	PA0/IC2
A-2	PA2/IC1	PA0/IC1
A-3	PA3/OC5/ and-or OC1	PA3/OC5/ and-or OC1
A-4	PA4/OC4/ and-or OC1	PA4/OC4/ and-or OC1
A-5	PA5/OC3/ and-or OC1	PA5/OC3/ and-or OC1
A-6	PA6/OC2/ and-or OC1	PA6/OC2/ and-or OC1
A-7	PA7/PAI/ and-or OC1	PA7/PAI/ and-or OC1
B-0	PB0	A8
B-1	PB1	A9
B-2	PB2	A10
B-3	PB3	A11
B-4	PB4	A12
B-5	PB5	A13
B-6	PB6	A14
B-7	PB7	A15
C-0	PC0	A0/D0
C-1	PC1	A1/D1
C-2	PC2	A2/D2
C-3	PC3	A3/D3
C-4	PC4	A4/D4
C-5	PC5	A5/D5
C-6	PC6	A6/D6
C-7	PC7	A7/D7
D-0	PD0/R x D	PDO/R x D
D-1	PD1/T x D	PD1/T x D
D-2	PD2/MISO	PD2/MISO
D-3	PD3/MOSI	PD3/MOSI
D-4	PD4/$\overline{SCK}$	PD4/$\overline{SCK}$
D-5	PD5/$\overline{SS}$	PD5/$\overline{SS}$
	STRA	AS
	STRB	R/W
E-0	PE0/AN0	PE0/AN0
E-1	PE1/AN1	PE1/AN1
E-2	PE2/AN2	PE2/AN2
E-3	PE3/AN3	PE3/AN3
E-4	PE4/AN4 (see Note)	PE4/AN4 (see Note)
E-5	PE5/AN5 (see Note)	PE5/AN5 (see Note)
E-6	PE6/AN6 (see Note)	PE6/AN6 (see Note)
E-7	PE7/AN7 (see Note)	PE7/AN7 (see Note)

Note : Not bonded in 48-pin versions.

PORT C

In the single-chip mode, port C pins are general-purpose input/output pins. Port C inputs can be latched by the STRA or may be used in full handshake modes of parallel I/O where the STRA input and STRB output acts as handshake control lines. In the expanded-multiplexed mode, port C pins are configured as multiplexed address/data pins. During the address cycle, bits 0 through 7 of the address are output on PC0-PC7 ; during the data cycle, bits 0 through 7 (PC0-PC7) are bidirectionnal data pins controlled by the R/W signal.

PORT D

In all modes, port D bits 0-5 may be used for general-purpose I/O or with the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems. Bit 0 is the receive data input, and bit 1 is the transmit data output for the SCI. Bits 2 through 5 are used by the SPI subsystem.

PORT E

Port E is used for general-purpose static inputs and/or analog-to-digital channel inputs in all operating modes. Port E should not be read as static inputs while an A/D conversion is actually taking place.

6.4 · Memory

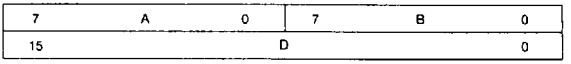
The memory maps for each mode of operation, a single-chip, expanded-multiplexed, special boot, and special test is shown in Figure 20. In the single-chip mode, the MCU does not generate external addresses. The internal memory locations are shown in the shaded areas, and the contents of the shaded areas are shown on the right side of the diagram. In the expanded-multiplexed mode, the memory locations are basically the same as the single-chip, except the memory locations between s shown in Figure 20. In the single-chip mode, the MCU does not (EXT) are for externally addressed memory and I/O. The special bootstrap mode is similar to the single-chip mode, except the bootstrap program ROM is located at memory locations $BF40 through $BFFF. The special test mode is similar to the expanded-multiplexed mode, except the interrupt vectors are at external memory locations.

6.5 · Registers

The MCU contains the registers described in the following paragraphs.

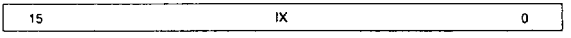
ACCUMULATOR A AND B

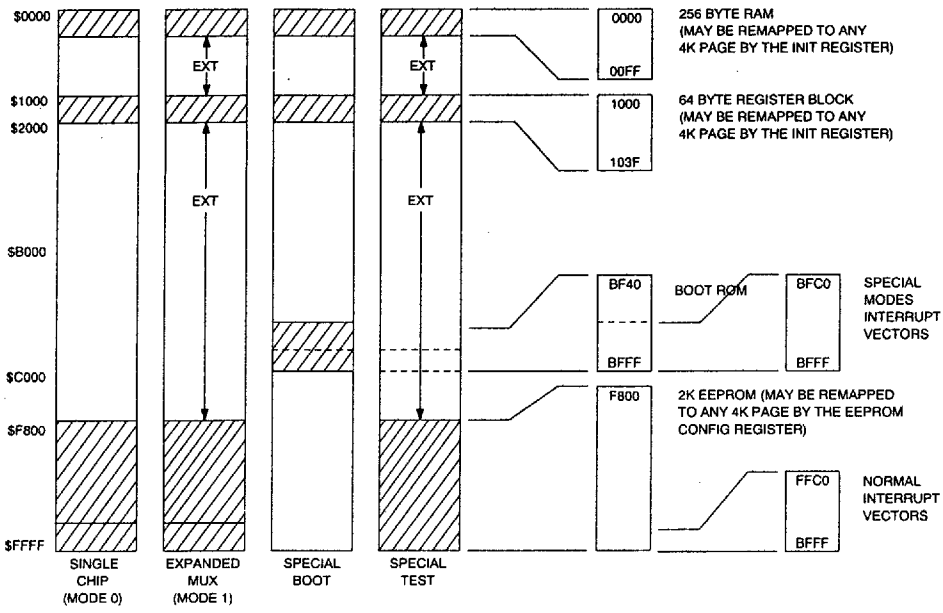
These accumulators are general-purpose 8-bit registers used to hold operands and results of arithmetic calculations or data manipulations. These two accumulators are treated as a single, double-byte accumulator called the D accumulator fo some instructions.



INDEX REGISTER X (IX)

This index register is a 16-bit register used for the indexed addressing mode. It provides a 16-bit value that may be added to an 8-bit offset provided in an instruction to create an effective address. The index register may also be used either as a counter or a temporary storage area.





NOTE :

Note : Either or both the internal RAM and registers can be remapped to any 4K boundary by software.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1000	Bit 7	—	—	—	—	—	—	Bit 0	PORTA	I/O Port A
$1001									Reserved	
$1002	STAF.	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC	Parallel I/O Control Register
$1003	Bit 7	—	—	—	—	—	—	Bit 0	PORTC	I/O Port C
$1004	Bit 7	—	—	—	—	—	—	Bit 0	PORTB	Output Port B
$1005	Bit 7	—	—	—	—	—	—	Bit 0	PORTCL	Alternate Latched Port C
$1006									Reserved	
$1007	Bit 7	—	—	—	—	—	—	Bit 0	DDRC	Data Direction for Port C
$1008			Bit 5	—	—	—	—	Bit 0	PORTD	I/O Port D
$1009			Bit 5	—	—	—	—	Bit 0	DDRD	Data Direction for Port D
$100A	Bit 7	—	—	—	—	—	—	Bit 0	PORTE	Input Port E
$100B	FOC1	FOC2	FOC3	FOC4	FOC5				CFORC	Compare Force Register
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3				OC1M	OC1 Action Mask Register

Figure 20 : Memory map.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3				OC1D	OC1 Action Data Register
$100E	Bit 15	—	—	—	—	—	—	Bit 8	TCNT	Timer Counter Register
$100F	Bit 7	—	—	—	—	—	—	Bit 0		
$1010	Bit 15	—	—	—	—	—	—	Bit 8	TIC1	Input Capture 1 Register
$1011	Bit 7	—	—	—	—	—	—	Bit 0		
$1012	Bit 15	—	—	—	—	—	—	Bit 8	TIC2	Input Capture 2 Register
$1013	Bit 7	—	—	—	—	—	—	Bit 0		
$1014	Bit 15	—	—	—	—	—	—	Bit 8	TIC3	Input Capture 3 Register
$1015	Bit 7	—	—	—	—	—	—	Bit 0		
$1016	Bit 15	—	—	—	—	—	—	Bit 8	TOC1	Output Capture 1 Register
$1017	Bit 7	—	—	—	—	—	—	Bit 0		
$1018	Bit 15	—	—	—	—	—	—	Bit 8	TOC2	Output Capture 2 Register
$1019	Bit 7	—	—	—	—	—	—	Bit 0		
$101A	Bit 15	—	—	—	—	—	—	Bit 8	TOC3	Output Capture 3 Register
$101B	Bit 7	—	—	—	—	—	—	Bit 0		
$101C	Bit 15	—	—	—	—	—	—	Bit 8	TOC4	Output Capture 4 Register
$101D	Bit 7	—	—	—	—	—	—	Bit 0		
$101E	Bit 15	—	—	—	—	—	—	Bit 8	TOC5	Output Capture 5 Register/
$101F	Bit 7	—	—	—	—	—	—	Bit 0		Input Capture 4 Register
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1	Timer Control Register 1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2	Timer Control Register 2
$1022	OC1I	OC2I	OC3I	OC4I	I405I	IC1I	IC2I	IC3I	TMSK1	Timer Interrupt Mask Reg. 1
$1023	OC1F	OC2F	OC3F	OC4F	I405F	IC1F	IC2F	IC3F	TFLG1	Timer Interrupt Flag Reg. 1
$1024	TOI	RTII	PAOVI	PAII			PR1	PR0	TMSK2	Timer Interrupt Mask Reg. 2
$1025	TOF	RTIF	PAOVF	PAIF					TFLG2	Timer Interrupt Flag Reg. 1
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL	Pulse Accum. Control Reg
$1027	Bit 7	—	—	—	—	—	—	Bit 0	PACNT	Pulse Accum. Count Reg.
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR	SPI Control Register
$1029	SPIF	WCOL		MODF					SPSR	SPI Status Register
$102A	Bit 7	—	—	—	—	—	—	Bit 0	SPDR	SPI Data Register
$102B	TCLR		SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD	SCI Baud Rate Control
$102C	R8	T8		M	WAKE				SCCR1	SCI Control Register 1

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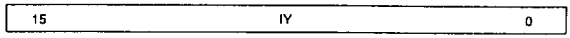
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2	SCI Control Register
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE		SCCR	SCI Status Register
$102F	Bit 7	—	—	—	—	—	—	Bit 0	SCDR	SCI Data (Read RDR, Write TDR)
$1030	CCF		SCAN	MULT	CD	CC	CB	CA	ADCTL	A/D Control Register
$1031	Bit 7	—	—	—	—	—	—	Bit 0	ADR1	A/D Result Register 1
$1032	Bit 7	—	—	—	—	—	—	Bit 0	ADR2	A/D Result Register 2
$1033	Bit 7	—	—	—	—	—	—	Bit 0	ADR3	A/D Result Register 3
$1034	Bit 7	—	—	—	—	—	—	Bit 0	ADR4	A/D Result Register 4
$1035				PTCON	BPRT3	BPRT2	BPRT1	BPRT0	ADR1	EEPROM Block Protect Reg.
$1036 Thru $1038									Reserved	
$1039	ADPU	CSEL	IRGE	DLY	CME		CR1	CR0	OPTION	System Configuration Options
$103A	Bit 7	—	—	—	—	—	—	Bit 0	COPRST	Arm/Reset COP Timer Circuitry
$103B	ODD	EVEN	—	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG	EEPROM Prog. Control Reg.
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO	Highest Priority I-Bit Int and Misc
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT	RAM and I/O Mapping Reg.
$103E	TILOP		OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1	Factory TEST Control Register
$103F	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON	CONFIG	COP, ROM, and EEPROM Enables.

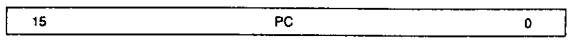
INDEX REGISTER Y (IY)

This index register is an 16-bit register used for the indexed addressing mode similar to the IX register ; however, most instructions using the IY register are two-byte opcodes and require an extra byte of machine code and an extra cycle of execution time. The index register may also be used as a counter or a temporary storage area.



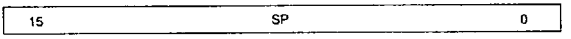
PROGRAM COUNTER (PC)

The program counter is a 16-bit register that contains the address of the next byte to be fetched.



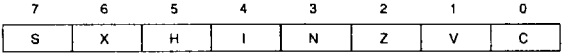
STACK POINTER (SP)

The stack pointer is a 16-bit register that contains the address of the next free location on the stack. The stack is configured as a sequence of last-in-first-out read/write registers, which allow important data to be stored during interrupts and subroutine calls. Each time a new byte is added to the stack, the SP is incremented ; each time a byte is removed, the SP is incremented. The address contained in the SP also indicates the location at which the accumulators A and B registers IX and IY can be stored during certain instructions.



CONDITION CODE REGISTER (CCR)

The condition code register is an 8-bit register in which each bit is used to indicate the results of the instruction just executed. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.



Carry/Borrow (C)
When set, this bit indicates that a carry of borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during shift and rotate instructions.

Overflow (V)
The overflow bit is set if an arithmetic overflow occured as a result of the operation ; otherwise the V bit is cleared.

Zero (Z)
When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Negative (N)
When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (the MSB of the result is a logic one).

Interrupt (I)
This bit is set either by hardware or program instruction to disable (mask) all maskable interrupt sources (both external and internal).

Half carry (H)
This bit is set during ADD, ABA, and ADC operations to indicate that a carry occured between bits 3 and 4. This bit is mainly useful in BCD calculations.

X interrupt mask (X)
This mask bit is set only by hardware (reset or $\overline{XIRQ}$) and is cleared only by program instruction (TAP or RTI).

Stop disable (S)
This bit, under program control, is set to disable the STOP instruction, and is cleared to enable the STOP instruction. The STOP instructions is treated as no operation (NOP) if the S bit is set.

6.6 · Resets

The MCU can be reset four ways :

- an active low input to the $\overline{RESET}$ pin,
- a power-on reset function,
- a computer operating properly (COP) watchdog-timer timeout and,
- a clock monitor failure.

The $\overline{RESET}$ input consists mainly of a Schmitt trigger that senses the $\overline{RESET}$ line logic level.

RESET PIN

To request an external reset, the $\overline{RESET}$ pin must be held low for eight E_{cyc} (two E_{cyc} if no distinction is needed between internal and external resets). To prevent the EEPROM contents from being corrupted during power transitions, the reset line should be held low while V_{DD} is below its minimum operating level. A low voltage inhibit (LVI) circuit is required to protect EEPROM from corruption as shown in Figure 21.

POWER-ON RESET (POR)

Power-on reset occurs when a positive transition is detected on V_{DD}. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drop in the power supply voltage. If the external $\overline{RESET}$ pin is low at the end of the power-on delay time, the processor remains in the reset condition until $\overline{RESET}$ goes high.

COMPUTER OPERATING PROPERLY (COP) RESET

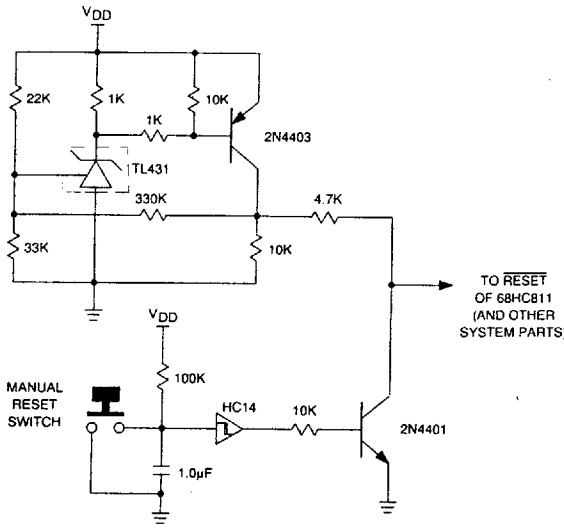
The MCU contains a watchdog timer that automatically times out if not reset within a specific time by a program reset sequence. If the COP watchdog timer is allowed to timeout, a reset is generated, which drives the $\overline{RESET}$ pin low to reset the MCU and the external system.

The COP reset function can be enabled or disabled by setting the control bit in an EEPROM cell of the system configuration register. Once programmed, this control bit remains set (or cleared) even when no power is applied, and the COP function is enabled or disabled independent of resident software. Protected control bits (CR1 and CR0),in the configuration options register, allow the user to select one of four COP timeout rates. Table 12 shows the relationship between CR1 and CR0 and the COP timeout period for various system clock frequencies.

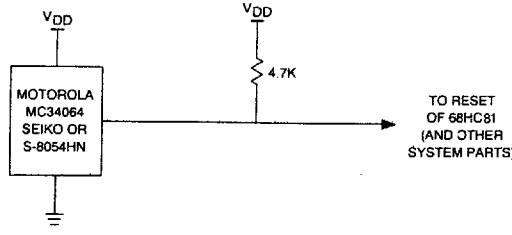
CLOCK MONITOR RESET

The MCU contains a clock monitor circuit which measures the E clock input frequency. If the E clock input rate is above 200 kHz, then the clock monitor does not generate a MCU reset. If the E clock signal is lost or its frequency falls below 10 kHz, then a MCU reset is generated, and the $\overline{\text{RESET}}$ pin is driven low to reset the external system.

The clock monitor reset can be enabled or disabled by a read-write control bit (CME) in the system configuration options register.



Reset Circuit with LVI and RC Delay



Simple LVI Reset Circuits

Figure 21 : Typical LVI reset circuits.

Table 12 - COP timeout periods

CR1	CR0	E/2^{15} divided by	XTAL = 2^{23} timeout −1/+15.6 ms	XTAL = 8.0 MHz timeout −0/+16.4 ms	XTAL = 4.9152 MHz timeout −0/+26.7 ms	XTAL = 4.0 MHz timeout −0/+32.8 ms	XTAL = 3.6864 MHz timeout −0/+35.6 ms
0	0	1	15.625 ms	16.384 ms	26.667 ms	32.768 ms	35.556 ms
0	1	4	62.5 ms	65.536 ms	106.67 ms	131.07 ms	142.22 ms
1	0	16	250 ms	262.14 ms	426.67 ms	524.29 ms	568.89 ms
1	1	64	1 s	1.049 s	1.707 s	2.1 s	2.276 s
		E =	2.1 MHz	2.0 MHz	1.2288 MHz	1.0 MHz	921.6 kHz

6.7 - Interrupts

There are seventeen hardware and one software interrupts (excluding reset type interrupts) that can be generated from all the possible sources. These interrupts can be divided into two categories, maskable and non-maskable. Fifteen of the interrupts can be masked with the condition code register I bit. All the on-chip interrupts are individually maskable by local control bits. The software interrupt is non-maskable. The external input to the $\overline{\text{XIRQ}}$ pin is considered a non-maskable interrupt because, once enabled, it cannot be masked by software ; however, it is masked during reset and upon receipt of an interrupt at the $\overline{\text{XIRQ}}$ pin. The last interrupt, illegal opcode, is also a non-maskable interrupt. Table 13 provides a list of each interrupt, its vector location in ROM, and the actual condition code and control bits that mask it. Figure 22 shows the interrupt stacking order.

SOFTWARE INTERRUPT (SWI)

The SWI is executed the same as any other instruction and will take precedence over interrupts only if the other interrupts are masked (I and X bits in the CCR set). The SWI execution is similar to the maskable interrupts such as setting the I bit. CPU registers are stacked, etc.

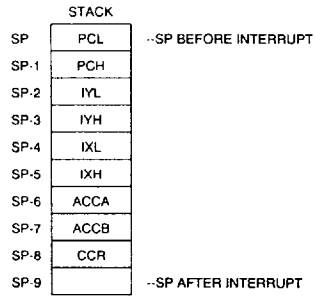


Figure 22 : Stacking order.

Note : The SWI instruction cannot be fetched as long as another interrupt is pending execution. However, once fetched, no other interrupt can be honored until the first instruction in the SWI service routine is completed.

Table 13 - Interrupt vector assignments

Vector address	Interrupt source	CC register mask	Local mask
FFC0, C1	Reserved		
*	*		
*	*		
FFD4, D5,	Reserved		
FFD6, D7	SCI serial system	I bit	
	Receive data register full		RIE
	Receive overrun		RIE
	Idle line detect		ILIE
	Transmit data register empty		TIE
	Transmit complet		TCIE

Table 13 - Interrupt vector assignments (continued)

Vector address	Interrupt source	CC register mask	Local mask
FFD8, D9	SPI serial transfer complete	I bit	SPIE
FFDA, DB	Pulse accumulator input edge	I bit	PAII
FFDC, DD	Pulse accumulator overflowd	I bit	PAOVI
FFDE, DF	Timer overflow	I bit	TOI
FFE0, E1	Timer output compare 5	I bit	OC5I
FFE2, E3	Timer output compare 4	I bit	OC4I
FFE4, E5	Timer output compare 3	I bit	OC3I
FFE6, E7	Timer output compare 2	I bit	OC2I
FFE8, E9	Timer output compare 1	I bit	OC1I
FFEA, EB	Timer input capture 3	I bit	OC3I
FFEC, ED	Timer input capture 2	I bit	OC2I
FFEE, EF	Timer input capture 1	I bit	OC1I
FFF0, F1	Real-time interrupt	I bit	RTII
FFF2, F3	IRQ (external pin or parallel I/O)	I bit	
	External pin		None
	Parallel I/O handshake		STAI
FFF4, F5	XIRQ pin (pseudo non-maskable interrupt)	X bit	None
FFF6, F7	SWI	None	None
FFF8, F9	Illegal opcode trap	None	None
FFFA, FB	COP failure (reset)	None	NOCOP
FFFC, FD	COP clock monitor fail (reset)	None	CME
FFFE, FF	RESET	None	None

ILLEGAL OPCODE TRAP

Since not all possible opcodes or opcode sequences are defined, an illegal opcode detection circuit has been included in the MCU. When an illegal opcode is detected, an interrupt is requested to the illegal opcode vector.

REAL-TIME INTERRUPT

The real-time interrupt provides a programmable periodic interrupt. This interrupt is maskable by either the I bit in the CCR or the RTII control bit. The rate is based on the MCU E clock and is software selectable to be $E/2^{13}$, $E/2^{14}$, $E/2^{15}$, or $E/2^{16}$.

6.8 - Low-power modes

The MCU contains two programmable low-power operating modes : stop and wait. In the wait mode, the on-chip oscillator remains active ; in the stop mode, the oscillator is stopped. The following paragraphs describe the tow low-power modes.

STOP

The STOP instruction places the MCU in its lowest power consumption mode, provided the S bit in the CCR is clear. In this mode, all clocks are stopped, thereby halting all internal processing.

To exit the stop mode, a low level must be applied to either $\overline{IRQ}$, $\overline{XIRQ}$ or $\overline{RESET}$. An external interrupt used at $\overline{IRQ}$ is only effective if the I bit in the CCR is clear. An external interrupt applied at the $\overline{XIRQ}$ input would be effective regardless of the X-bit setting in the CCR ; however, the actual recovery sequence differs, depending on the X-bit setting. If the X bit is clear, the MCU starts with the stacking sequence leading to the normal service of the $\overline{XIRQ}$ request. If the X bit is set, the processing will always continue with the instruction immediately following the STOP instruction. A low jnput to the $\overline{RESET}$ pin will always result in an exit from the stop mode, and the start of MCU operations is determined by the reset vector.

A restart delay is required if the internal oscillator is being used, to allow the oscillator to stabilize when exiting the stop mode. If a stable external oscillator is being used, a control bit in the OPTION register may be used (cleared) to bypass the delay. If the control bit is clear, then the $\overline{RESET}$ pin would not normally be used for exiting the stop mode. In this case, the reset sequence sets the delay control bit, and the restart delay will be imposed.

WAIT

The WAIT instruction places the MCU in a low-power consumption mode, but the WAIT mode consumes slightly more power than the STOP mode. In the WAIT mode, the oscillator is kept running. Upon execution of the WAIT instruction, the machine state is stacked and program execution stops. The WAIT state can only be exited by an unmasked interrupt or $\overline{RESET}$. If the I bit is set and the COP is disabled, the timer system will be turned off to further reduce power consumption. The amount of power savings is application dependent and depends upon circuitry connected to the MCU pins and upon subsystems (i.e., timer, SPI SCI) that are active when the WAIT mode is entered. Turning off the A/D subsystem by clearing ADPU further reduces WAIT-mode current.

6.9 - Programmable timer

The timer system uses a «time-of-day» approach in that all timing functions are related to a single 16-bit free-running counter. The free-running counter is clocked by the output of a programmable prescaler (divide by 1, 4, 8, or 16), which is, in turn, clocked by the MCU E clock. The free-running counter can be read by software at any time without affecting its value because it is clocked and read on opposite half cycles of the E clock. The counter is cleared on reset and is a read-only register. The counter repeats every 65,536 counts, and when the count changes from $FFFF to $0000, a timer overflow flag bit is set. The overflow flag also generates an internal interrupt if the overflow interrupt enable bit is set. The timer has three input capture and five output compare functions. The functions and registers of the timer are explainded in the following paragraphs.

INPUT CAPTURE FUNCTION

There are four 16-bit read-only input capture registers that are not affected by reset. Each register is used to latch the value of the free-running counter when a selected transition at an external pin is detected. External devices provide the inputs on the PA0-PA3 pins, and an interrupt can be generated when an input capture edge is detected. The time of detection can be read from the appropriate register as part of the interrupt routine.

Port A pin 3 serves multiples functions. After reset, data direction bit 3 (DDRA3) in the PACTL register is cleared to zero configuring port A pin 3 as an input. Port A pin 3 can then be used as a input capture 4 (IC4), by setting 14/05 to «one» in the PACTL register. The 14/05 bit is configured to OC5 (cleared to zero) on reset. If DDRA3 is configured as an output and IC4 is enabled, writes to port A bit 3 causes edges on the PA3 to result in input captures. When the TI1405 register is acting as the IC4 capture register it cannot be written to. When PA3 is being used as IC4, writes to TI405 register have no meaning.

TIMER CONTROL REGISTER 2 (TCTL2) $1021

7	6	5	4	3	2	1	0
EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET							
0	0	0	0	0	0	0	0

EDGxB and EDGxA — input capture x edge control.

These two bits (EDGxB and EDGxA) are cleared to zero by reset and are encoded to configure the input sensing logic for input capture x.

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any (rising or faling) edge

6

OUTPUT COMPARE FUNCTION

There are five 16-bit read/write output compare registers, which are set to $FFFF on reset. A value written into the SE registers is compared to the free-running counter value during each E-clock cycle. If a match is found, the particular output compare flag is set, and an interrupt is generated, provided that particular interrupt is enabled.

In addition to the interrupt, a specified action may be intitiated at a timer output pin(s). For output compare one (OC1), the output action to be taken when a match is found is controlled by a 5-bit mask register and a 5-bit data regiser. The mask register specifies which timer port outputs are to be used, and the data register specifies what data is placed on the SE timer ports. For OC2 through OC5, one specific timer output is affected as controlled by the two-bit fields in a timer control register. These action include :

- timer disconnect from output pin logic,
- toggle output compare line,
- clear output compare line to zero, or
- set output compare line to one.

Upon reset, 14/05 is configured as OC5. The OC5 function overides DDRA3 to force the Port A pin 3 to be an output whenever OM5 : OL5 bits are not 0 : 0. In all other aspects, OC5 works the same as the other output compare.

TIMER COMPARE FORCE REGISTER (CFORC) $100B

This 8-bit write-only register is used to force early output compare actions. This compare force function is not recommended for use with the output toggle function because a normal compare occurring immediately before or after the force may result in undersirable operation.

7	6	5	4	3	2	1	0
FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
RESET							
0	0	0	0	0	0	0	0

F0C1-F0C5 — Force output compare x action
1 = causes action programmed for output compare x, except the OCxF flag bit is not set.
0 = has no meaning
Bits 2-0 — not implemented. These bits always read zero.

These bits always read zero.

OUTPUT COMPARE 1 MASK REGISTER (0C1M) $100C

This register is used with output compare 1 to specify the bits of port A which are affected as a result of a successful OC1 compare.

7	6	5	4	3	2	1	0
OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
RESET							
0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding pin(s) of port A.

OUTPUT COMPARE 1 DATA REGISTER (OC1D) $100D

This register is used with output compare 1 to specify the data which is to be stored to the affected bit of port A as a result of a successful OC1 compare.

7	6	5	4	3	2	1	0
OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
RESET							
0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit-x on successful OC1 compares.

TIMER CONTROL REGISTER (TCTL1) $1020

7	6	5	4	3	2	1	0
OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET							
0	0	0	0	0	0	0	0

OM2-OM5 — output mode
OL2-OL5 — output level.
These control bit pairs (OMx and OLx) are encoded to specify the output action taken as a result of a successful OCx comppare.

OMx	OLx	Action taken upon successful compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

TIMER INTERRUPT MASK REGISTER 1 (TMSK1)

7	6	5	4	3	2	1	0
OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I
RESET							
0	0	0	0	0	0	0	0

OCxI — output compare x interrupt
1 = interrupt sequence requested if OCxF = 1 in TFLG1
0 = interrupt inhibited

¦ Cx ¦ — input capture x interrupt
1 = interrupt sequence requested if ICxF = 1 in TFLG1
0 = interrupt inhibited.

Note : when the 14/05 bit in the PACTL register is one, the ¦ 405 ¦ bit behaves as the input capture 4 interrupt bit. When 14/05 is zero, the ¦ 405 ¦ bit acts as the output compare 5 interrupt control bit.

TIMER INTERRUPT FLAG REGISTER 1 (TFLG1)

This register is used to indicate the occurence of timer system events and, with the TMSK1 register, allows the timer sybsystem to operate in a polled or interrupt driven system. Each bit in the TFLG1 has a corresponding bit in the TMSK1 in the same bit position.

7	6	5	4	3	2	1	0
OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F
RESET							
0	0	0	0	0	0	0	0

OCxF — output compare x flag
Set each time the timer counter matches the output compare register x value. To clear a flag bit in TFLG1, you must write a «one» to the corresponding bit position(s).
1 = bit cleared
0 = not affected.

ICxF — input capture x flag
Set each time a selected active edge is detected on the ICx input line. To clear a flag bit in TFLG1, you must write a «one» to the corresponding bit position(s).
1 = bit cleared
0 = not affected.

Note : When the 14/05 bit in the PACTL register is one, the I405F bit behaves as the input capture 4 flag bit. When 14/05 is zero, the ¦ 405 ¦ bit acts as the output compare 5 flag.

TIMER INTERRUPT MASK REGISTER 2 (TMSK2) $1024

This register is used to control whether or not a hardware interrupt sequence is requested as a result of a status bit being set in TFLG1. Two timer prescaler bits are also included in this register.

7	6	5	4	3	2	1	0
TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET							
0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt enable
1 = interrupt request when TOF = 1
0 = TOF interrupt disabled.

RTII — RTI Interrupt enable
1 = interrupt requested when RTIF = 1
0 = RTIF interrupt disabled

PAOVI — Pulse Accumulator OVerflow Interrupt enable
1 = interrupt requested when PAOVF = 1
0 = PAOVF disabled.

PAII — Pulse Accumulator Input Interrupt enable
1 = interrupt requested when PAIF = 1
0 = PAIF disabeld.

Bits 3-2 — not implemented
These bits always read zero.

PR1 and PR0 — timer prescaler selects.
Can only be written to during intitialization. Writes are disabled after the first write or after 64 E cycles our of reset.

PR1	PR0	Divide-by-factor
0	0	1
0	1	4
1	0	8
1	1	16

TIMER INTERRUPT FLAG REGISTER 2 (TFLG2)

This register is used to indicate the occurrence of timer system events and, with the TMSK2 register, allows the timer subsystem to operate in a polled or interrupt driven system. Each bit in the TFLG2 has a corresponding bit in the TMSK2 in the same bit position.

7	6	5	4	3	2	1	0
TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET							
0	0	0	0	0	0	0	0

TOF — Timer Overflow

Set to one each time the 16-bit free-running counter advances from a value of $FFFF to $0000. Cleared by a write to TFLG2 with bit 7 set.

RTIF — Real-Time Interrupt Flag

Set at each rising edge of the seleted tap point. Cleared by a write to TFLG2 with bit 6 set.

PAOVF — Pulse-Accumulator OVerflow interrupt Flag

Set when the count in the pulse accumulator rolls over from $FF to $00. Cleared by a write to the TFLG2 with bit 5 set.

PAIF — Pulse-Accumulator Input-edge interrupt Flag

Set when an active edge is detected on the PAI input pin. Cleared by a write to TFLG2 with bit 4 set.

Bits 3-0 — not implemented

These bits always read zero.

6.10 - Pulse accumulator

The pulse accumulator is an 8-bit counter that can operate in either of two modes, depending on the state of a control bit in the PACTL register. These are the event counting mode and the gated time accumulation mode. In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is E clock divided by two. In the gated time accumulation mode, a free-running E clock/64 signal drives the 8-bit counter, but only while the external PAI input pin is activated.

PULSE ACCUMULATOR CONTROL REGISTER (PACTL) $1026

Four bits in this register are used to control an 8-bit pulse accumulator system, and tow other bits are used to select the rate for the real-time interrupt system.

7	6	5	4	3	2	1	0
DDRA7	PAEN	PAMOD	PEDGE	DDRA3	14/05	RTR1	RTR0
RESET							
0	0	0	0	0	0	0	0

DDRA7 — Data Direction for port A bit 7

1 = output

0 = input only

PAEN — Pulse-Accumulator system ENable

1 = pulse accumulator on

0 = pulse accumulator off

PAMOD — Pulse Accumulator Mode

1 = gated time accumultor

0 = exernal even counting

RTR1	RTR0	Divide E by	XTAL = 2^{23}	XTAL = 8.0 MHz	XTAL = 4.9152 MHz	XTAL = 4.0 MHz	XTAL = 3.6864 MHz
0	0	2^{13}	3.91 ms	4.10 ms	6.67 ms	8.19 ms	8.89 ms
0	1	2^{14}	7.81 ms	8.19 ms	13.33 ms	16.38 ms	17.78 ms
1	0	2^{15}	15.62 ms	16.38 ms	26.67 ms	32.77 ms	35.56 ms
1	1	2^{16}	31.25 ms	32.77 ms	53.33 ms	65.54 ms	71.11 ms
		E =	2.1 MHz	2.0 MHz	1.2288 MHz	1.0 MHz	921.6 kHz

PEDGE — Pulse accumulator EDGE control

This bit provides clock action along with PAMOD.

1 = sensitive to rising edges at PAI pin if PAMOD = 0. In gated accumulation mode counting is enabled by a low on PAI pin if PAMOD = 1.

0 = sensitive to falling edges at PAI pin if PAMOD = 0. In gated accumulation mode counting is enabled by a high on PAI pin if PAMOD = 1

DDRA3 — Data Directional for port A bit 3

1 = output

0 = input only.

14/05 — Input 4/output 5

1 = input capture 4 function enabled (No OC5)

0 = output compare 5 function enabled (No IC4).

RTR1 and RTR0 — RTI interrupt rate selects.

These two bits slect one of four rates for the real-time peirodic interrupt circuits. Reset clears these two bits and after reset, a full RTI period elapses before the first RTI interrupt.

6

6.11 - EEPROM programming

The 2K bytes of EEPROM are located at $F800 through $FFFF. Programming of the EEPROM is controled by the EEPROM programming control register (PPROG). The EEPROM is disabled when the EEON bit in the system configuration register (CONFIG) is zero. Programming and erasure of the EEPROM relies on an internal high-voltage charge pump. At E clock frequencies below 2 MHz, the efficiency of this charge pump decreases, which increases the time required to program or erase a location. Recommended program and erase time is 10 milliseconds when the E clock is between 2 MHz and should be increased to as much as 20 milliseconds when E clock is between 1 MHz and 2 MHz. When E clock below 1 MHz, the clock source for the charge pump should be switched from the system clock to an on-chip R-C oscillator clock. This is done by setting the CSEL bit in the OPTION register. A 10 millisecond period should be allowed after setting the CSEL bit to allow the charge pump to stabilize. The following paragraphs describe how to program or erase the EEPROM using the PPROG control register.

EEPROM BLOCK PROTECT REGISTER (BPROT) $1035

This 5-bit register protects against inadvertent writes to the CONFIG register and to the EEPROM. To permit the user to separate EEPROM into categories like «temporary» or «permanent», EEPROM is divided inot four individually protected blocks. The CONFIG register is also protected.

In normal operating modes, EEPROM and CONFIG are protected out of reset, and the user has 64 E clock cycles to unprotect any of the blocks that will require programming or erasing. The BPROT register bits can only be cleared, written to zero, during the first 64 E clock cycles after reset. Once the bits are cleared, the associated EEPROM section and/or the CONFIG register can be programmed or erased in the normal manner. The EEPROM is visible only if the EEON bit in the CONFIG register is set. In the test or bootstrap modes, bits of the BPROT register can be set or cleared at any time. In either single-chip or expanded mode, BPROT register bits can be writtent back to one anytime after the first 64 E clock cycles in order to protect the EEPROM and/or the CONFIG register. However, these bits can only be cleared again in the test or bootstrap modes.

7	6	5	4	3	2	1	0
0	0	0	ITCON	BPRT3	BPRT2	BPRT1	BPRT0
RESET							
0	0	0	1	1	1	1	1

Bits 7-5 — Not implemented

These bits always read zero.

PTCON — Protect CONFIG register bit.

1 = programming / erasure of the CONFIG register disabled

0 = programming / erasure of the CONFIG register allowed.

BPRT3-BPRT0 — block protect bits

1 = a set bit protects a block of EEPROM against programming or erasure

0 = a cleared bit permits programming or erasure of the associated block.

Bit	Block protected	Block size
BPRT0	$1800-19FF	512 bytes
BPRT1	$1A00-1BFF	512 bytes
BPRT2	$1C00-1DFF	512 bytes
BPRT3	$1E00-1FFF	512 bytes

ERASING THE EEPROM

Erasure of the EEPROM is controled by bit settings in PPROG, and the appropriate bits int eh BPROT register must also be cleared before the EEPROM can be changed. Programs can be written to perform bulk, row, or byte erase. In bulk erase, all 2048 bytes of the EEPROM are erased. In row erase, 16 bytes ($F800-$F80F-$F810-$F81F, etc) are erased. Other MCU operations can continue to be performed during erasing provided the operations do not include reads of data from EEPROM.

PROGRAMMING EEPROM

During programming, the ROW and BYTE bits are not used. If the E clock frequency is 1 MHz or less, the CSEL bit in the OPTION register must be set. Zeros must be erased by a separate erase operation before programming. Other MCU operations can continue to be performed during programming provided the operations do not include reads of data from EEPROM.

EEPROM PROGRAMMING CONTROL REGISTER (PPROG) $103B

This 8-bit register is used to control programming and erasure of the EEPROM. This register is cleared on reset so the EEPROM is configured for normal reads.

7	6	5	4	3	2	1	0
ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM
RESET							
0	0	0	0	0	0	0	0

ODD — program odd rows (TEST)

EVEN — program even rows (TEST)

Bit 5 — not implemented.

This bit always reads zero.

BYTE — byte erase select.

This bit overrides the ROW bit.

1 = erase only one byte

0 = row or bulk erase.

ROW — row erase select.

If BYTE bit = 1, ROW has no meaning.

1 = row erase

0 = bulk or byte erase.

ERASE — erase mode select.

1 = erase mode

0 = normal read or program.

EELAT — EEPROM latch control.

1 = EEPROM address and data configured for programming/erasing

0 = EEPROM address and data configured for read mode.

EEPGM — EEPROM programming voltage enable

1 = programming voltage turned on

0 = programming voltage turned off.

Note : A strict register access seaquence must be followed to allow successfult programming and erase operations. The following procedures for modifying the EEPROM and CONFIG register detail the sequence. If an attempt is made to set bothe the EELAT and EEPGM bits in the same write cycle and if this attempt occurs before the required write cycle with the EELAT bit set, then neither is set. If a write to an EEPROM address is performed while the EEPGM bit is set, the write is ignored, and the programming operation in progress is not disturbed. If no EEPROM address is written between when EELAT is set and EEPGM is set, then no program or erase operation takes place. These safeguards were included to preven accidental EEPROM changes in cases of program runaway.

ERASING THE CONFIG REGISTER

Erasing the CONFIG register follows the same procedures as that used for the EEPROM including bulk, byte, and row erase. The CONFIG register may be programmed or erased while the MCU is operating in any mode depending on the setting of bit 4 in BPROT.

PROGRAMMING THE CONFIG REGISTER

Programming the CONFIG register follows the same procedures as that used for the EEPROM except the CONFIG register address is used.

SYSTEM CONFIGURATION REGISTER (CONFIG) $103F

The CONFIG is implemented in EEPROM cells and controls the presense of ROM and EEPROM in the memory map and enables the COP watchdog system.

7	6	5	4	3	2	1	0
EE3	EE2	EE1	EE0	0	NOCOP	0	EEON

EE0-EE3 — EEPROM map position

These four bits specify the upper four bits of the EEPROM address. These bit have no meaning in the single-chip mode, because the 2K EEPROM is forced on a locations $F800 through $FFFF.

EE3	EE2	EE1	EE0	Location
0	0	0	0	$0800-$0FFF
0	0	0	1	$1800-$1FFF
0	0	1	0	$2800-$2FFF
0	0	1	1	$3800-$3FFF
0	1	0	0	$4800-$4FFF
1	0	1	0	$5800-$5FFF
0	1	1	0	$6800-$6FFF
0	1	1	1	$7800-$7FFF
1	0	0	0	$8800-$8FFF
1	0	0	1	$9800-$9FFF
1	0	1	0	$A800-$AFFF
1	0	1	1	$B800-$BFFF
1	1	0	0	$C800-$CFFF
1	1	0	1	$D800-$DFFF
1	1	1	0	$E800-$EFFF
1	1	1	1	$F800-$FFFF

Bit 3 — not implemented

This bit always reads one.

NOCOP — COP system disable

1 = COP watchdog system disabled

0 = COP watchdog system enabled

Bit 1 — not implemented

This bit always reads zero.

EEON — enable on-chip EEPROM

When this bit is programmed to «zero», the 2048-byte EEPROM is disabled, and that memory space becomes externally accessed space.

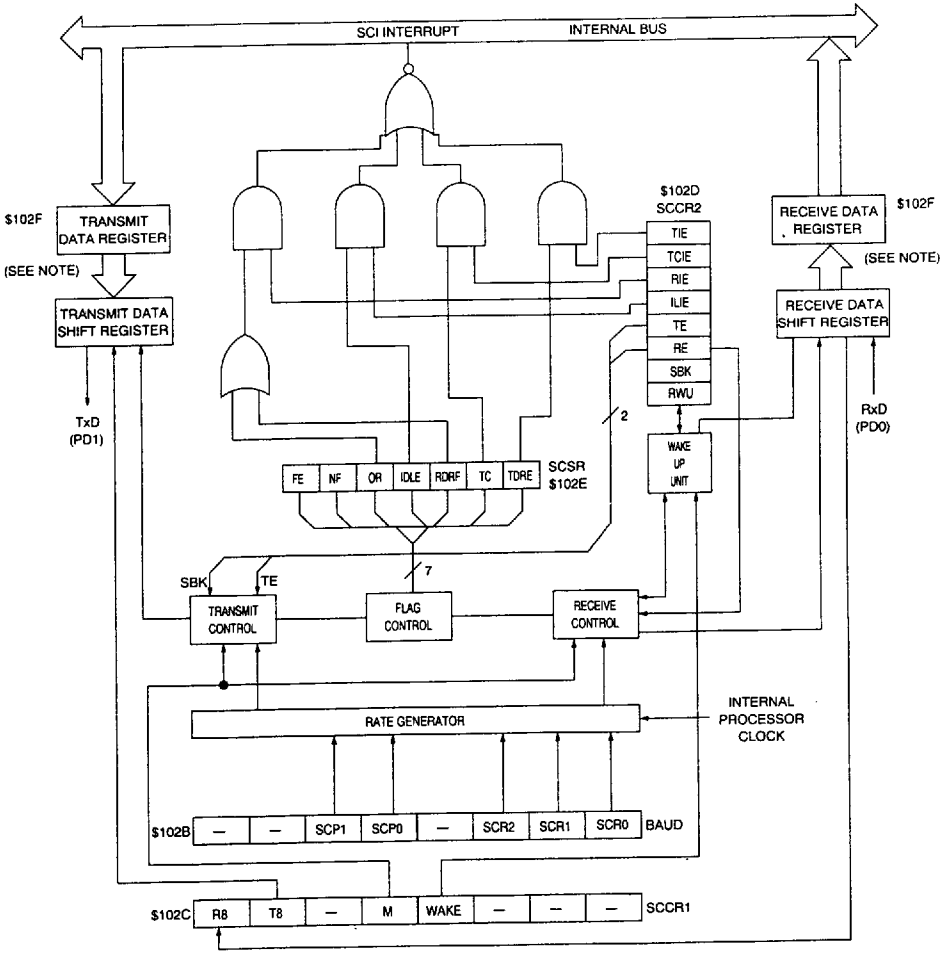
6.12 · Serial communications interface

The serial communications interface (SCI) allows the MCU to be interfaced efficiently with peripheral devices that require an asynchronous serial data format. The SCI uses a standard NRZ format with a variety of baud rates derived from the crystal clock circuit. Interfacing is accomplished using port D pins : PD0 for receive data (RxD) and PD1 for the transmit data (TxD). The baud-rate generation circuit contains a programmable prescaler and divider clocked by the MCU E clock. Figure 23 shows a block diagram of the SCI.

DATA FORMAT

Receive data in or transmit data out is the serial data presented between the PD0 and the internal data bus and between the internal data bus and PD1. The data format requires :

– an idle line in the high state prior to transmission/reception of a message,



Note : The serial communications data register (SCDR) is controlled by the internal R/W signal. It is the transmit data register when written and received data register when read.

Figure 23 : SCI block diagram.

- a start bit that is transmitted/received, indicating the start of each character,
- data that is transmitted and received least-significant bit (LSB) first,
- a stop bit (tenth or eleventh bit set to logic one), which indicates the frame is complet ; and
- a break defined as the transmission or reception of a logic zero for some multiple of frames.

Selection of the word length is controlled by the M bit in serial communications control register 1 (SCCR1).

TRANSMIT OPERATION

The SCI transmitter includes a parallel data register and a serial shift register. This double-buffered system allows a character to be shifted out serially while another character is waiting in the transmit data register to be transferred into the serial shift register. The output of the serial shift register is applied to PD1 as long as transmission is in progress or the transmit enable bit is set.

RECEIVE OPERATION

Data is received in a serial shift register and is transferred to a parallel receive data register as a complete word. This double-buffered system allows a character to be shifted in serially while another character is already in the receive data register. An advanced data recovery scheme is used to distinguish valid data from noise in the serial data stream. The data input is selectively sampled to detect receive data, and a majority voting circuit determines the value and intergrity of each bit.

WAKE-UP FEATURE

The wake-up feature reduces SCI service overhead in multiple receiver systems. Software for each receiver evaluates the first character(s) of each message. If the message is intended for a different receiver, the SCI can be placed in a sleep mode, disabling the rest of the message from generating requests for service. Whenever a new message begins, logic causes the sleeping receivers to awaken and evaluate the initial character(s) of the new message. Two methods of wake up are available : idle-line wake up or address mark wake up. In idle-line wake up, a sleeping receiver wakes up as soon as the RxD line becomes idel. In the address mark wake up, a «one» in the most-significant bit (MSB) of a character is used to indicate that the message is an address that wakes up a sleeping receiver.

SCI REGISTERS

The following paragraphs describe the operations of the five registers used in the SCI.

Serial communications data registers (SCDR)
The SCDR performs two functions : as the receive data register when it is read and as the transmit data register when it is written. Figure 23 shows the SCDR as two separate registers.

Serial communications control register 1 (SCCR1)
The SCCR1 provides the control bits to determine word length and select the method used for the wake-up feature.

7	6	5	4	3	2	1	0
R8	T8	0	M	WAKE	0	0	0
RESET							
U	U	0	0	0	0	0	0

R8 — receive data bit 8

If the M bit is set, this bit provides a storage location for the ninth bit in the receive data character.

T8 — transmit data bit 8

If the M bit is set, this bit provides a storage location for the ninth bit in the transmit data character.

Bit 5 — not implemented

This bit always reads zero.

M — SCI character length

1 = 1 start bit, 9 data bits, 1 stop bit
0 = 1 start bit, 8 data bits, 1 stop bit.

WAKE — wake-up method select

1 = address mark
0 = idle line.

Bits 2-0 — not implemented

These bits always read zero.

Serial conmmunications control register 2 (SCCR2)
The SSCR2 provides the control bits that enable/disable individual SCI functions.

7	6	5	4	3	2	1	0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET							
0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
1 = SCI interrupt if TDRE = 1
0 = TDR interrupts disabled.

TCIE — Transmit-Complete Interrupt Enable
1 = SCI interrupt if TC = 1
0 = TC interrupts disabled.

RIE — Receive Interrupt Enable
1 = SCI interrupt if RDRF or OR = 1
0 = RDRF or OR interrupt disabled.

ILIE — Idle-Line Interupt Enable
1 = SCI interrupt if IDLE = 1
0 = IDLE interrupt disabled.

TE — Transmit Enable
1 = transmit shift register output is applied to the TxD line
0 = PD1 pin reverts to general-purpose I/O as soon as current transmitter activity finishes.

RE — Receive Enable
1 = receiver enabled
0 = receiver disabled and RDRF, IDLE, OR, NF, and FE interrupts are inhibited.

RWU — Receiver Wake Up
When set by user's software, this bit puts the receiver to sleep and enables the «wake-up» function. If the WAKE bit is zero, RWU is cleared by the SCI logic after receiving 10 (M = 0) or 11 (M = 1) consecutive ones. If WAKE is one, RWU is cleared by the SCI logic after receiving a data word whose MSB is set.

SBK — Send BreaK
If this bit is toggled set and cleared, the transmitter sends 10 (M = 0) or 11 (M = 1) zeros and then reverts to idle or to sending data. If SBK remains set, the transmitter will continually send whole frames of zeros (sets of 10 or 11) until cleared.

Serial communications status register (SCSR)
The SCSR provides inputs to the interrupt logic circuits for generation of the SCI system interrupts.

7	6	5	4	3	2	1	0
TDRE	TC	RDRF	IDLE	OR	NF	FE	0
RESET							
1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty
1 = automatically set when contents of the serial communications data register was transferred to the transmit serial shift register
0 = cleared by a read of SCSR (with TDRE = 1) followed by a write to SCDR.

TC — Transmit Complete
1 = automatically set when all data frame, preambel, or break condition transmissions are complete
0 = cleared by a read of SCSR (with TC = 1) followed by a write to SCDR.

RDRF — Receive Data Register Full
1 = automatically set when a character is transferred from the receiver shift register to the SCDR
0 = cleared by a read of SCSR (with RDRF = 1) followed by a read of SCDR.

IDLE — IDLE-line detect
This bit is inhibited while RWU = 1.
1 = automatically set when the receiver serial input becomes idle after having been active
0 = cleared by a read of SCSR (with IDLE = 1) followed by a read of SCDR.

OR — Overrun error
1 = automatically set when a new character cannot transfer from the receive shift register because the character in SCDR has not been read
0 = cleared by a read of SCSR (with OR = 1) followed by a read of SCDR.

NF — Noise Flag
1 = automatically set when majority voting logic does not bind unanimous agreement of all samples in any bit in the recieved frame
0 = cleared by a read of SCSR (with NF = 1) followed by a write to SCDR.

FE — Framing Error

1 = automatically set when a logic 0 is detected where a stop bit was expected

0 = cleared by a read of SCSR (with FE = 1) followed by a read of SCDR.

Bit 0 — not implemented

This bit always reads zero.

Baud-rate register (BAUD)

This register is used to select different baud rates that may be used as the rate control for the receiver and transmitter.

7	6	5	4	3	2	1	0
TDLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET							
1	1	0	0	0	U	U	U

TCLR — clear baud-rate counters (test)

This bit is used to clear the baud-rate counter chain during factory testing. TCLR is zero and cannot be set while in normal operating modes.

Bit 6 — not implemented

This bit always reads zero.

SCP1 and SCP0 — SCI baud-rates prescaler selects

These bits control a prescaler whose output provides the input to a second divider which is controlled by the SCR2-SCR0 bits. Refer to Table 14.

RCKB — SCI baud-rate clock check (test)

This bit is used during factory testing to enable the exlcusive-OR of the receiver clock and transmitter clock to be driven out the TxD pin. RCKB is zero and cannot be set while in normal operating modes.

SCR2-SCR0 — SCI baud-rate selects

These bits select the baud rate for both the transmitter and the receiver. The prescaler output selected by SCP1 and SCP0 is further divided by the setting of these bits. Refer to Table 15.

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Table 14 - Prescaler highest baud-rate frequency output

SCP bit		Clock * divided by	Crystal frequency (MHz)				
1	0		8.3886	8.0	4.9152	4.0	3.6864
0	0	1	131.072 K Baud	125.000 K Baud	76.80 K Baud	62.50 K Baud	57.60 K Baud
0	1	3	43.690 K Baud	41.666 K Baud	25.60 K Baud	20.833 K Baud	19.20 K Baud
1	0	4	32.768 K Baud	31.250 K Baud	19.20 K Baud	15.625 K Baud	14.40 K Baud
1	1	13	10.082 K Baud	9600 K Baud	5.907 K Baud	48000 K Baud	4430 K Baud

* The clock in the «clock divide by» column is the internal processor clock.

Table 15 - Transmit baud-rate output for a given prescaler output

SCR bit			Divided by	Representative highest output for baud-rate output				
2	1	0		131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud
0	0	0	1	131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud
0	0	1	2	65.536 K Baud	16.384 K Baud	38.40 K Baud	9600 Baud	4800 Baud
0	1	0	4	32.768 K Baud	8.192 K Baud	19.20 K Baud	4800 Baud	2400 Baud
0	1	1	8	16.384 K Baud	4.096 K Baud	9600 Baud	2400 Baud	1200 Baud
1	0	0	16	8.192 K Baud	2.048 K Baud	4800 Baud	1200 bau	600 Baud
1	0	1	32	4.096 K Baud	1.024 K Baud	2400 Baud	600 Baud	300 Baud
1	1	0	64	2.048 K Baud	512 Baud	1200 Baud	300 Baud	150 Baud
1	1	1	128	1.024 K Baud	256 Baud	600 Baud	150 Baud	75 Baud

6.13 - Serial peripheral interface

The serial peripheral interface (SPI) is a high-speed synchronous serial I/O system. The transfer rate is software selectable up to one-half of the MCU E clock rate. The SPI may be used for simple I/O expansion or to allow several MCUs to be interconnected in a multimaster configuration. Clock phase and polarity are software programmable to allow direct compatibility with a large number of peripheral devices.

Four basic signal lines are associated with the SPI system. These are the master-out-slave-in (MOSI), the master-in-slave-out (MISO), the serial clock (SCK), and the slate select (SS). When data is written to the SPI data register of a master device, a transfer is automatically initiated. A series of eight SCK clock cycles are generated to synchronize data transfer.

When a master device transmits data to a slave device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal. The byte transmitted is replaced by the byte received, thereby eliminating the need for separate transmit-empty and receiver-full status bits. Figure 24 shows a block diagram of the SPI.

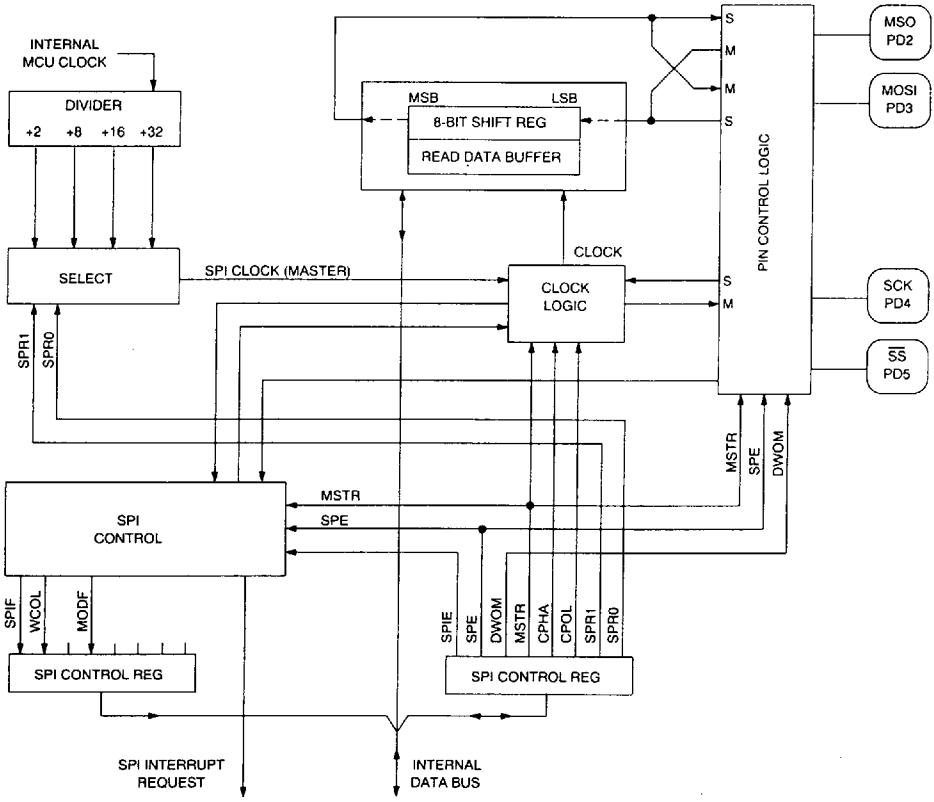


Figure 26 : Opcode map.

SPI REGISTERS

There are three registers in the SPI that provide control, status, and data-storage functions. These registers are described in the following paragraphs.

Serial peripheral control register (SPCR)

7	6	5	4	3	2	1	0
SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET							
0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable
- 1 = SPI interrupt if SPIF = 1
- 0 = SPIF interrupts disabled

SPE — Serial Peripheral system Enable
- 1 = SPI system on
- 0 = SPI system off

DWOM — port D Wire-OR Mode option

This bit affects all six port D together.
- 1 = port D outputs act as open-drain outputs
- 0 = port D outputs are normal CMOS outputs

MSTR — master mode select
- 1 = master mode
- 0 = slave mode

CPOL — Clock Polarity

This bit selects the polarity of the SCK clock.
- 1 = SCK line idles high
- 0 = SCK line idles low

CPHA — Clock PHAse

This bit selects one of two fundamentally different clock protocols. Refer to Figure 25.

If CPHA = 0, transfer begins when SS goes low and ends when SS goes high after eight clock cycles on SCK. If CPHA = 1, transfer begins the first time SCK becomes active while SS is low and ends when the SPIF flag gests set.

SPR1 and SPR0 — SPI clock rate select

These two bits select on of four baud rates to be used as SCK if the SPI is set as the master. They have no effect in the slave mode.

SPR1	SPR0	Internal processor clock divide by
0	0	5
0	1	4
1	0	16
1	1	32

Serial Peripheral Status Register (SPSR) $1029

7	6	5	4	3	2	1	0
SPIF	WCOL	0	MODF	0	0	0	0
RESET							
0	0	0	0	0	0	0	0

SPIF — SPI transfer complete flag

1 = automatically set when data transfer is complete between processor and external device

0 = cleared by a read of SPSR (with SPIF = 1), followed by a access (read or write) of the SPDR.

WCOL — Write COLlision

1 = automatically set when an attempt is made to write to the SPI data register while data is being transferred

0 = cleared by a read of SPSR (with WCOL = 1), followed by an access (read or write) of the SPDR.

Bit 5 — not implemented

This bit always reads zero.

MODF — mode fault

This bit indicates the possibility of a multi-master conflict for system control and therefore allows a proper exit from system operation to a reset or default system state.

1 = automatically set when a master device has its SS pin pulled low

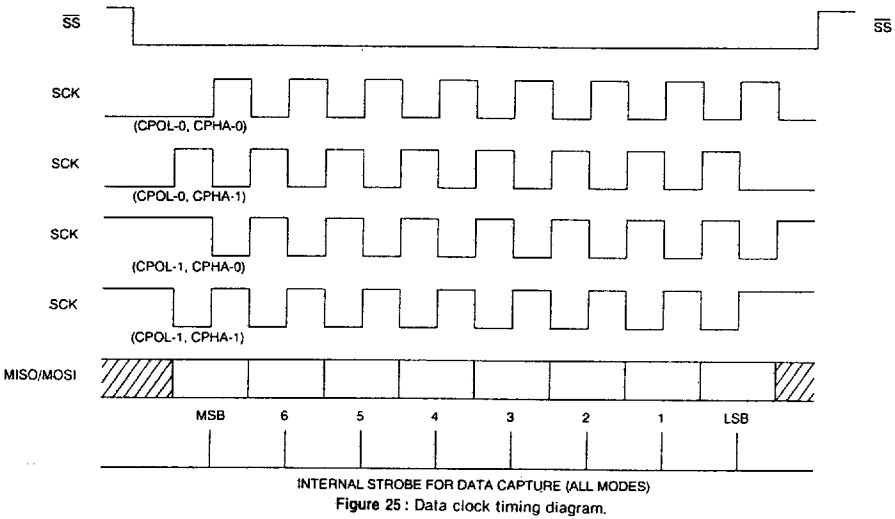


Figure 25 : Data clock timing diagram.

0 = cleared by a read of SPSR (with MODF = 1), followed by a write to the SPCR.

Bits 3-0 — not implemented

These bits always read zero.

Serial peripheral data I/O (SPDR)

This register is used to transmit and receive data on the serial bus. A write to this register in a master will initiate transmission/reception of another byte. A slave writes data to this register for later transmission to a master. When transmission is complete, the SPIF status bit is set in both the master and slave device. When a read is performed on the SPDR, a buffer is actually being read. The first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated, or an overrun condition will exist. In case of an overrrun, the byte causing the overrrun is lost.

6.14 · Analog-to-digital converter

The MCU contains an 8-channel, multiplexed-intput, successive approximation, analog-to-digital (A/D) converter with sample and hold. Two dedicated lines (V_{RL}, and V_{RH}) are provided for the reference supply voltage input. These pins are used instead of the device power pins to increase the accuracy of the A/D converions.

The 8-bit A/D conversions of the MCU are accurate to within ± 1 LSB (± 1/2 LSB quantizing errors and ± 1/2 LSB all other errors combined). Each conversion is accomplished in 32 MCU E-clock cycles. An internal control bit allows selection of an internal conversion clock oscillator that allows the A/D to be used with very low MCU clock rates. A typical conversion cycle requires 16 microseconds to complete at a 2-MHz bus frequency.

Four result registers are included to further enhance the A/D subsystem along with control logic to control conversion activity automatically. A single write instruction selects one of four conversion sequences, resulting in a conversion complete flag after the first four conversions. The sequences are as follows :

- Convert one channel four times and stop, sequential results placed in the result registers.
- Convert one group of four channels and stop, each result register is dedicated to one channel.
- Convert one channel continuously, updating the result registers in a roud-robin fashion.
- Convert one group of four channels (roud-robin fashion) continuously, each result register is dedicated to one channel.

6.15 - Instruction set

The MCU can execute all of the M6800 and M6801 instructions. In addition to these instructions, 91 new opcodes are provided by the paged opcode map. These instructions can be divided into five different types :

- accumulator and memory,
- index register and stack pointer,
- jump, branch, and program control,
- bit manipulation, and
- conditon code register instructions.

The following paragraphs briefly explain each type.

ACCUMULATOR/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The accumulator/memory instructions can be divided into four subgroups :

- load/store/transfer,
- arithmetic/math,
- logical, and
- shift/rotate.

The following paragraphs describe the different groups of accumulator/memory instructions.

Load/Store/Transfer
Refer to the following table for load/store/transfer instructions.

Function	Mnemonic
Clear memory byte	CLR
Clear accumulator A	CLRA
Clear accumulator B	CLRB
Load accumulator A	LDAA
Load accumulator B	LDAB
Load double accumulator D	LDD
Push A onto stack	PSHA
Push B onto stack	PSHB
Pull A from stack	PULA
Pull B from stack	PULB

Function	Mnemonic
Store accumulator A	STAA
Store accumulator B	STAB
Store accumulator D	STD
Transfer A to B	TAB
Transfer A to CC register	TAP
Transfer B to A	TBA
Transfer CC register to A	TPA
Exchange D with X	XGDX
Exchange D with Y	XGDY

Logical
This group is used to make comparisions, decisions, and extractions of data. Refer to the following list for the logical instructions.

Function	Mnemonic
AND A with memory	ANDA
AND B with memory	ANDB
Bit(s) test A with memory	BITA
Bit(s) test B with memory	BITB
1's complement memory byte	COM
1's complement A	COMA

Function	Mnemonic
1's complement B	COMB
Exclusive OR A with memory	EORA
Exclusive OR B with memory	EORB
OR accumulator A (inclusive)	ORAA
OR accumulator B (inclusive)	ORAB

Shift/Rotate
The shift and rotate instructions automatically operate through the carry bit, which allows easy extension to multiple bytes. Refer to the following list for the shift/rotate instructions.

Function	Mnemonic
Arithmetic shift left	ASL
(Logical shift left)	(LSL)
Arithmetic shift left A	ASLA
(Logical shift left accumulator A)	(LSLA)
Arithmetic shift left B	ASLB
(Logical shift left accumulator B)	(LSLB)
Arithmetic shift left double	ASLD
(Logical shift left double)	(LSLD)
Arithmetic shift right	ASR
Arithmetic shift right A	ASRA
Arithmetic shift right B	ASRB

Function	Mnemonic
Logical shift right	LSR
Logical shift right accumulator A	LSRA
Logical shift right accumulator B	LSRB
Logical shift right double	LSRD
Rotate left	ROL
Rotate left accumulator A	ROLA
Rotate left accumulator B	ROLB
Rotate right	ROR
Rotate right accumulator A	RORA
Rotate right accumulator B	RORB

Arithmetic/Math
Refer to the following table for the arithmetic/math instructions.

Function	Mnemonic
Add accumulators	ABA
Add B to X	ABX
Add B to Y	ABY
Add with carry to A	ADCA
Add with carry to B	ADCB
Add memory to A	ADDA
Add memory to B	ADDB
Add 16-bit to D	ADDD
Compare A to B	CBA
Compare A to memory	CMPA
Compare B to memory	CMPB
Compare D to memory (16 bit)	CPD
Decimal adjust A	DAA
Decrement memory byte	DEC
Decrement accumulator A	DECA
Decrement accumulator B	DECB
Fractional divide 16 × 16	FDIV

Function	Mnemonic
Integer divide 16 × 16	IDIV
Increment memory byte	INC
Increment accumulator A	INCA
Increment accumulator B	INCB
Multiply 8 × 8	MUL
2's complement memory byte	NEG
2's complement A	NEGA
2's complement B	NEGB
Subtract B from A	SBA
Subtract with carry from A	SBCA
Subtract with carry from B	SBCB
Subtract memory from A	SUBA
Subtract memory from B	SUBB
Subtract memory from D	SUBD
Test for zero or minus	TST
Test for zero or minus A	SBA
Test for zero or minus B	TSTB

INDEX-REGISTER AND STACK-POINTER INSTRUCTIONS
These instructions provide a method for storing data and for manipulation of index register, stack pointer, and individual segments of data within the register and stack pointer. Refer to the following list for the index-register and stack-pointer instuctions.

Function	Mnemonic
Add B to X	ABX
Add B to Y	ABY
Compare X to memory (16 bit)	CPX
Compare Y to memory (16 bit)	CPY
Decrement stack pointer	DES
Decrement index register X	DEX
Decrement index register Y	DEY
Increment stack pointer	INS
Increment index register X	INX
Increment index register Y	INY
Load index register X	LDX
Load index register Y	LDY
Load stack pointer	LDS

Function	Mnemonic
Push X onto stack (low first)	PSHX
Push Y onto stack (low first)	PSHY
Pull X from stack (high first)	PULX
Pull Y from stack (high first)	PULY
Store stack pointer	STS
Store index register X	STX
Store index register Y	STY
Transfer stack pointer to X	TSX
Transfer stack pointer to Y	TSY
Transfer X to stack pointer	TXS
Transfer Y to stack pointer	TYS
Exchange D with X	XGDX
Exchange D with Y	XGDY

BIT-MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any bit residing in the first 256 bytes of the memory space in direct address mode. The MCU can use any bit in the 64K memory map, and all bit-manipulation instructions can be used with direct or index (x or y) addressing modes. Software can configure the memory map so that internal RAM, and/or internal registers, or external memory space can occupy these addresses. The bit-manipulation instructions use an 8-bit mask, which allows simultaneous operations on any combination of bits in a location. Refer to the following list for the bit-manipulation instructions.

6

Function	Mnemonic
Clear bit(s)	BCRL
Branch if bit(s) clear	BRCRL

Function	Mnemonic
Branch if bit(s) set	BRSET
Set bit(s)	BSET

JUMPS/BRANCHES/PROGRAM-CONTROL INSTRUCTIONS

These instructions provide techniques for modifying the normal sequence of the program for conditional and unconditional branching. Refer to the following list for the jump/branch/program-control instructions.

Function	Mnemonic
Branch if carry clear	BCC
(Branch if higher or same)	(BHS)
Branch if carry set	BCS
(Branch if lower)	(BLO)
Branch if = zero	BEQ
Branch if ≥ zero	BGE
Branch if > zero	BGT
Branch if higher	BHI
Branch if ≤ zero	BLE
Branch if lower or same	BLS
Branch if < zero	BLT
Branch if minus	BMI
Branch if not = zero	BNE
Branch if plus	BPL
Branch always	BRA

Function	Mnemonic
Branch if bit(s) clear	BRCLR
Branch never	BRN
Branch if bit(s) set	BRSET
Branch to subroutine	BSR
Branch if overflow clear	BVC
Branch if overflow set	BVS
Jump	JMP
Jump to subroutine	JSR
No operation	NOP
Return from interrupt	RTI
Return from subroutine	RTS
Stop internal clocks	STOP
Software interrupt	SWI
Test operation (test mode only)	TEST
Wait for interrupt	WAI

CONDITION-CODE-REGISTER INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to the following list for the condition-code-register instructions.

Function	Mnemonic
Clear carry bit	CLC
Clear interrupt mask	CLI
Clear overflow flag	CLV
Set carry	SEC

Function	Mnemonic
Set interrupt mask	SEI
Set overflow flag	SEV
Transfer A to CC register	TAP
Transfer CC register to A	TPA

OPCODE MAP SUMMARY

Table 26 is an opcode map for the instructions used on the MCU.

6.16 - Addressing modes

The MCU uses six different addressing modes to provide the programmer with an opportunity to optimize the code for all situations. Some instructions require an additional byte before the opcode to accomodate a multipage opcode map ; this byte is called a prebyte.

The term «effective address» (EA) is used in describing the various addressing modes. Effective address is defined as the address from which the argument for an instruction is fetched or stored. The following paragraphs describe the different addressing modes.

IMMEDIATE

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. These are two, three, or four (if prebyte is required) byte instructions.

DIRECT

In the direct addressing mode, the least-significant byte of the operand address is contained in a single byte following the opcode and the most-significant byte of an address is assumed to be $00. Direct addressing allows the user to directly address $0000 through $00FF using two-byte instructions, and execution time is reduced by eliminating the additional memory access. In most applications, this 256-byte area is reserved for frequently referenced data. In the MCU, software can configure the memory map so that internal RAM, and/or internal registers, or external memory space can occupy these addresses.

EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. These are three or four (if prebyte is required) byte instructions : one or two for the opcode and two for the effective address.

INDEXED

In the indexed addressing mode, one of the index registers (X or Y) is used in calculating the effective address. In this case, the effective address is variable and depends on two factors :

- the current contents of the index register (X or Y) being used, and
- the 8-bit unsigned offset contained in the instruction.

This addressing mode allows referencing any memory location in the 64K byte address space. These are usually two or three (if prebyte is required) byte instructions, the opcode plus the 8-bit offset.

RELATIVE

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode is added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instructions. These are usually two-byte instructions.

INHERENT

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator as well as the control instruction with no other arguments are included in this mode. These instructons are one-or two-byte instructions.

PREBYTE

To expand the number of instructions used in the MCU, a prebyte instruction has been added to certain instructions. The instructions affected are usually associated with index register Y. Accessing opcodes from pages 2, 3, or 4 would require a prebyte instruction.

HI / LOW	INH 0	INH 1	REL 2	INH 3	ACCA 4	ACCB 5	INDX(Y) 6	EXT 7	IMM 8	DIR 9	INDX(Y) A	EXT B	IMM C	DIR D	INDX(Y) E	EXT F	HI / LOW
0	TEST	SBA	BRA	TSX(Y)	NEGA	NEGB	NEG	NEG	SUBA	SUBA	SUBA	SUBA	SUBB	SUBB	SUBB	SUBB	0
1	NOP	CBA	BRN	INS					CMPA	CMPA	CMPA	CMPA	CMPB	CMPB	CMPB	CMPB	1
2	IDIV	BRSET	BHI	PULA					SBCA	SBCA	SBCA	SBCA	SBCB	SBCB	SBCB	SBCB	2
3	FDIV	BRCLR	BLS	PULB	COMA	COMB	COM	COM	*SUBD	SUBD	*SUBD	*SUBD	ADDD	ADDD	ADDD	ADDD	3
4	LSRD	BSET	(BHS) BCC	DES	LSRA	LSRB	LSR	LSR	ANDA	ANDA	ANDA	ANDA	ANDB	ANDB	ANDB	ANDB	4
5	(LSLD) ASLD	BCLR	(BLO) BCS	TX(Y)S					BITA	BITA	BITA	BITA	BITB	BITB	BITB	BITB	5
6	TAP	TAB	BNE	PSHA	RORA	RORB	ROR	ROR	LDAA	LDAA	LDAA	LDAA	LDBB	LDBB	LDBB	LDBB	6
7	TPA	TBA	BEQ	PSHB	ASRA	ASRB	ASR	ASR		STAA	STAA	STAA		STBB	STBB	STBB	7
8	INX(Y)	PAGE 2	BVC	PULX(Y)	ASLA	ASLB	ASL	ASL	EORA	EORA	EORA	EORA	EORB	EORB	EORB	EORB	8
9	DEX(Y)	DAA	BVS	RTS	ROLA	ROLB	ROL	ROL	ADCA	ADCA	ADCA	ADCA	ADCB	ADCB	ADCB	ADCB	9
A	CLV	PAGE 3	BPL	ABX(Y)	DECA	DECB	DEC	DEC	DRAA	DRAA	ORAA	ORAA	ORAB	ORAB	ORAB	ORAB	A
B	SEV	ABA	BMI	RTI					ADDA	ADDA	ADDA	ADDA	ADDB	ADDB	ADDB	ADDB	B
C	CLC	BSET	BGE	PSHX(Y)	INCA	INCB	INC	INC	CPX(Y)	CPX(Y)	*CPX(Y)	CPX(Y)	LDD	LDD	LDD	LDD	C
D	SEC	BCLR	BLT	MUL	TSTA	TSTB	TST	TST	BSR	JSR	JSR	JSR	PAGE 4	STD	STD	STD	D
E	CLI	BRSET	BGT	WAI			JMP	JMP	LDS	LDS	LDS	LDS	LDX(Y)	LDX(Y)	LDX(Y)	*LDX(Y)	E
F	SEI	BRCLR	BLE	SWI	CLRA	CLRB	CLR	CLR	XGDX(Y)	STS	STS	STS	STOP	STX(Y)	STX(Y)	*LDD	F

INH : Inherent REL : Relative IMM : Immediate EXT : Extended DIR : Direct INDX(Y) : Index X(Y).

Mnemonic	Page	Opcode	Bytes	Cycles
CPD	3	83	4	5
	3	93	3	6
	3	B3	4	7
	3	A3	3	7
	4	A3	3	7
CPY	3	AC	3	7
CPX	4	AC	3	7
LDY	3	EE	3	6
LDX	4	EE	3	6
STY	3	EF	3	6
STX	4	EF	3	6

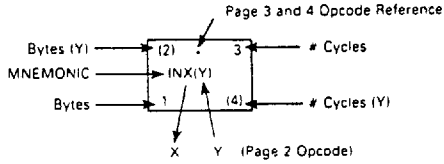


Table 16 - Opcode map

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38535 or TCS standards.

7.2 · Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with MIL-STD-883 and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

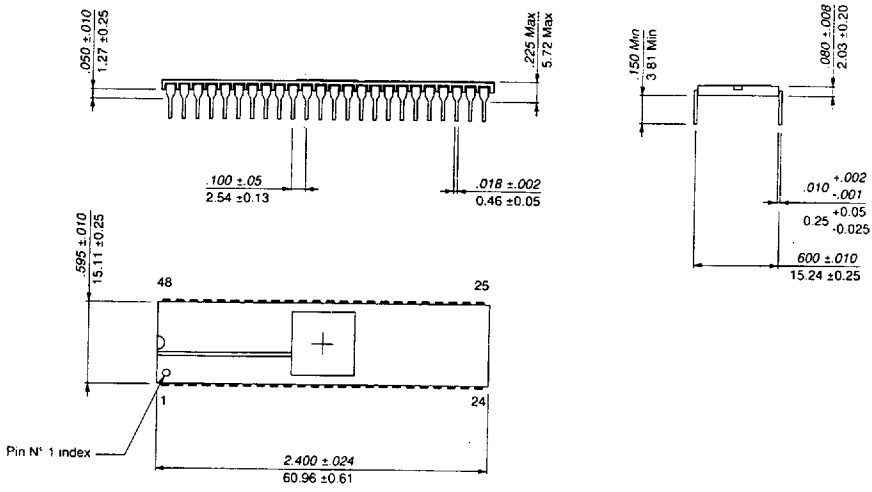
8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

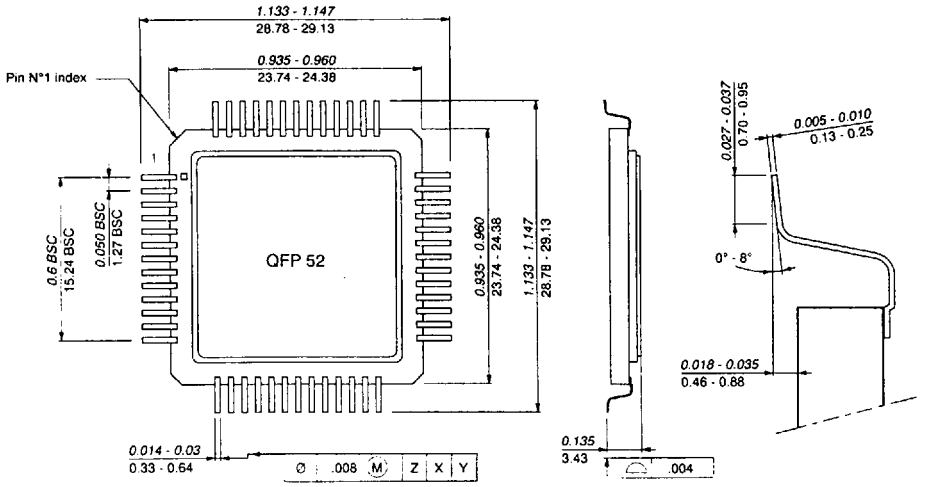
a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 %, if practical.

9 · PACKAGE MECHANICAL DATA

9.1 · 48 pins · Ceramic Side Brazed Dual in Line



9.2 - 52 pins - Ceramic Quad Flat Pack



10 - TERMINAL CONNECTIONS

10.1 - 48 pins - Ceramic Dil

See Figure 2.1 page 3.

10.2 - 52 pins - Ceramic Quad Flat Pack

See Figure 2.2 page 3.

6

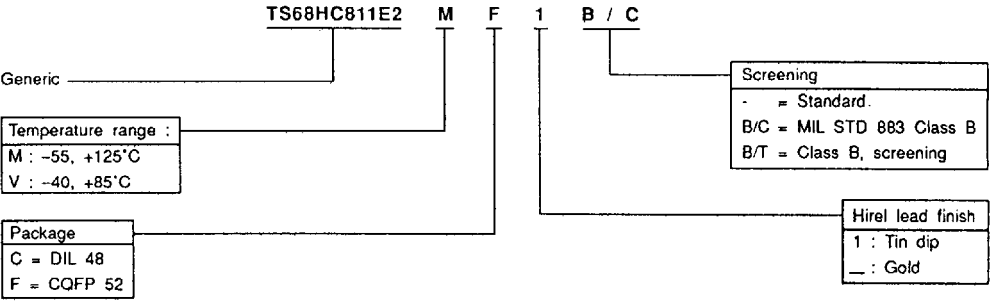
11 · ORDERING INFORMATION

11.1 · Hi-REL product

Commercial TCS part-number (see Note)	Norms	Package	Temperature range T_C (°C)	Drawing number
TS68HC11E2MCB/C	MIL-STD-883	DIL 48	−55 / +125	TCS data-sheet
TS68HC11E2MFB/C	MIL-STD-883	CQFP 52	−55 / +125	TCS data-sheet
TS68HC11E2MC1B/C	MIL-STD-883	DIL 48	−55 / +125	TCS data-sheet
TS68HC11E2MF1B/C	MIL-STD-883	CQFP 52	−55 / +125	TCS data-sheet
TS68HC11E2DES01XC	DESC	DIL 48	−55 / +125	5962-89527
TS68HC11E2DES01YC	DESC	CQFP 52	−55 / +125	5962-89527
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.				

11.2 · Standard product

Commercial TCS part-number (see Note)	Norms	Package	Temperature range T_C (°C)	Drawing number
TS68HC811E2VC	TCS standard	DIL 48	−40 / +85	Internal
TS68HC811E2MC	TCS standard	DIL 48	−55 / +125	Internal
TS68HC811E2VF	TCS standard	CQFP 52	−40 / +85	Internal
TS68HC811E2MF	TCS standard	CQFP 52	−55 / +125	Internal
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.				


TS68HC811E2 M F 1 B / C
Generic
Temperature range :
M : -55, +125°C
V : -40, +85°C
Package
C = DIL 48
F = CQFP 52
Screening
- = Standard.
B/C = MIL STD 883 Class B
B/T = Class B, screening
Hirel lead finish
1 : Tin dip
_ : Gold

6