REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outlines N and T.	98-06-01	K. A. Cottongim
B	Changed figure 1 for case outlines N and T to allow for pedestal or non-pedestal version of these case outlines. -sld	98-12-09	K. A. Cottongim
C	Added device type 04. -sld	99-04-02	K. A. Cottongim
D	Add note to paragraph 1.2.2 and table I. Table I, add note 3 to C_{IN} and C_{OUT} tests.	00-11-03	Raymond Monnin
E	Made corrections to table I in the conditions for the standby current and output leakage current tests. Made corrections to figures 5 and 6. Updated drawing to reflect the latest requirements of MIL-PRF-38534. -sld	03-12-22	Raymond Monnin
F	Table I; Changed the I_{OL} from 8 mA to 6 mA V_{OL} test. Editorial changes throughout. -sld	04-10-25	Raymond Monnin

REV																				
SHEET																				
REV	F	F	F	F	F															
SHEET	15	16	17	18	19															

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
97-12-23

REVISION LEVEL
F

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil/

MICROCIRCUIT, HYBRID, MEMORY, STATIC RANDOM ACCESS MEMORY (SRAM) 256K x 16-BIT

SIZE	CAGE CODE	
A	**67268**	**5962-96902**

SHEET 1 OF 19

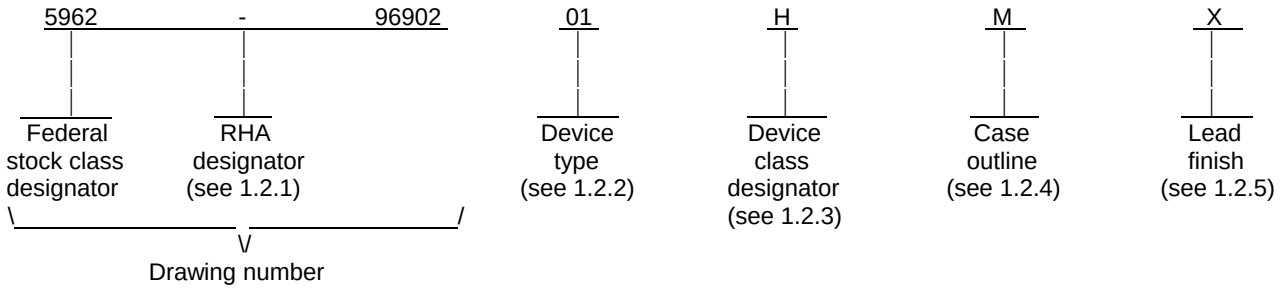
DSCC FORM 2233
APR 97

5962-E012-05

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type 1/	Generic number	Circuit function	Access time
01	WMS256K16-35DL	SRAM, 256K x 16-bit	35 ns
02	WMS256K16-25DL	SRAM, 256K x 16-bit	25 ns
03	WMS256K16-20DL	SRAM, 256K x 16-bit	20 ns
04	WMS256K16-17DL	SRAM, 256K x 16-bit	17 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.

1/ Due to the nature of the 4 transistor design of the die used in these device types, topologically pure testing is important, particularly for high reliability applications. The device manufacturer should be consulted concerning their testing methods and algorithms.

D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	See figure 1	44	Ceramic SOJ
N	See figure 1	44	Ceramic flat pack
T	See figure 1	44	Ceramic flat pack, lead formed

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +7.0 V
Input voltage range	-0.5 V to +7.0 V
Power dissipation(P_D)	1.6 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.3 V dc to +0.8 V dc
Input high voltage range(V_{IH})	+2.2 V dc to V_{CC} + 0.5 V dc
Output voltage, high minimum (V_{OH})	+2.4 V dc
Output voltage, low maximum (V_{OL})	-0.5 V to +7.0 V
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4 and 5.

3.2.5 Output load circuit. The output load circuit shall be as specified in figure 6.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$, $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DC parameters							
Operating supply current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, $f = 5\ MHz$, $V_{CC} = 5.5\ V\ dc$	1, 2, 3	All		275	mA
Standby current	I_{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, $f = 5\ MHz$, $V_{CC} = 5.5\ V\ dc$	1, 2, 3	All		17	mA
Input leakage current	I_{LI}	$V_{CC} = 5.5\ V\ dc$, V_{IN} = GND to V_{CC}	1, 2, 3	All		10	µA
Output leakage current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{OUT} = GND to V_{CC}	1, 2, 3	All		10	µA
Output low voltage	V_{OL}	$I_{OL} = 6\ mA$, $V_{CC} = 4.5\ V$	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	$I_{OH} = -4.0\ mA$, $V_{CC} = 4.5\ V$	1, 2, 3	All	2.4		V
Dynamic characteristics							
Input capacitance 3/	C_{IN}	$V_{IN} = 0\ V$, $f = 1.0\ MHz$	4	All		20	pF
Output capacitance 3/	C_{OUT}	$V_{OUT} = 0\ V$, $f = 1.0\ MHz$	4	All		20	pF
Data retention characteristics							
Data retention supply voltage	V_{DR}	$\overline{CS} \ge V_{CC} - 0.2\ V$	1, 2, 3	All	2.0	5.5	V
Data retention current	ICCDR1	$V_{CC} = 3.0\ V$	1, 2, 3	All		8.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc, V_{SS} = 0 V Unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Functional testing							
Functional tests		See 4.3.1c	7, 8A, 8B	All			
Read cycle AC timing characteristics							
Read cycle time	t_{RC}	See figure 4	9, 10, 11	01 02 03 04	35 25 20 17		ns
Address access time	t_{AA}	See figure 4	9, 10, 11	01 02 03 04		35 25 20 17	ns
Output hold from address change	t_{OH}	See figure 4	9, 10, 11	All	0		ns
Chip select access time	t_{ACS}	See figure 4	9, 10, 11	01 02 03 04		35 25 20 17	ns
Output enable to output valid	t_{OE}	See figure 4	9, 10, 11	01 02 03 04		20 15 12 10	ns
Chip select to output enable in low Z 3/	t_{CLZ}	See figure 4	9, 10, 11	01,02,03 04	5 2		ns
Output enable to output in low Z 3/	t_{OLZ}	See figure 4	9, 10 ,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$, $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle AC timing characteristics – Continued.							
Chip enable to output in high Z 3/	t_{CHZ}	See figure 4	9, 10, 11	01 02 03 04		15 12 10 9	ns
Output enable to output in high Z 3/	t_{OHZ}	See figure 4	9, 10, 11	01 02 03 04		15 12 10 9	ns
$\overline{LB}$, $\overline{UB}$, access time	t_{BA}	See figure 4	9, 10, 11	01 02 03 04		17 14 12 10	ns
$\overline{LB}$, $\overline{UB}$, enable to low Z output 3/	t_{BLZ}	See figure 4	9, 10, 11	All	0		ns
$\overline{LB}$, $\overline{UB}$, disable to high Z output 3/	t_{BHZ}	See figure 4	9, 10, 11	01 02 03 04		15 12 10 9	ns
Write cycle AC timing characteristics.							
Write cycle time	t_{WC}	See figure 5	9, 10, 11	01 02 03 04	35 25 20 17		ns
Chip select to end of write	t_{CW}	See figure 5	9, 10, 11	01 02 03 04	25 20 17 14		ns
Address valid to end of write	t_{AW}	See figure 5	9, 10, 11	01 02 03 04	25 20 17 14		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

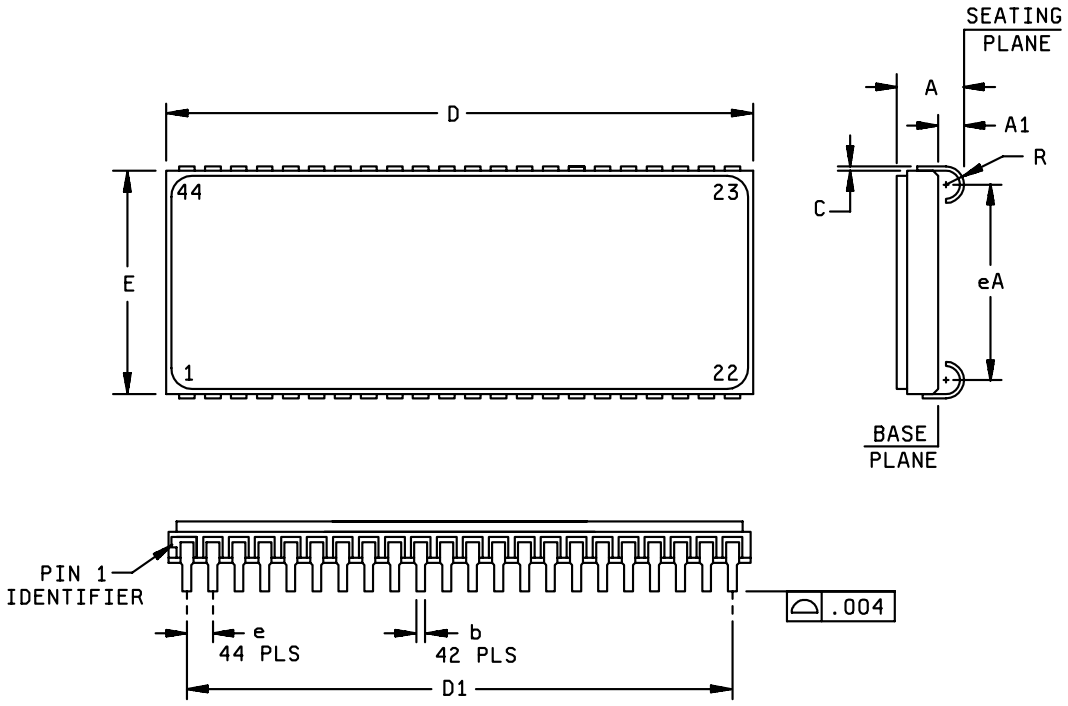
Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc, V_{SS} = 0 V Unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write cycle AC timing characteristics - Continued.							
Data valid to end of write	t_{DW}	See figure 5	9, 10, 11	01 02 03 04	20 15 12 10		ns
Write pulse width	t_{WP}	See figure 5	9, 10, 11	01 02 03 04	25 20 17 14		ns
Address setup time	t_{AS}	See figure 5	9, 10, 11	All	0		ns
Address hold time	t_{AH}	See figure 5	9, 10, 11	All	2		ns
Output active from end of write	t_{OW}	See figure 5	9, 10, 11	All	0		ns
Write enable to output in high Z 3/	t_{WHZ}	See figure 5	9, 10, 11	01 02 03 04		15 10 10 9	ns
Data hold time	t_{DH}	See figure 5	9, 10, 11	All	0		ns
$\overline{LB}$, $\overline{UB}$, valid to end of write	t_{BW}	See figure 5	9, 10, 11	01 02 03 04	25 20 17 14		ns

1/ Unless otherwise specified, the DC test conditions are as follows:
Input pulse levels; $V_{IH} = V_{CC}$ - 0.3 V and V_{IL} = 0.3 V.
Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels; V_{IH} = 3.0 V and V_{IL} = 0.0 V.
Input rise and fall times; 5 ns.
Input to output timing reference levels; 1.5 V.

2/ Due to the nature of the 4 transistor design of the die used in these device types, topologically pure testing is important, particularly for high reliability applications. The device manufacturer should be consulted concerning their testing methods and algorithms.

3/ Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be guaranteed to the limits specified in table I for all lots not specifically tested.

Case outline M.

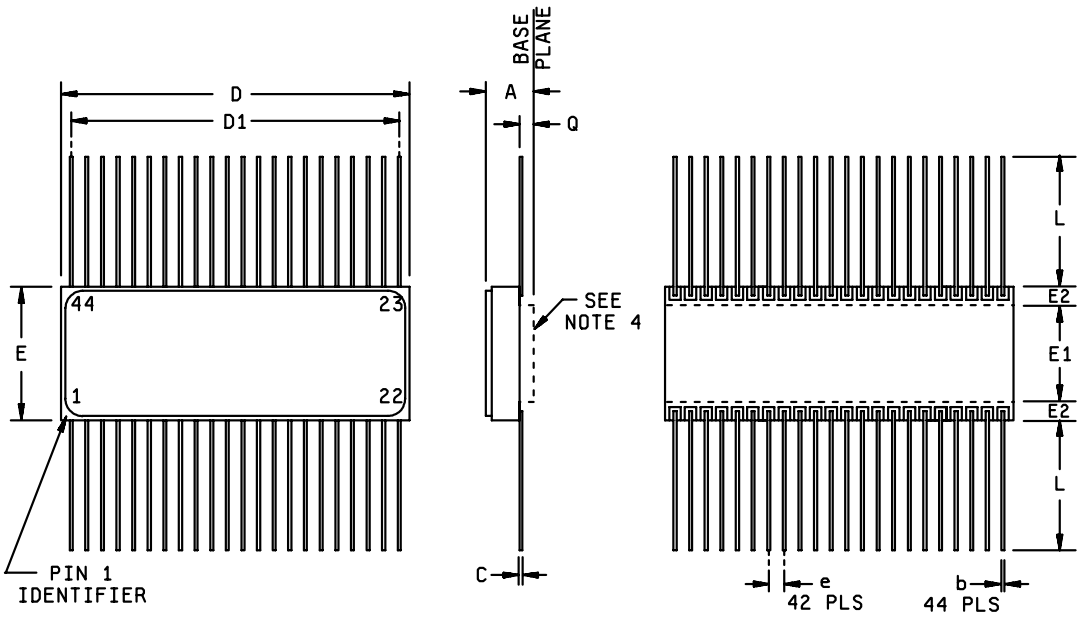


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.69	3.96	.106	.156
A1	1.01	1.52	.040	.060
b	0.38	0.48	.015	.019
C	0.15	0.25	.006	.010
D	28.44	28.95	1.120	1.140
D1	26.54	26.79	1.045	1.055
E	10.79	11.04	.425	.435
e	1.27 TYP		.050 TYP	
eA	9.29	9.80	.366	.386
R	0.88 TYP		.035 TYP	

NOTES:
1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s).

Case outline N.

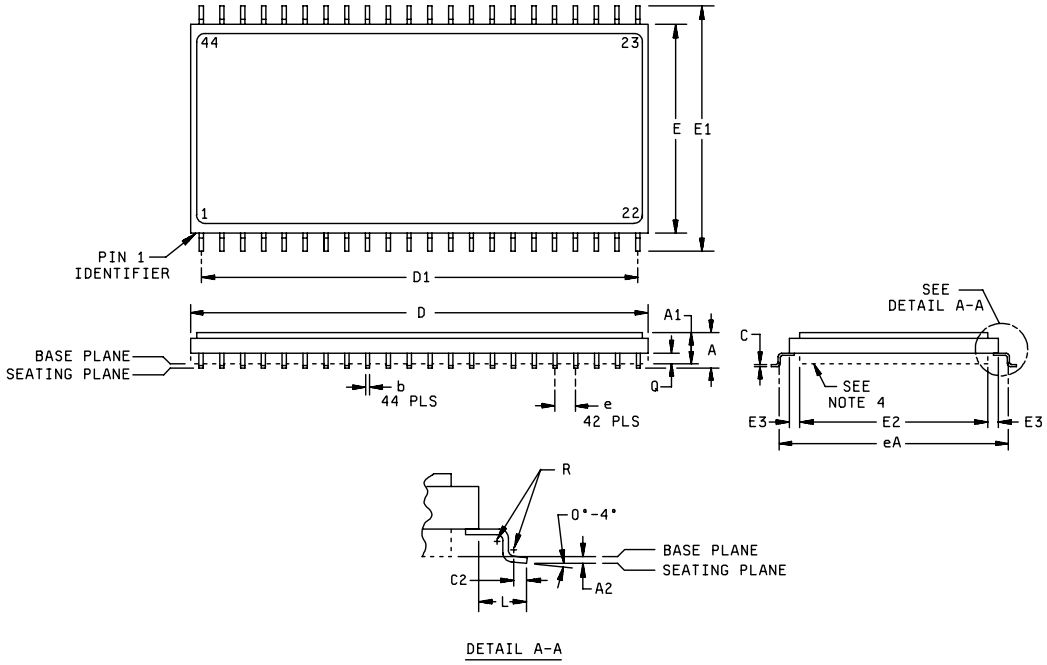


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.31	3.18	.091	.125
b	0.38	0.48	.015	.019
C	0.10	0.18	.004	.007
D	28.19	28.70	1.110	1.130
D1	26.54	26.80	1.045	1.055
E	12.83	13.80	.505	.515
E1	9.78	10.03	.385	.395
E2	1.52 TYP		.060 TYP	
e	1.27 TYP		.050 TYP	
L	9.65	10.67	.380	.420
Q	0.56	0.71	.022	.028

NOTES:
1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.
4. The case outline N is available in either a pedestal or non-pedestal package. The Q dimension only applies to the pedestal version of case outline N.

FIGURE 1. Case outline(s) - Continued.

Case outline T.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.57	3.81	.101	.150
A1	2.31	3.18	.091	.125
A2	0.25	0.64	.010	.025
b	0.38	0.48	.015	.019
C	0.10	0.18	.004	.007
C2	0.76 TYP		.030 TYP	
D	28.19	28.70	1.110	1.130
D1	26.67 TYP		1.050 TYP	
E	12.83	13.08	.505	.515
E1	16.64	16.89	.655	.665
E2	9.78	10.03	.385	.395
E3	1.52 TYP		.060 TYP	
eA	11.07 TYP		.436 TYP	
e	1.27 TYP		.050 TYP	
L	1.91 TYP		.075 TYP	
Q	0.38	0.64	.015	.025
R	0.18 TYP		.007 TYP	

NOTES:
1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.
4. The case outline T is available in either a pedestal or non-pedestal package. The Q dimension only applies to the pedestal version of case outline T.

FIGURE 1. Case outline(s) - Continued.

Device types	All	Device types	All
Case outlines	M, N, T	Case outlines	M, N, T
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	23	A10
2	A1	24	A11
3	A2	25	A12
4	A3	26	A13
5	A4	27	A14
6	$\overline{CS}$	28	NC
7	I/O1	29	I/O9
8	I/O2	30	I/O10
9	I/O3	31	I/O11
10	I/O4	32	I/O12
11	V_{CC}	33	V_{CC}
12	V_{SS}	34	V_{SS}
13	I/O5	35	I/O13
14	I/O6	36	I/O14
15	I/O7	37	I/O15
16	I/O8	38	I/O16
17	$\overline{WE}$	39	$\overline{LB}$
18	A5	40	$\overline{UB}$
19	A6	41	$\overline{OE}$
20	A7	42	A15
21	A8	43	A16
22	A9	44	A17

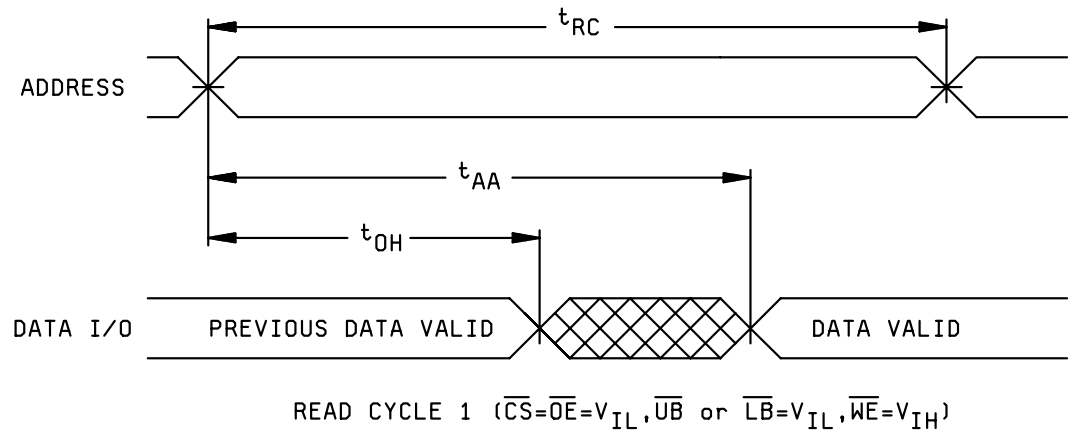
FIGURE 2. Terminal Connections.

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	Data I/O		Power
						I/O 1-8	I/O 9-16	
H	X	X	X	X	Not select	High Z	High Z	Standby
L	H	H	X	X	Output disable	High Z	High Z	Active
L	X	X	H	H	Output disable	High Z	High Z	Active
L	H	L	L	H	Read	Data out	High Z	Active
L	H	L	H	L		High Z	Data out	
L	H	L	L	L		Data out	Data out	
L	L	X	L	H	Write	Data in	High Z	Active
L	L	X	H	L		High Z	Data in	
L	L	X	L	L		Data in	Data in	

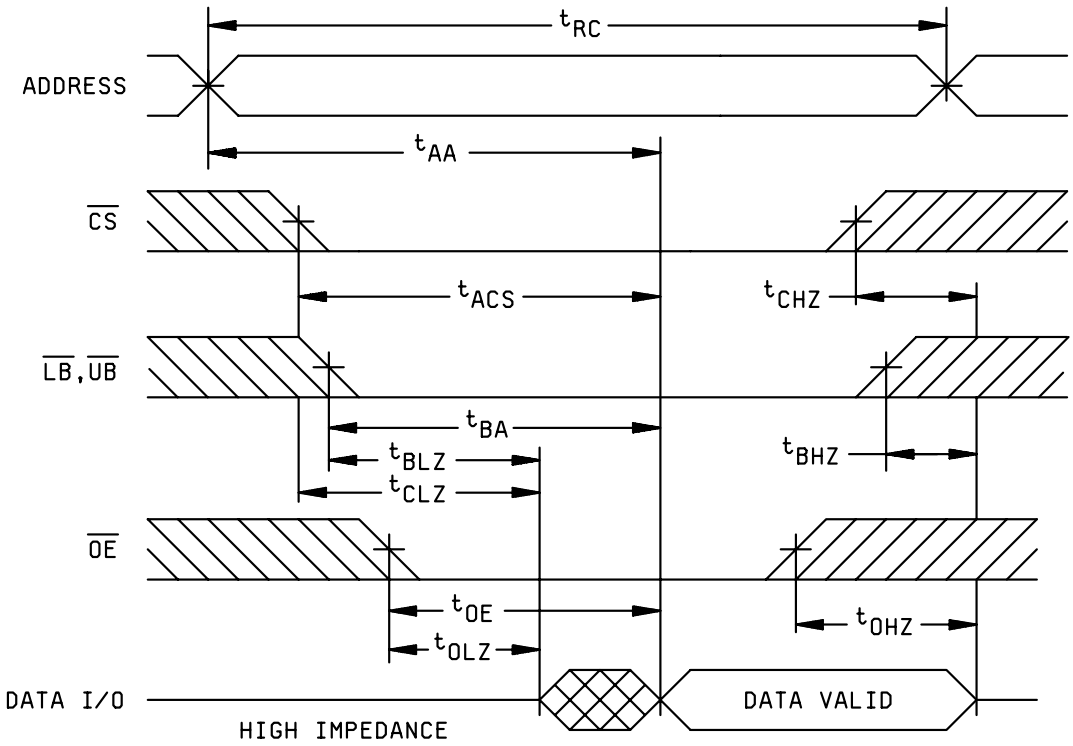
NOTES:

1. H = V_{IH} = high logic state.
2. L = V_{IL} = low logic level.
3. X = don't care (either high or low).
4. High Z = high impedance state.

FIGURE 3. Truth table.

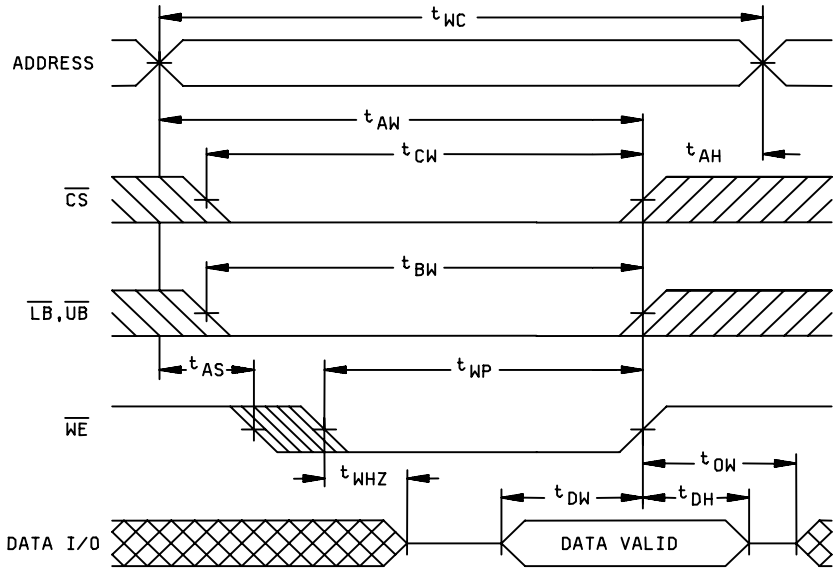


READ CYCLE 1 ($\overline{CS}$=$\overline{OE}$=V_{IL},$\overline{UB}$ or $\overline{LB}$=V_{IL},$\overline{WE}$=V_{IH})

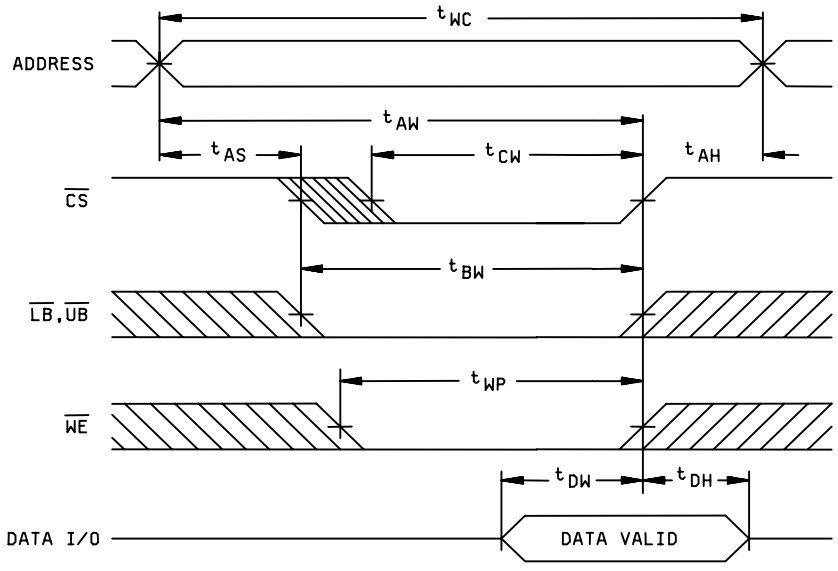


READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIGURE 4. Read cycle timing diagram.

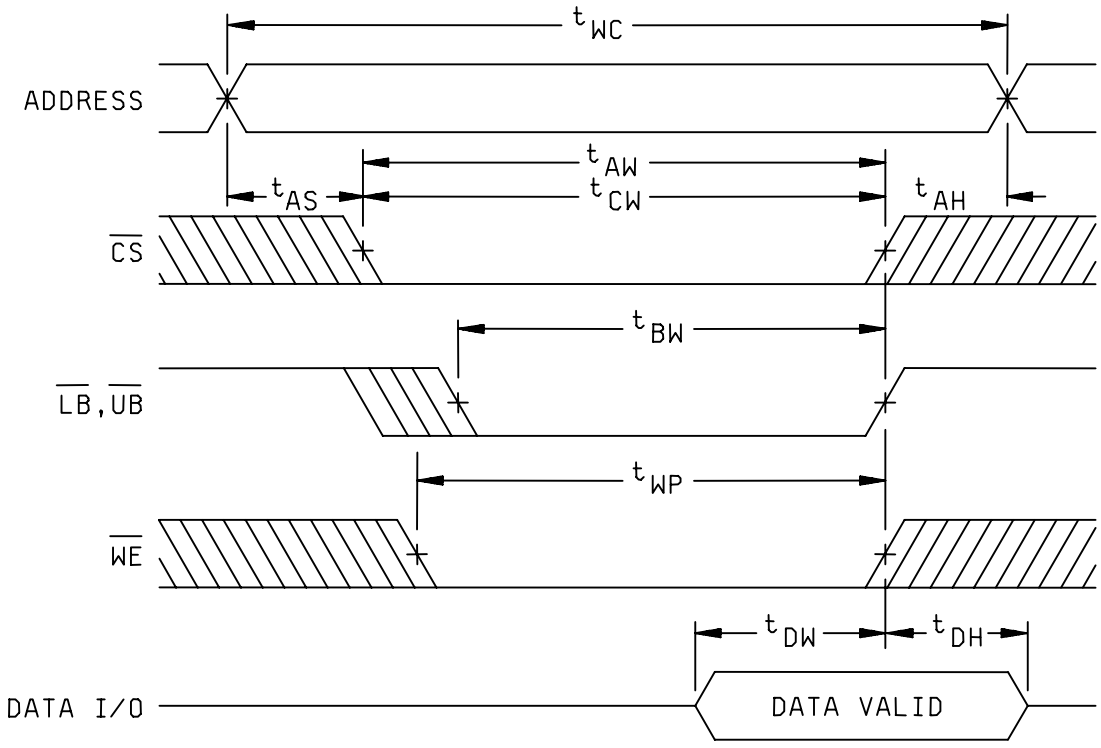


WRITE CYCLE 1 $\overline{WE}$ CONTROLLED



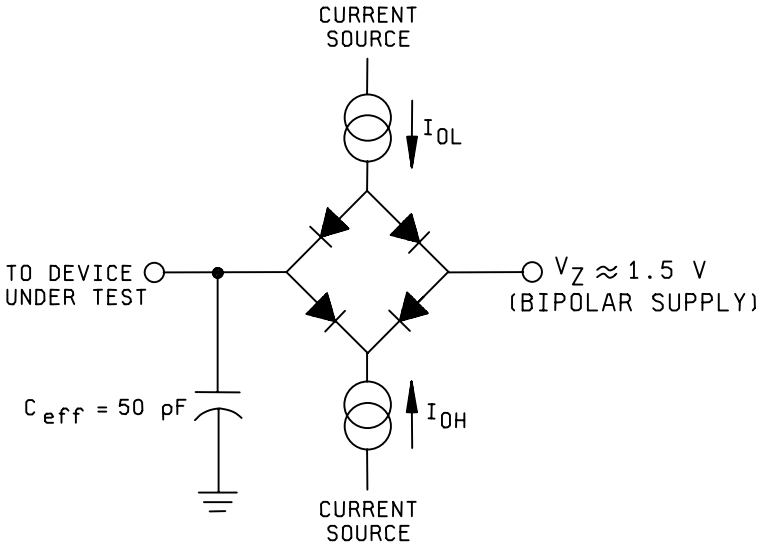
WRITE CYCLE 2 $\overline{CS}$ CONTROLLED

FIGURE 5. Write cycle timing diagram.



WRITE CYCLE 3, $\overline{LB}$, $\overline{UB}$ CONTROLLED

FIGURE 5. Write cycle timing diagram - Continued.



Parameter	Typical	Unit
Input pulse level	0 - 3.0	V
Input rise and fall	5	ns
Input and output reference level	1.5	V
Output load capacitance	50	pF

NOTES:
1. V_Z is programmable from -2 V to +7 V.
2. I_{OL} and I_{OH} programmable from 0 to 16 mA.
3. Tester impedance $Z_O = 75\Omega$.
4. V_Z is typically the midpoint of V_{OH} and V_{OL}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 6. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*,2 3 4 7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7, 8A, and 8B shall include verification of the truth table on figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-10-25

Approved sources of supply for SMD 5962-96902 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9690201HMA	54230	WMS256K16-35DLQ
5962-9690201HMC	54230	WMS256K16-35DLQ
5962-9690201HNA	54230	WMS256K16-35FLQ
5962-9690201HNC	54230	WMS256K16-35FLQ
5962-9690201HTA	54230	WMS256K16-35FGQ
5962-9690201HTC	54230	WMS256K16-35FGQ
5962-9690202HMA	54230	WMS256K16-25DLQ
5962-9690202HMC	54230	WMS256K16-25DLQ
5962-9690202HNA	54230	WMS256K16-25FLQ
5962-9690202HNC	54230	WMS256K16-25FLQ
5962-9690202HTA	54230	WMS256K16-25FGQ
5962-9690202HTC	54230	WMS256K16-25FGQ
5962-9690203HMA	54230	WMS256K16-20DLQ
5962-9690203HMC	54230	WMS256K16-20DLQ
5962-9690203HNA	54230	WMS256K16-20FLQ
5962-9690203HNC	54230	WMS256K16-20FLQ
5962-9690203HTA	54230	WMS256K16-20FGQ
5962-9690203HTC	54230	WMS256K16-20FGQ
5962-9690204HMA	54230	WMS256K16-17DLQ
5962-9690204HMC	54230	WMS256K16-17DLQ
5962-9690204HNA	54230	WMS256K16-17FLQ
5962-9690204HNC	54230	WMS256K16-17FLQ
5962-9690204HTA	54230	WMS256K16-17FGQ
5962-9690204HTC	54230	WMS256K16-17FGQ

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
54230	White Electronic Designs Corporation 3601 East University Drive Phoenix, AZ 85034