Features

- High-performance Complex Programmable Logic Devices (CPLDs)
  - 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 125 MHz maximum clock frequency
- 100% PCI compliant
- 18 outputs with 24 mA drive
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 61 MHz 18-bit accumulators
- Multiple independent clocks
- Up to 54 inputs programmable as direct, latched, or registered
- Power management options
- Multiple security bits for design protection
- 54 macrocells with programmable I/O architecture
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - 4 High-Density Function Blocks
- 0.8 µ CMOS EPROM technology
- Available in 44-pin and 68-pin PLCC and CLCC packages

General Description

The XC7354 is a high performance CPLD providing general purpose logic integration. It consists of two PAL-like 24V9 Fast Function Blocks and four High Density Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™).

Power Management

The XC7354 features a power-management scheme that permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC}\ (mA) = MC_{HP}\ (3.0) + MC_{LP}\ (2.6) + MC\ (0.006\ mA/MHz)\ f$$

Where:

MC_{HP} = Macrocells in high-performance mode
MC_{LP} = Macrocells in low-power mode
MC = Total number of macrocells used
f = Clock frequency (MHz)

Figure 1 shows a typical power calculation for the XC7354 device, programmed as three 16-bit counters and operating at the indicated clock frequency.

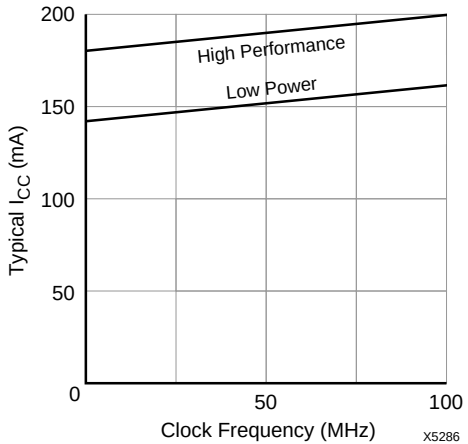


Figure 1: Typical I_{CC} vs. Frequency for XC7354

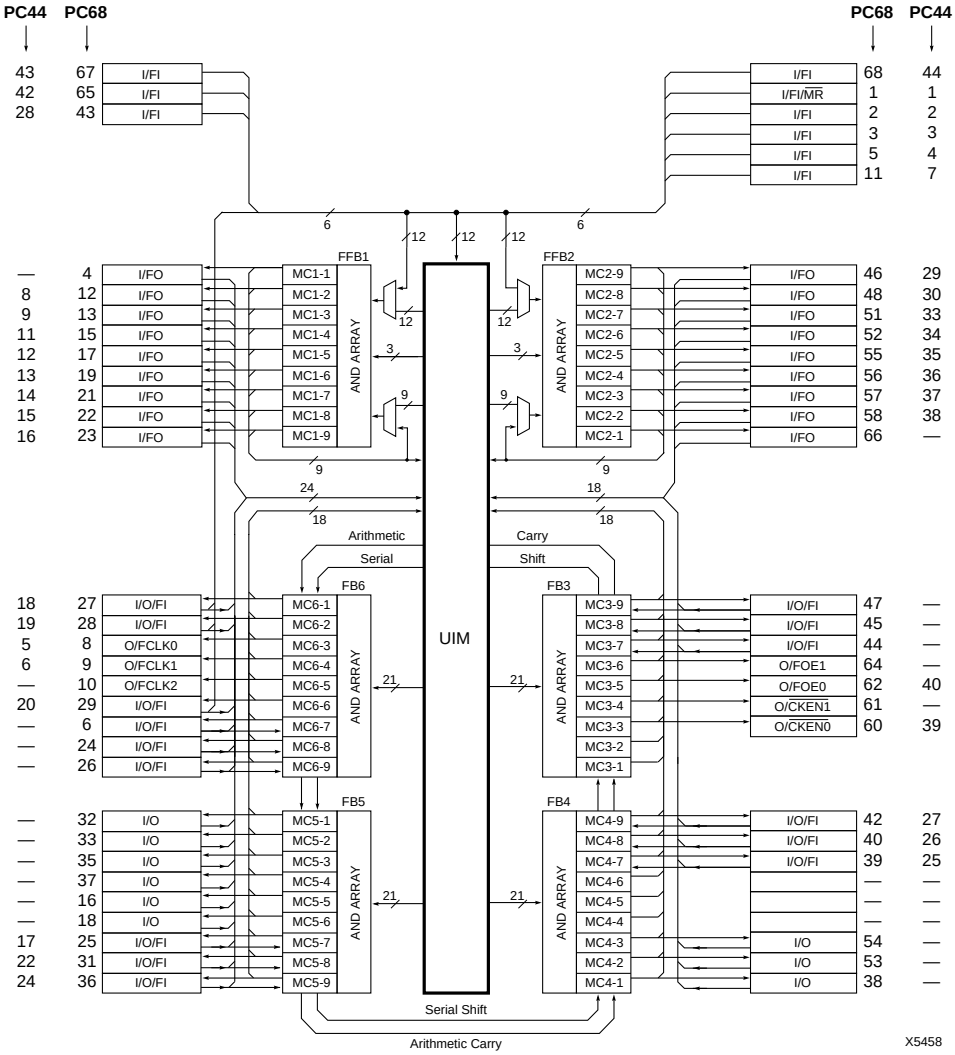


Figure 2: XC7354 Architecture

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT} V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT}[1]	Output capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}[2]	Supply current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5V f = 1.0 MHz @ 25°C	140 Typ		mA

Notes: 1. Sample tested.
2. Measured with device programmed as three 16-bit counters.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Fast Function Block (FFB) External AC Characteristics[3]

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency [1, 2, 4]	125.0		100.0		80.0		66.7		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0	ns
t_{PDFO}	Fast input to output valid [1, 2]		7.5		10.0		12.0		15.0	ns
t_{PDFU}	I/O to output valid [1, 2]		12.0		16.0		19.0		23.0	ns
t_{CWF}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
3. All appropriate AC specifications tested using Figure 3 as the test load circuit.
4. Export Control Max. flip-flop toggle rate.

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1, 2]	95.2		76.9		66.7		55.6		MHz
t_{SU}	I/O setup time before FCLK ↑ [1, 2]	10.5		13.0		15.0		18.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		13.5		17.0		20.0		24.0	ns
t_{PD}	I/O to output valid [1, 2]		16.5		22.0		27.0		32.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [1]		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [1]		3.5		5.5		7.0		8.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [1]		3.5		3.5		4.0		5.0	ns
t_{LOGILP}	Low power FB logic delay [1]		7.0		7.5		9.0		11.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	13.5		16.0		18.0		21.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0	ns
t_{CARY8}	ALU carry delay within 1 FB [2]		5.0		6.0		8.0		12.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [2]		1.0		1.5		2.0		3.0	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for adder with registered outputs.

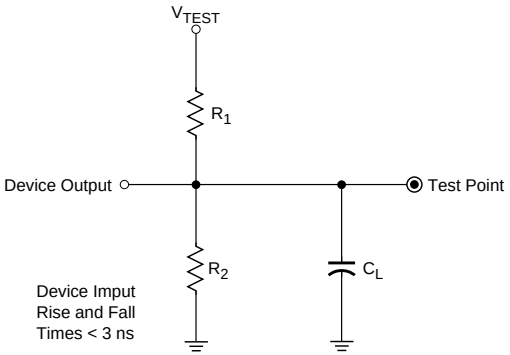
I/O Block External AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [1]	95.2		76.9		66.7		55.6		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Internal AC Characteristics

Symbol	Parameter	XC7354-7 (Com only)		XC7354-10 (Com/Ind only)		XC7354-12		XC7354-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0	ns
t_{UIM}	Universal Interconnect Matrix delay		4.5		6.0		7.0		8.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3491

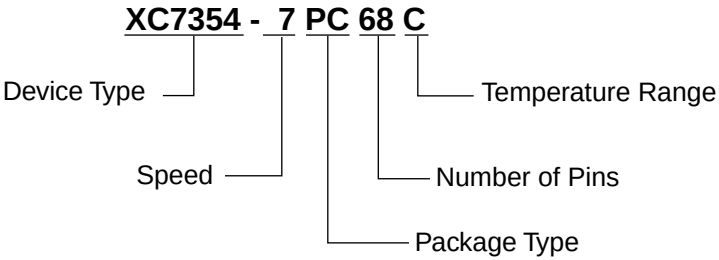
Figure 3: AC Load Circuit

XC7354 Pinouts

PC68	PC44	Input	XC7354	Output
1	1	I/FI/ $\overline{MR}$		
2	2	I/FI		
3	3	I/FI		
4	–	I/FO		MC1-1
5	4	I/FI		
6	–	I/O/FI		MC6-7
7	–		**GND**	
8	5	O/FCLK0		MC6-3
9	6	O/FCLK1		MC6-4
10	–	O/FCLK2		MC6-5
11	7	I/FI		
12	8	I/FO		MC1-2
13	9	I/FO		MC1-3
14	10		**GND**	
15	11	I/FO		MC1-4
16	–	I/O		MC5-5
17	12	I/FO		MC1-5
18	–	I/O		MC5-6
19	13	I/FO		MC1-6
20	–		V_{CCIO}	
21	14	I/FO		MC1-7
22	15	I/FO		MC1-8
23	16	I/FO		MC1-9
24	–	I/O/FI		MC6-8
25	17	I/O/FI		MC5-7
26	–	I/O/FI		MC6-9
27	18	I/O/FI		MC6-1
28	19	I/O/FI		MC6-2
29	20	I/O/FI		MC6-6
30	21		V_{CCINT}	
31	22	I/O/FI		MC5-8
32	–	I/O		MC5-1
33	–	I/O		MC5-2
34	23		**GND**	

PC68	PC44	Input	XC7354	Output
35	–	I/O		MC5-3
36	24	I/O/FI		MC5-9
37	–	I/O		MC5-4
38	–	I/O		MC4-1
39	25	I/O/FI		MC4-7
40	26	I/O/FI		MC4-8
41	–		**GND**	
42	27	I/O/FI		MC4-9
43	28	I/FI		
44	–	I/O/FI		MC3-7
45	–	I/O/FI		MC3-8
46	29	I/FO		MC2-9
47	–	I/O/FI		MC3-9
48	30	I/FO		MC2-8
49	31		**GND**	
50	32		V_{CCIO}	
51	33	I/FO		MC2-7
52	34	I/FO		MC2-6
53	–	I/O		MC4-2
54	–	I/O		MC4-3
55	35	I/FO		MC2-5
56	36	I/FO		MC2-4
57	37	I/FO		MC2-3
58	38	I/FO		MC2-2
59	–		V_{CCINT}	
60	39	O/$\overline{CKEN0}$		MC3-3
61	–	O/$\overline{CKEN1}$		MC3-4
62	40	O/FOE0		MC3-5
63	41		V_{CCINT}/V_{PP}	
64	–	O/FOE1		MC3-6
65	42	I/FI		
66	–	I/FO		MC2-1
67	43	I/FI		
68	44	I/FI		

Ordering Information



Speed Options

-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay (commercial and industrial only)
-7	7.5 ns pin-to-pin delay (commercial only)

Packaging Options

PC44	44-Pin Plastic Leaded Chip Carrier
WC44	44-Pin Windowed Ceramic Leaded Chip Carrier
PC68	68-Pin Plastic Leaded Chip Carrier
WC68	68-Pin Windowed Ceramic Leaded Chip Carrier

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C (Ambient) to 125°C (Case)

Component Availability

Pins		**44**		**68**	
Type		**Plastic PLCC**	**Ceramic CLCC**	**Plastic PLCC**	**Ceramic CLCC**
Code		**PC44**	**WC44**	**PC68**	**WC68**
XC7354	–15	CI	CI	CI	CIM
	–12	CI	CI	CI	CIM
	–10	CI	CI	CI	CI
	–7	C	C	C	C

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C M = Military = –55°C(A) to 125°C (C)