FSK Demodulator/Tone Decoder

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 2mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply provides rationometric operation for low system performance variations with power supply changes.

The XR-2211 is available in 14 pin DIP ceramic or plastic packages specified for commercial or military temperature ranges.

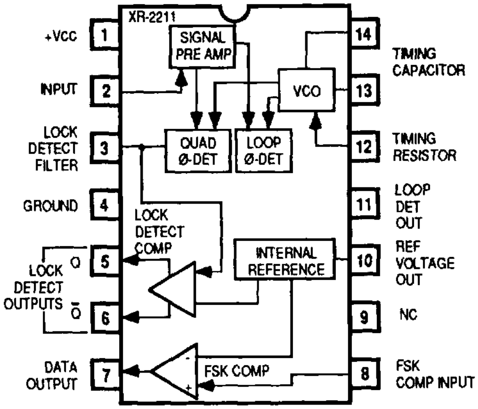
FEATURES

Wide Frequency Range	0.01Hz to 300kHz
Wide Supply Voltage Range	4.5V to 20V
HCMOS/TTL/Logic Compatibility	
FSK Demodulation, with Carrier Detection	
Wide Dynamic Range	2mV to 3V rms
Adjustable Tracking Range (±1% to 80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	900mW
Ceramic Package	750mW
Derate Above T_A = +25°C	8mW/°C
Plastic Package	800mW
Derate Above T_A = +25°C	60mW/°C
JEDEC SO	390mW
Derate Above T_A = +25°C	5mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	–55°C to +125°C
XR-2211CN	Ceramic	0°C to +70°C
XR-2211CP	Plastic	0°C to +70°C
XR-2211N	Ceramic	–40°C to +85°C
XR-2211P	Plastic	–40°C to +85°C
XR-2211D	JEDEC SO-14	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V+ = 12V, T_A = +25°C, R_O = 30KΩ, C_O = 0.033μF.

PARAMETER	2211/2211M			XR-2211C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL								
Supply Voltage	4.5		20	4.5		20	V	
Supply Curreent		4	7		5	9	mA	$R_0 \geq$ 10kΩ. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		11	13		11		%	Deviation from fo = 1/RoCo
Frequency Stability								R_1 = 1/2
Temperature		120	150		120		ppm/°C	* See Figure 8.
Power Supply		0.05	0.5		0.05		%/V	V+ = 12 ± 1V. See Fig. 7.
		0.2			0.2		%/V	V+ 5 ± 0.5V. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	R_0 = 8.2kΩ, C_0 = 400pF
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	R_0 = 2MΩ, C_0 = 50μF
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	kΩ	
Recommended Range 1	15			5		100	kΩ	See Figs. 7 and 8.
LOOP PHASE DETECTOR SECTION								
Peak Output Current	1150	1200	1300	1 100	±200	±300	μA	Measured at Pin 11.
Output Offset Current		1			±2		μA	
Output Impedance		1			1		MΩ	
Maximum Swing	14	±5		14	±5		V	Referenced to Pin 10.
QUADRATURE PHASE DETECTOR								Measured at Pin 3.
Peak Output Current	100	150			150		μA	
Output Imped		1			1		MΩ	
Maximum Swing		11			11		V pp	
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		kΩ	
Input Signal								
Voltage Required to								
Cause Limiting		2	10		2		mV rms	
VOLTAGE COMPARATOR SECTION								
Input Impedance		2			2		MΩ	Measured at Pins 3 and 8.
Input Bias Current		100			100		nA	
Voltage Gain	55	70			55 70		dB	R_L = 5.1kΩ
Output Voltage Low		300			300		mV	I_C = 3mA
Output Leakage Current		0.01			0.01		μA	V_O = 20V
INTERNAL REFERENCE								
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	Measured at Pin 10.
Output Impedance		100			100		Ω	AC Small Signal
Maximum Source Current		80			80		μA	

*These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

SYSTEM DESCRIPTION

The output of the phase detector produces sum and difference frequencies of the input and the VCO (internally connected). When in lock, these frequencies are $f_{IN} + f_{VCO}$ (2 times f_{IN} when in lock) and $f_{IN} - f_{VCO}$ (0HZ when lock). By adding a capacitor to the phase detector output, the 2 times f_{IN} component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The other sections of the XR-2211 act to: determine if the VCO is driven above or below the center frequency (FSK comparator); produced both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20KΩ. Recommended input signal level is in the range of 10mV rms to 3V rms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 2) to eliminate the chatter at lock detect outputs. It the tone detect section is not used, Pin 3 can be left open circuited.

Lock Detect Output, Q (Pin 5): The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to V+ for proper operation. At "low" state, it can sink up to 5mA of load current.

Lock Detect Complement, Q (Pin 6): The output at Pin 6 is the logic complement of the lock detect output at Pin 5. This output is also an open collector type stage which can sink 5mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R_L, to V+ for proper operation. It can sink 5mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate,

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (Pin 11). This data filter is formed by R_F and C_F of Figure 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at Pin 10.

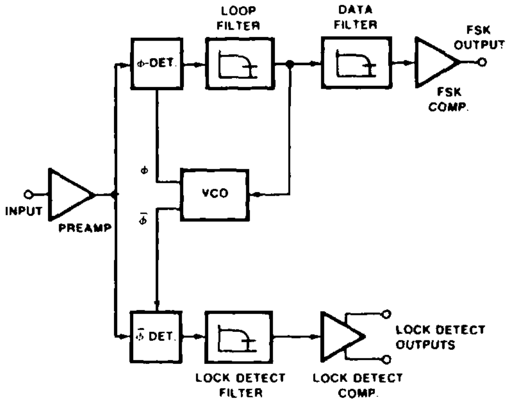


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

Reference Voltage, V_R (Pin 10): This pin is internally biased at the reference voltage level, V_R: $V_R = V+/2 - 650mV$. The dc voltage level at this pin forms an internal reference for the voltage levels at Pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1µF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 11 (see Figure 2). With no input signal, or with no phase error within the PLL, the dc level at Pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

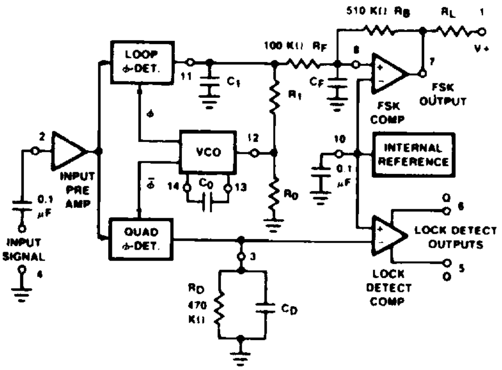


Figure 2. Generalized Circuit Connection for FSK and Tone Detection

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

where C_0 is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10KΩ to 100KΩ see Figure 8).

This terminal is a low impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤ 3mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 5). C_0 must be nonpolar, and in the range of 200pF to 10µF.

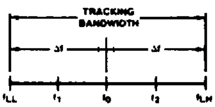
VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (see Figure 9).

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. For set-up or adjustment purposes, the VCO free-running frequency can be tuned by using the generalized circuit in Figure 2, and applying an alternating bit pattern of O's and I's at known mark and space frequencies. By adjusting R_O, the VCO can then be tuned to obtain a 50% duty cycle on the FSK output (pin 7). This will ensure that the VCO f_o value is accurately referenced to the mark and space frequencies.

DESIGN EQUATIONS

(See Figure 2 for definition of components.)

1. VCO Center Frequency, f_0:
   $f_0 = 1/R_o C_0$ Hz
2. Internal Reference Voltage, V_R (measured at Pin 10):
   $V_R = V+/2 - 650\text{mV}$
3. Loop Low-Pass Filter Time Constant, τ:
   $\tau = R_1 C_1$
4. Loop Damping, ζ:
   $$\zeta = 1/4 \sqrt{\frac{C_0}{C_1}}$$
5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:
   $\Delta f/f_0 = R_0/R_1$



6. FSK Data Filter Time Constant, τ_F:
   $\tau_F = R_F C_F$
7. Loop Phase Detector Conversion Gain, Kø: (Kø is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase detector input):
   $K\text{ø} = 02V_R/\pi$ volts/radian
8. VCO Conversion gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 11):
   $K_0 = -1/V_R C_0 R_1$ Hz/volt
9. Total Loop Gain, K_T:
   $K_T = 2\pi K\text{ø} K_0 = 4/C_0 R_1$ rad/sec/volt
10. Peak Phase Detector Current I_A:
    $I_A = V_R$ (volts)/25mA

APPLICATIONS INFORMATION

FSK Decoding

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510KΩ) from Pin 7 to Pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states. Recommended component values for some of the most commonly used FSK bands are given in Table 1.

Design Instructions:

The circuit of Figure 9 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

a) Calculate PLL center frequency, f_0:

$$f_0 = \frac{f_1 + f_2}{2}$$

b) Choose value of timing resistor R_0, to be in the range of 10KΩ to 100KΩ. This choice is arbitrary. The recommended value is R_0 = 20KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Figure 6:

$$C_0 = 1/R_0 f_0$$

d) Calculate R_1 to give a Δf equal to the mark space deviation:

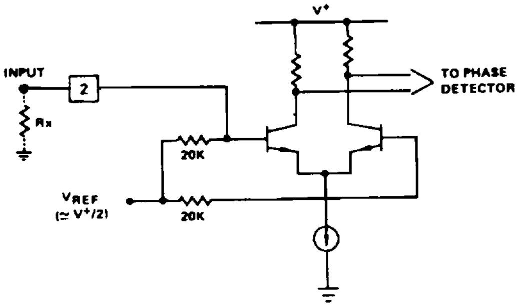
$$R_1 = R_0[f_0/(f_1 - f_2)]$$

e) Calculate C_1 to set loop damping. (See design equation No. 4.):

Normally, $\zeta \approx 1/2$ is recommended.

Then: $C_1 = C_0/4$ for $\zeta = 1/2$

f) The input to the XR-2211 may sometimes be to sensitive to noise conditions on the input line. Figure 3 illustrates a method of de-sensitizing the XR-2211 from such noisy line conditions by the use of a resistor, R_X, connected from pin 2 to ground. The value of R_X is chosen by the equation and the desired minimum signal threshold level.



$$V_{IN\ MINIMUM\ (PEAK)} \approx V^+ \left[\frac{10K}{R_X + 20K}\right] \pm 2.8\text{ mV}$$

Figure 3. Desensitizing Input Stage

g) Calculate Data Filter Capacitance, C_F:

For R_F = 100KΩ, R_B = 510KΩ, the recommended value of C_F is:

$C_F \approx 3/(\text{Baud Rate})\ \mu F$

Note: All calculated component values except R_0 can be rounded to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Figure 9.)

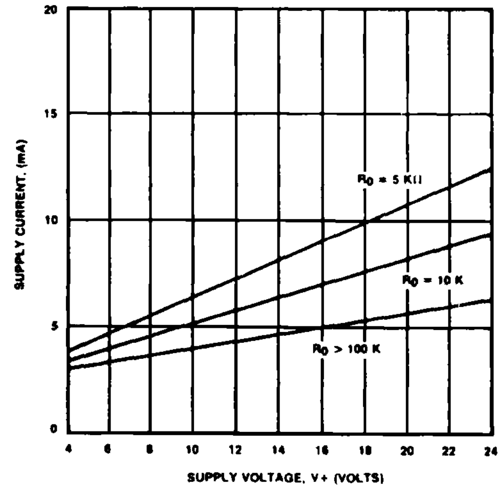


Figure 4. Typical Supply Current vs V+ (Logic Outputs Open Circuited)

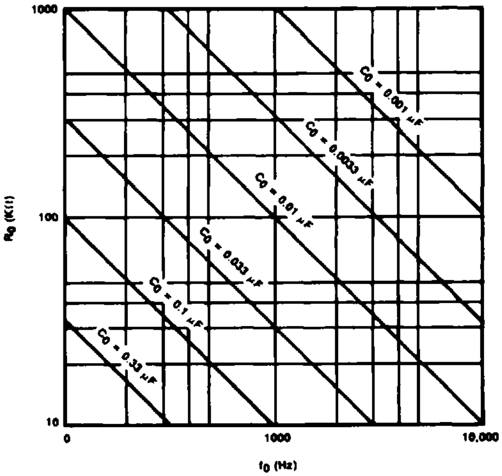


Figure 6. VCO Frequency vs Timing Capacitor

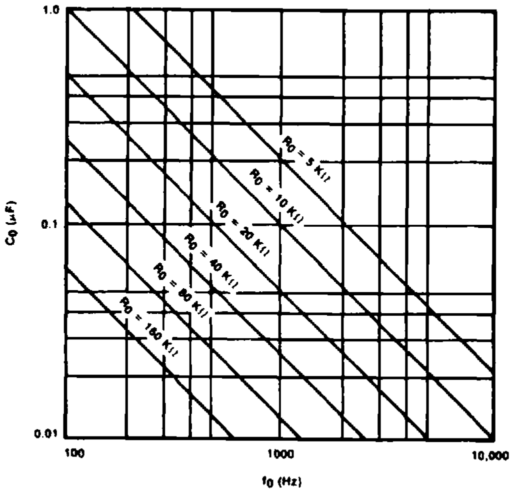


Figure 5. VCO Frequency vs Timing Resistor

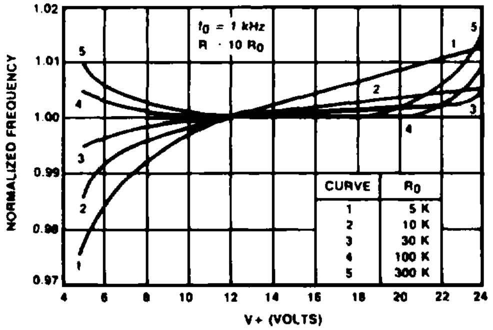


Figure 7. Typical f_0 vs Power Supply Characteristics

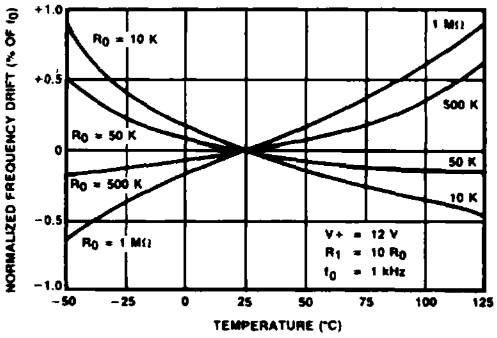


Figure 8. Typical Center Frequency Drift vs Temperature

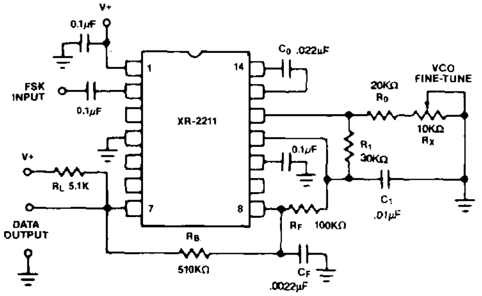


Figure 9. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format)

Design Example:

1200 Baud FSK demodulator with mark space frequencies of 1200/2200Hz:

Step 1: Calculate f_0: f_0 (1200 + 2200) (1/2) = 1700Hz

Step 2: Choose $R_0 \simeq 26.7K\Omega$ (20KΩ fixed resistor in series with 10KΩ potentiometer)

Step 3: Calculate C_0 from design equation 1: yielding $C_0 = 0.022\mu F$

Step 4: Calculate R_1: $R_1 = R_0$ (1700/1000) ≈ 45KΩ

Step 5: Calculate C_1: $C_1 = C_0/4 = 0.055\mu F \approx 0.01\mu f$

Note: All values except R_0 can be rounded to nearest standard value.

Table 1. Recommended Component Values for Commonly Used FSK Bands. (See Circuit of Figure 10.)

FSK BAND	COMPONENT VALUES	
300 Baud f_1 = 1070 Hz f_2 = 1270 Hz	$C_0 = 0.039\mu F$ $C_1 = 0.01\mu F$ $R_1 = 100K\Omega$	$C_F = 0.005\mu F$ $R_0 = 18K\Omega$
300 Baud f_1 = 2025 Hz f_2 = 2225 Hz	$C_0 = 0.022\mu F$ $C_1 = 0\ 0047\mu F$ $R_1 = 200K\Omega$	$C_F = 0.005\mu F$ $R_0 = 18K\Omega$
Caller I.D. Rec'v (1200 Baud) f1 = 1200 Hz f_2 = 2200 Hz	$C_0 = 0.022\mu F$ C1 = 0.01µF $R_1 = 45K\Omega$	$C_F = 0.0022\mu F$ R0 = 26.7KΩ $C_D = 0.1\mu F$ $R_D = 470K\Omega$

FSK Decoding with Carrier Detect

The lock detect section of XR-2211 can be used as a carrier detect option, for FSK decoding. The recommended circuit connection for this application is shown in Figure 10. The open collector lock detect output, Pin 6, is shorted to data output (Pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL and the Pin 6 output goes "high," to enable the data output.

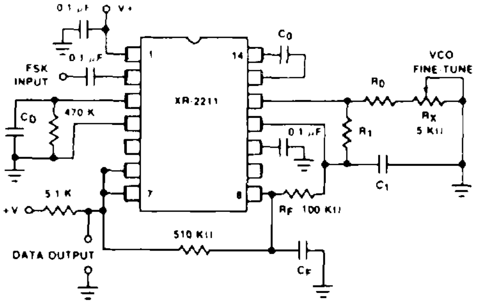


Figure 10. External Connectors for FSK Demodulation with Carrier Detect Capability

Note: Data Output is "Low" When No Carrier is Present.

The minimum value of the lock detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta f_c > \Delta f/2$. For $R_D = 470K\Omega$, the approximate minimum value of C_D can be determined by:

C_D (µF) ≥ 16/capture range in Hz.

With values of C_D that are too small, chatter can be observed on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detect output. For Caller I.D. applications choose $C_D = 0.1\mu F$.

Tone Detection

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs. Q and $\overline{Q}$ at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

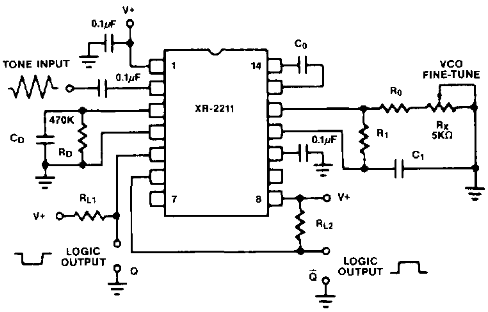


Figure 11. Circuit Connection for Tone Detection

Both logic outputs at Pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L1} and R_{L2}, as shown in Figure 11.

With reference to Figures 2 and 11, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\bar{Q}$ logic outputs.

Design Instructions:

The circuit of Figure 11 can be optimized for any tone detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input, the tone frequency, f_S, these parameters are calculated as follows:

a) Choose R_0 to be in the range of 15KΩ to 100KΩ. This choice is arbitrary.

b) Calculate C_0 to set center frequency, f_0 equal to f_S (see Figure 6): $C_0 \approx 1/R_0 f_S$

c) Calculate R_1 to set bandwidth ±Δf (see design equation No. 5):

$$R_1 = R_0(f_0/\Delta f)$$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

d) Calculate value of C_1 for a given loop damping factor;

$$C_1 = C_0/16 \zeta 2$$

Normally $\zeta \approx 1/2$ is optimum for most tone detector applications, giving $C_1 = 0.25\ C_0$.

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470KΩ, C_D must be:

$$C_D(\mu F) \geq (16/\text{capture range in Hz})$$

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of 1kHz ± 20Hz:

a) Choose R_0 = 20KΩ (18KΩ in series with 5KΩ potentiometer).

b) Choose C_0 for f_0 = 1kHz (from Figure 6): C_0 = 0.05µF.

c) Calculate R_1: $R_1 = (R_0)(1000/20)$ = 1MΩ.

d) Calculate C_1: for $\zeta = 1/2$, $C_1 = 0.25$, $C_0 = 0.013\mu F$

e) Calculate C_D: $C_D = 16/38 = 0.42\mu F$.

f) Fine-tune center frequency with 5KΩ potentiometer, R_X.

Linear FM Detection

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Figure 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post-detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 12.

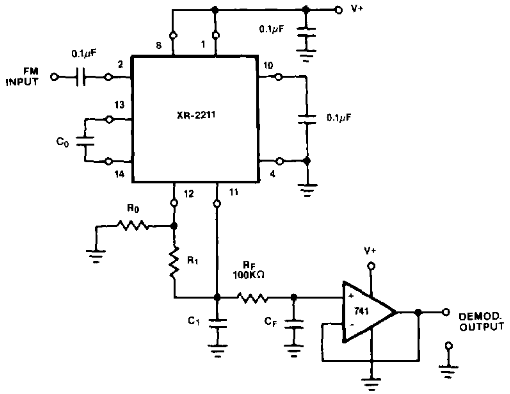


Figure 12. Linear FM Detector Using XR-2211 and an External Op Amp. (See Section an Design Equation for Component Values.)

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$$V_{OUT} = R_1 V_R/100 R_0 \text{ Volts/\% deviation}$$

where V_R is the internal reference voltage (V_R = V + /2 – 650mV). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see section on design equations.

EQUIVALENT SCHEMATIC DIAGRAM